



**Document Title**

32K x 8 Low Power SRAM with 3.3V

**Revision History**

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	October 5,2001	

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# 32K x 8 LOW VOLTAGE CMOS STATIC RAM

## FEATURES

- High-speed access time: 15, 20, 25 ns
- Automatic power-down when chip is deselected
- CMOS low power operation
  - 255 mW (max.) operating
  - 0.18 mW (max.) CMOS standby
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three-state outputs

## DESCRIPTION

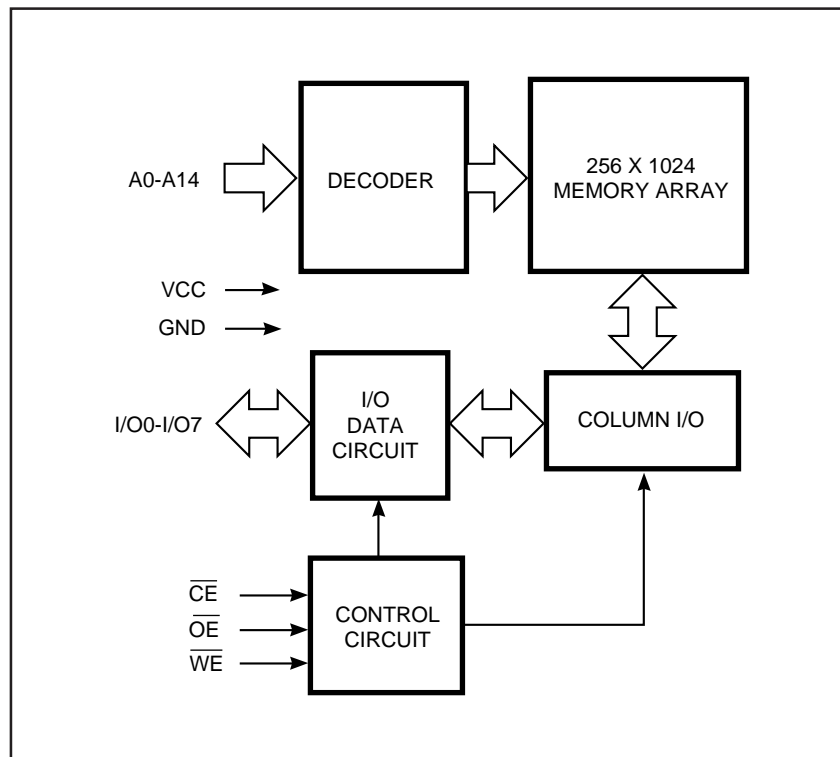
The *ICSI* IC62LV256L is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15 ns maximum.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 50  $\mu$ W (typical) with CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Enable ( $\overline{CE}$ ). The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

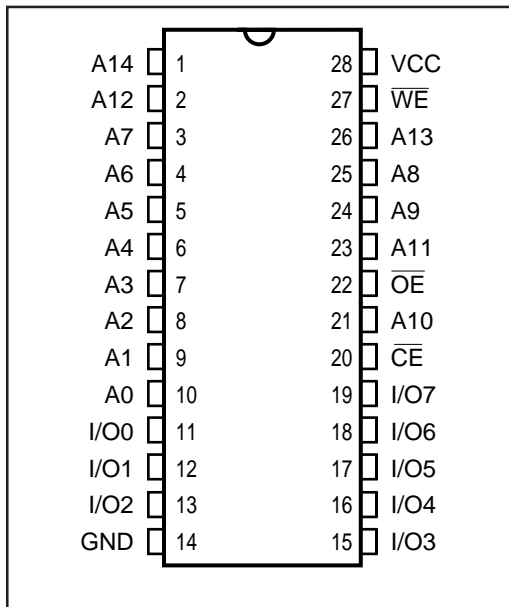
The IC62LV256L is available in the JEDEC standard 28-pin 300mil SOJ and the 8\*13.4mm TSOP-1 package.

## FUNCTIONAL BLOCK DIAGRAM

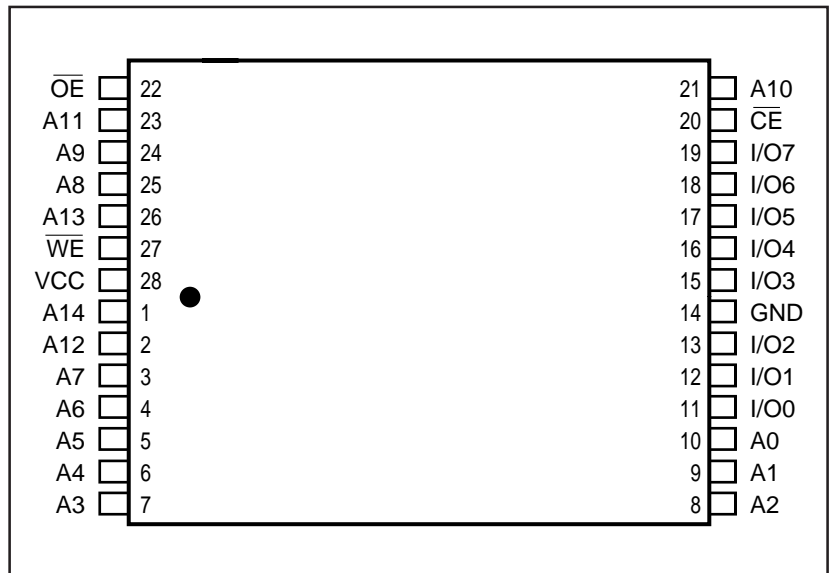


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**PIN CONFIGURATION**  
28-Pin SOJ



**PIN CONFIGURATION**  
8x13.4mm TSOP-1



**PIN DESCRIPTIONS**

A0-A14	Address Inputs
CE-bar	Chip Enable Input
OE-bar	Output Enable Input
WE-bar	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

**TRUTH TABLE**

Mode	WE-bar	CE-bar	OE-bar	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	High-Z	Isb1, Isb2
Output Disabled	H	L	H	High-Z	Icc1, Icc2
Read	H	L	L	DOUT	Icc1, Icc2
Write	L	L	X	DIN	Icc1, Icc2

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	W
I <sub>OUT</sub>	DC Output Current (LOW)	20	mA

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING RANGE**

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V +10%
Industrial	-40°C to +85°C	3.3V ± 10%

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA		2.4	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA		—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>			-0.3	0.8	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	Com. Ind.	-2 -5	2 5	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Outputs Disabled	Com. Ind.	-2 -5	2 5	μA

**Notes:**

- V<sub>IL</sub> = -3.0V for pulse width less than 10 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

**POWER SUPPLY CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	Test Conditions		-15 ns		-20 ns		-25 ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I <sub>CC1</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = 0	Com. Ind.	— —	50 60	— —	50 60	— —	50 60	mA
I <sub>CC2</sub>	V <sub>CC</sub> Dynamic Operating Supply Current	V <sub>CC</sub> = Max., $\overline{CE} = V_{IL}$ I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com. Ind.	— —	70 70	— —	60 60	— —	50 50	mA
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CE} \geq V_{IH}$ , f = 0	Com. Ind.	— —	3 5	— —	3 5	— —	3 5	mA
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>CC</sub> = Max., $\overline{CE} \geq V_{CC} - 0.2V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com. Ind.	— —	50 100	— —	50 100	— —	50 100	μA

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

**CAPACITANCE<sup>(1,2)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5	pF

**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 3.3V.

**READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup>** (Over Operating Range)

Symbol	Parameter	-15 ns		-20 ns		-25 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	15	—	20	—	25	—	ns
t <sub>AA</sub>	Address Access Time	—	15	—	20	—	25	ns
t <sub>OHA</sub>	Output Hold Time	2	—	2	—	2	—	ns
t <sub>ACE</sub>	$\overline{CE}$ Access Time	—	15	—	20	—	25	ns
t <sub>DOE</sub>	$\overline{OE}$ Access Time	—	7	—	8	—	9	ns
t <sub>LZOE<sup>(2)</sup></sub>	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	ns
t <sub>HZOE<sup>(2)</sup></sub>	$\overline{OE}$ to High-Z Output	—	8	—	9	—	10	ns
t <sub>LZCE<sup>(2)</sup></sub>	$\overline{CE}$ to Low-Z Output	3	—	3	—	3	—	ns
t <sub>HZCE<sup>(2)</sup></sub>	$\overline{CE}$ to High-Z Output	—	6	—	9	—	10	ns
t <sub>PU<sup>(3)</sup></sub>	$\overline{CE}$ to Power-Up	0	—	0	—	0	—	ns
t <sub>PD<sup>(3)</sup></sub>	$\overline{CE}$ to Power-Down	—	15	—	18	—	20	ns

**Notes:**

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

**AC TEST CONDITIONS**

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

**AC TEST LOADS**

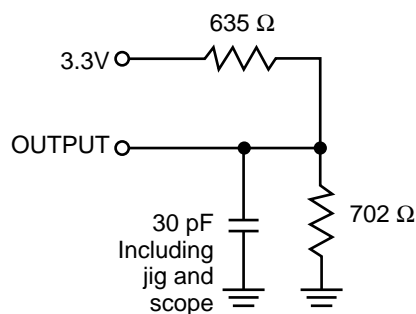


Figure 1.

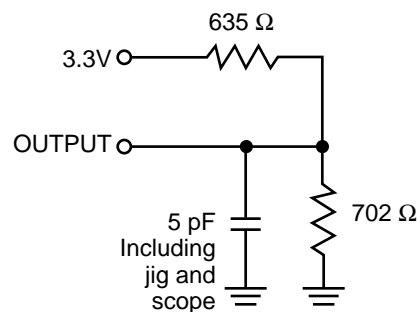
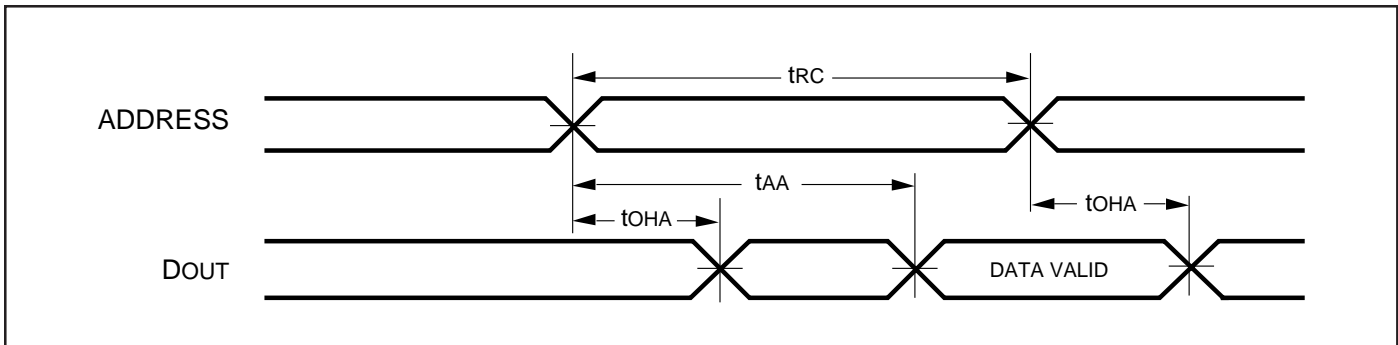


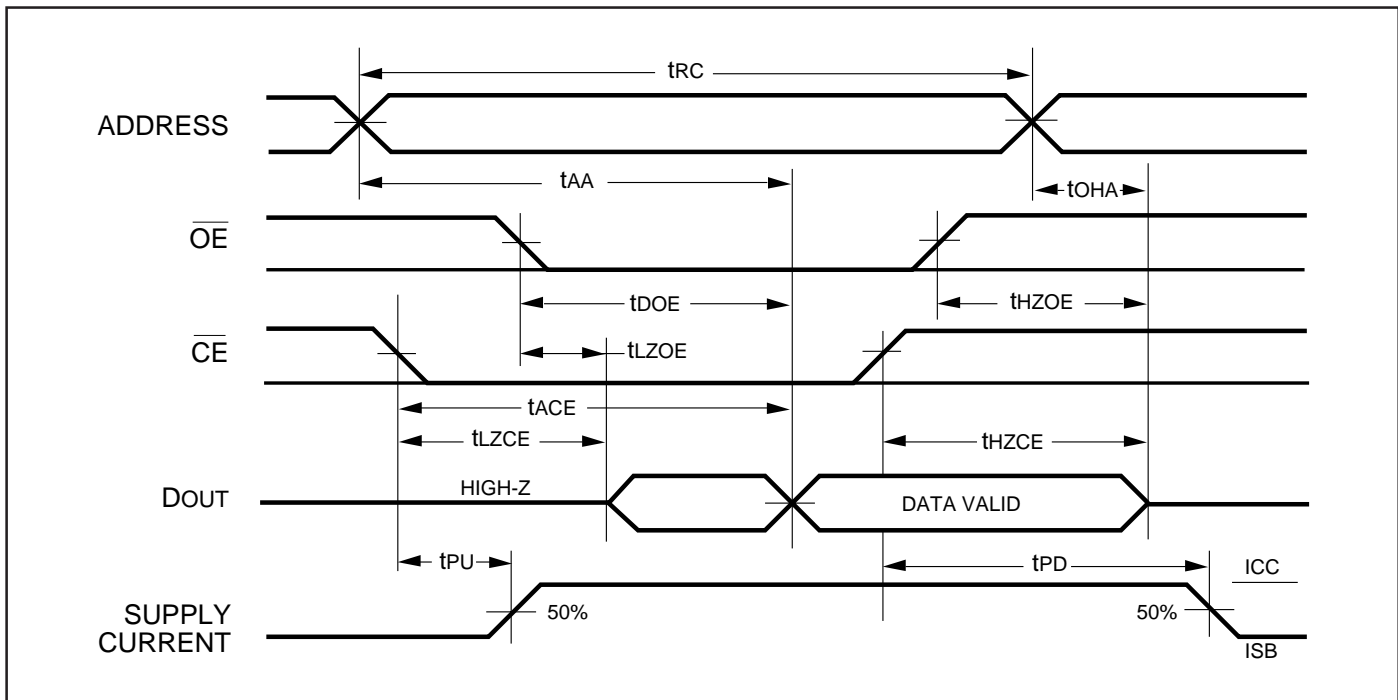
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>



READ CYCLE NO. 2<sup>(1,3)</sup>



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

**WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,3)</sup>** (Over Operating Range)

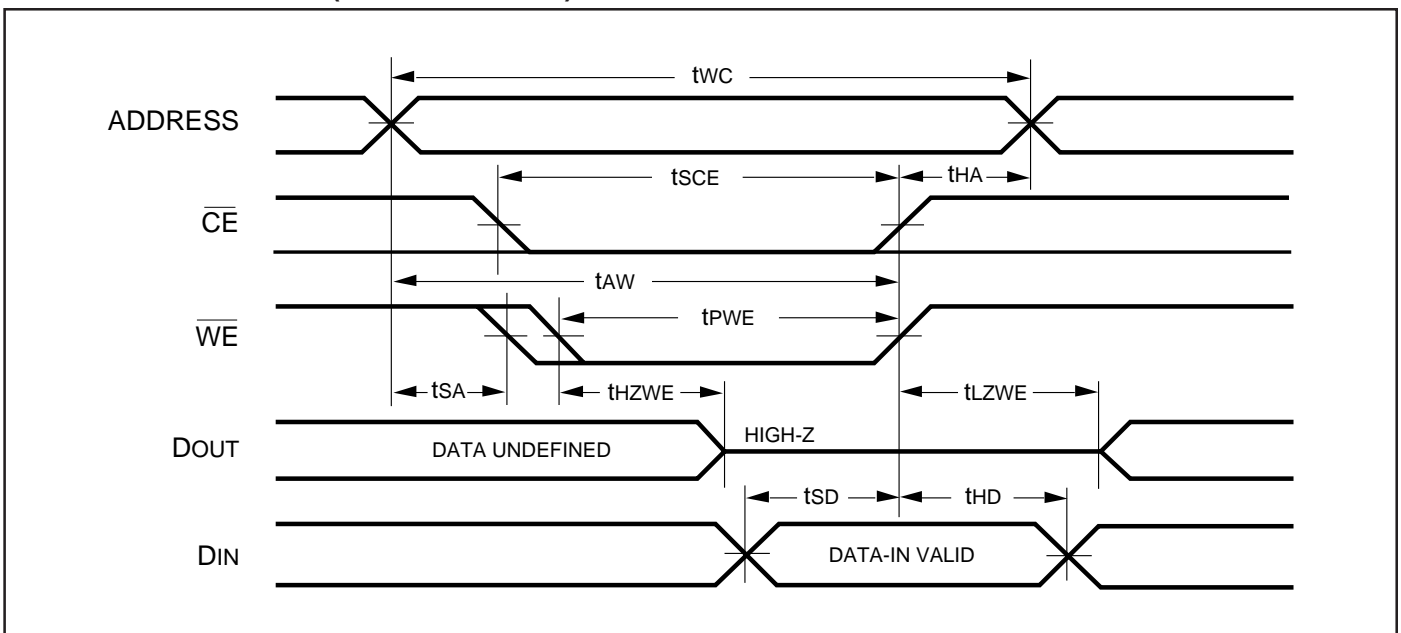
Symbol	Parameter	-15 ns		-20 ns		-25 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time	15	—	20	—	25	—	ns
t <sub>SCE</sub>	$\overline{CE}$ to Write End	10	—	13	—	15	—	ns
t <sub>AW</sub>	Address Setup Time to Write End	10	—	15	—	20	—	ns
t <sub>HA</sub>	Address Hold from Write End	0	—	0	—	0	—	ns
t <sub>SA</sub>	Address Setup Time	0	—	0	—	0	—	ns
t <sub>PWE<sup>(4)</sup></sub>	$\overline{WE}$ Pulse Width	10	—	13	—	15	—	ns
t <sub>SD</sub>	Data Setup to Write End	8	—	10	—	12	—	ns
t <sub>HD</sub>	Data Hold from Write End	0	—	0	—	0	—	ns
t <sub>HZWE<sup>(2)</sup></sub>	$\overline{WE}$ LOW to High-Z Output	—	7	—	8	—	10	ns
t <sub>LZWE<sup>(2)</sup></sub>	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	0	—	ns

**Notes:**

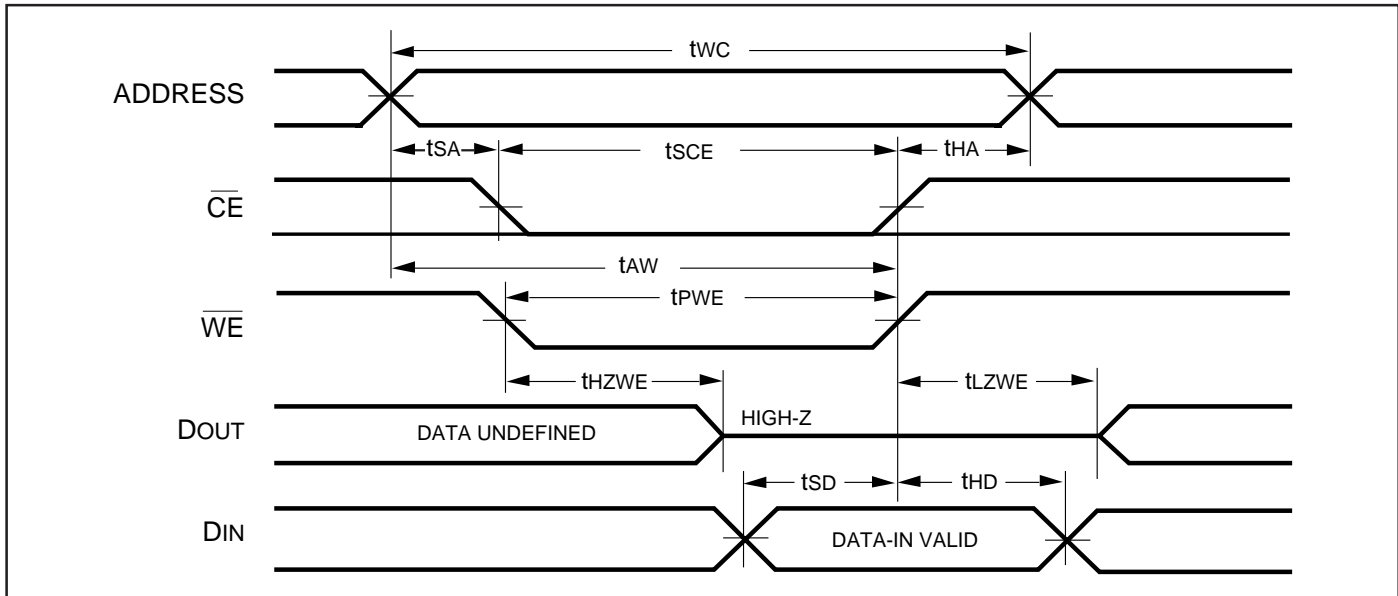
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
4. Tested with OE HIGH.

**AC WAVEFORMS**

**WRITE CYCLE NO. 1 ( $\overline{WE}$  Controlled)<sup>(1,2)</sup>**



**WRITE CYCLE NO. 2 ( $\overline{CE}$  Controlled)<sup>(1,2)</sup>**



**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .

**ORDERING INFORMATION**

**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
15	IC62LV256L-15T	8*13.4mm TSOP-1
	IC62LV256L-15J	300mil SOJ
20	IC62LV256L-20T	8*13.4mm TSOP-1
	IC62LV256L-20J	300mil SOJ
25	IC62LV256L-25T	8*13.4mm TSOP-1
	IC62LV256L-25J	300mil SOJ

**ORDERING INFORMATION**

**Industrial Range: -40°C to +85°C**

Speed (ns)	Order Part No.	Package
15	IC62LV256L-15TI	8*13.4mm TSOP-1
	IC62LV256L-15JI	300mil SOJ
20	IC62LV256L-20TI	8*13.4mm TSOP-1
	IC62LV256L-20JI	300mil SOJ
25	IC62LV256L-25TI	8*13.4mm TSOP-1
	IC62LV256L-25JI	300mil SOJ





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