



Pentium/Pro™ System Clock Chip

General Description

The ICS9148-18 is a Clock Synthesizer chip for Pentium and PentiumPro CPU based Desktop/Notebook systems that will provide all necessary clock timing.

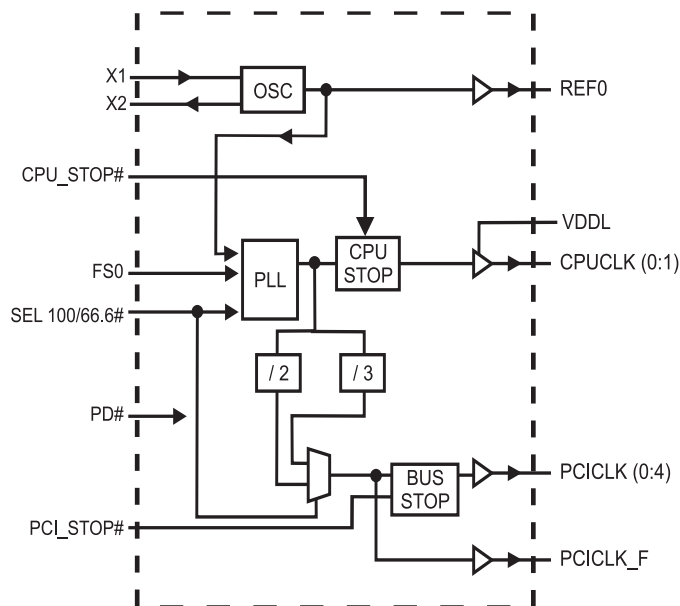
Features include two CPU and six PCI clocks. One reference output is available equal to the crystal frequency. Additionally, the device meets the Pentium power-up stabilization requirement, achieving stable CPU and PCI clocks 2ms after power-up.

PD# pin can enable a low power mode by stopping crystal OSC and PLL stages. Other power management features include, CPU_STOP# which stops CPU (0:1) clocks, and PCI_STOP# which stops PCICLK (0:4) clocks.

High drive CPUCLK outputs typically provide greater than 1 V/ns slew rate into 20pF loads. PCICLK outputs typically provide better than 1V/ns slew rate into 30pF loads while maintaining 50±5% duty cycle. The REF clock output typically provides better than 0.5V/ns slew rates.

The ICS9148-18 accepts a 14.318MHz reference crystal or clock as its input and runs on a 3.3V core supply.

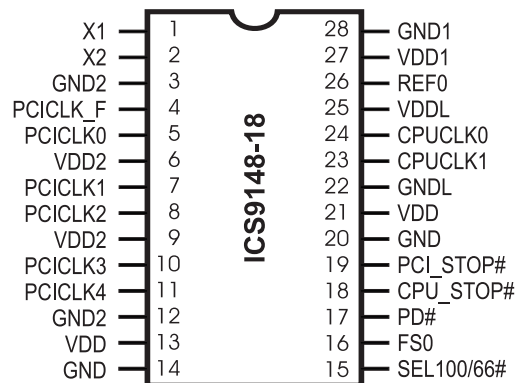
Block Diagram



Features

- Generates system clocks for CPU, PCI, plus 14.314 MHz REF0.
- Supports single or dual processor systems
- Skew from CPU (earlier) to PCI clock (rising edges for 100/33.3MHz) 1 to 4ns
- Separate 2.5V and 3.3V supply pins
- 2.5V or 3.3V output: CPU
- 3.3V outputs: PCI, REF
- No power supply sequence requirements
- Uses external 14.318MHz crystal, no external load cap required for C_L=18pF crystal
- 28 pin 209 mil SSOP

Pin Configuration



28 pin SSOP

Power Groups

VDD = Supply for PLL core
 VDD1 = REF0, X1, X2
 VDD2 = PCICLK_F, PCICLK (0:4)
 VDDL = CPUCLK (0:1)

Ground Groups

GND = Ground Source Core
 GND1 = REF0, X1, X2
 GND2 = PCICLK_F, PCICLK (0:4)
 GNDL = CPUCLK (0:1)

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Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|-----------------|--------------|------|---|
| 26 | REF0 | OUT | 14.318MHz clock output |
| 28 | GND1 | PWR | Ground for REF outputs |
| 1 | X1 | IN | XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2 |
| 2 | X2 | OUT | XTAL_OUT Crystal output, has internal load cap 33pF |
| 3, 12 | GND2 | PWR | Ground for PCI outputs |
| 4 | PCICLK_F | OUT | Free Running PCI output |
| 5, 7, 8, 10, 11 | PCICLK (0:4) | OUT | PCI clock outputs. TTL compatible 3.3V |
| 6, 9 | VDD2 | PWR | Power for PCICLK outputs, nominally 3.3V |
| 13, 21 | VDD | PWR | Isolated power for core, nominally 3.3V |
| 14, 20 | GND | PWR | Isolated ground for core |
| 15 | SEL100/66.6# | IN | Select pin for enabling 100MHz or 66.6MHz H=100MHz, L=66.6MHz (PCI always synchronous 33.3MHz) |
| 16 | FS0 | IN | Frequency Select pin |
| 17 | PD# | IN | Powers down chip, active low |
| 18 | CPU_STOP# | IN | Halts CPU clocks at logic "0" level when low |
| 19 | PCI_STOP# | IN | Halts PCI Bus at logic "0" level when low |
| 25 | VDDL | PWR | Power for CPU outputs, nominally 2.5V |
| 22 | GNDL | PWR | Ground for CPU outputs. |
| 23, 24 | CPUCLK (1:0) | OUT | CPU and Host clock outputs @ 2.5V |
| 27 | VDD1 | PWR | Power for REF outputs. |

Select Functions

(Functionality determined by FS0 and SEL100/66# pin, see below)

| Functionality | CPUCLK | PCI, PCI_F | REF0 |
|---------------|---------------------|---------------------|-------------------|
| Tristate | HI - Z | HI - Z | HI - Z |
| Testmode | TCLK/2 ¹ | TCLK/6 ¹ | TCLK ¹ |

Notes:

1. TCLK is a test clock driven on the X1 (crystal in pin) input during test mode.

| SEL 100/66# | FS0 | Function |
|-------------|-----|------------------------------|
| 0 | 0 | Tri-State |
| 0 | - | (Reserved) |
| 0 | - | (Reserved) |
| 0 | 1 | Active 66.6MHz CPU, 33.3 PCI |
| 1 | 0 | Test Mode |
| 1 | - | (Reserved) |
| 1 | - | (Reserved) |
| 1 | 1 | Active 100MHz CPU, 33.3 PCI |



Technical Pin Function Descriptions

VDD(1,2)

This is the power supply to the internal core logic of the device as well as the clock output buffers for REF0, PCICLK (0:4), and PCICLK_F.

This pin operates at 3.3V volts. Clocks from the buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the clocks, please consult the DC parameter table in this data sheet.

VDDL

This is the power supply for the CPUCLK output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that this pin supplies will have a voltage swing from Ground to VDDL. For the actual guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this data sheet.

GND(1,2)

This is the power supply ground (common or negative) return pin for the internal core logic and all the PCI output buffers.

GNDL

This is the ground for CPUCLK output buffers.

X1

This input pin serves one of two functions. When the device is used with a crystal, X1 acts as the input pin for the reference signal that comes from the crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also has an internal Crystal loading capacitor that is connected to ground. With a nominal value of 33pF, no external load cap is needed for a $C_L=17$ to 18pF crystal.

X2

This Output pin is used only when the device uses a crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the crystal. The X2 pin also has an internal loading capacitor, nominally 33pF.

CPUCLK(0:1)

These output pins are the clock outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these clocks is controlled by the voltage level applied to the VDDL pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these clocks and the selection codes to produce them.

REF0

The REF Output is fixed frequency clock that runs at the same frequency as the Input Reference Clock or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F

This Output is equal to PCICLK(0:4) and is FREE RUNNING, and will not be stopped by PCI_STOP#.

PCICLK(0:4)

These output clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification.

SELECT 100/66.6MHz#

This input pin controls the frequency of the clocks at the CPU & PCICLK output pins. If a logic "1" value is present on this pin, the 100MHz clock is selected. If a logic "0" is used, the 66.6MHz frequency is selected. The PCI clock is multiplexed to run at 33.3MHz for both select cases. PCI is synchronous at the rising edge of PCI to the CPU rising edge (with the skew making CPU early).

PD#

This is an asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and Crystal are stopped. Power down will also place all the outputs in a low state at the end of their current cycle. The latency of power down will not be greater than 3ms.

CPU_STOP#

This is a synchronous active low input pin used to stop the CPUCLK clocks in an active low state. All other clocks will continue to run while this function is enabled. The CPUCLKs will have a turn ON latency of at least 3 CPU clocks.

PCI_STOP#

This is a synchronous active low input pin used to stop the PCICLK clocks in an active low state. It will not effect PCICLK_F nor any other outputs.



Power Management

Clock Enable Configuration

| CPU_STOP# | PCI_STOP# | PWR_DWN# | CPUCLK | PCICLK | REF | Crystal | VCOs |
|-----------|-----------|----------|-------------|----------|---------|---------|---------|
| X | X | 0 | Low | Low | Stopped | Off | Off |
| 0 | 0 | 1 | Low | Low | Running | Running | Running |
| 0 | 1 | 1 | Low | 33.3 MHz | Running | Running | Running |
| 1 | 0 | 1 | 100/66.6MHz | Low | Running | Running | Running |
| 1 | 1 | 1 | 100/66.6MHz | 33.3 MHz | Running | Running | Running |

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PD# pin will not cause clocks of a short or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

ICS9148-18 Power Management Requirements

| SIGNAL | SIGNAL STATE | Latency No. of rising edges of free running PCICLK |
|-----------|-----------------------------------|--|
| CPU_STOP# | 0 (Disabled) ² | 1 |
| | 1 (Enabled) ¹ | 1 |
| PCI_STOP# | 0 (Disabled) ² | 1 |
| | 1 (Enabled) ¹ | 1 |
| PD# | 1 (Normal Operation) ³ | 3ms |
| | 0 (Power Down) ⁴ | 2max |

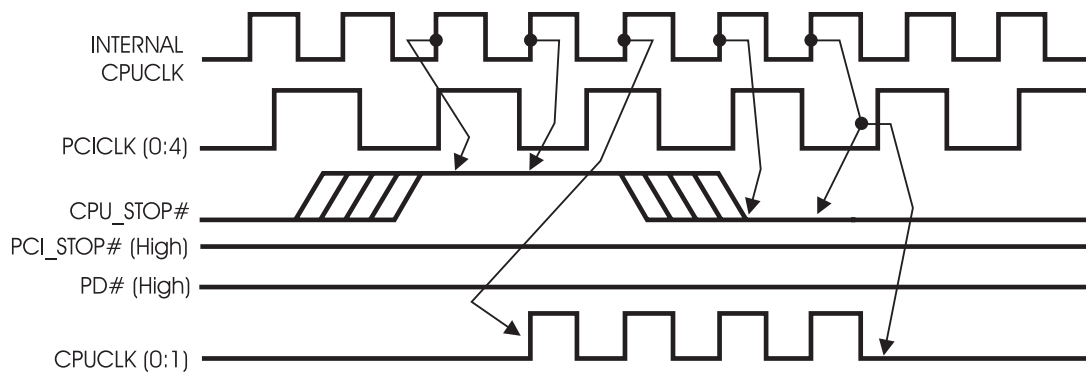
Notes.

1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, PCICLK only.
The REF and IOAPIC will be stopped independent of these.



CPU_STOP# Timing Diagram

CPUSTOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the ICS9148-18. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

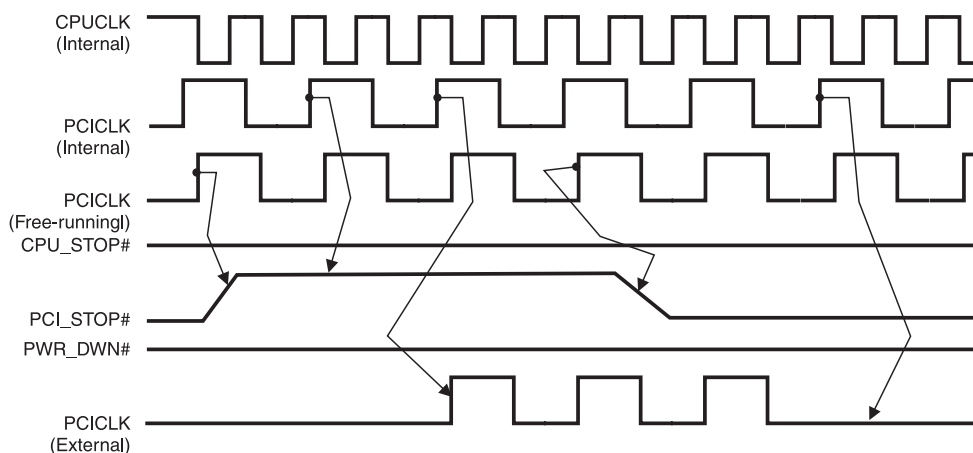


Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the ICS9148-18.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the ICS9148-18. It is used to turn off the PCICLK (0:4) clocks for low power operation. PCI_STOP# is synchronized by the ICS9148-18 internally. The minimum that the PCICLK (0:4) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:4) clocks. PCICLK (0:4) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:4) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



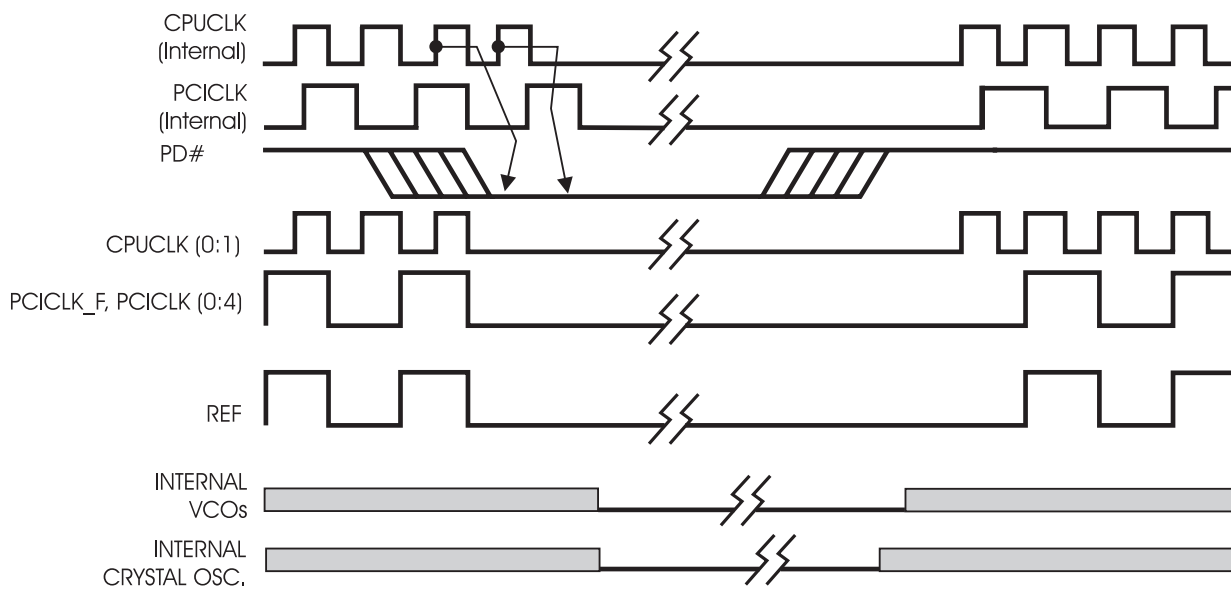
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.



PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internally by the ICS9148-18 prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the crystal oscillator. The power on latency is guaranteed to be less than 3ms. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9148.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.



Absolute Maximum Ratings

- Supply Voltage 7.0 V
- Logic Inputs GND–0.5 V to V_{DD}+0.5 V
- Ambient Operating Temperature 0°C to +70°C
- Storage Temperature –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | 2.0 | | μA |
| Operating Supply Current | I _{DD3.0(66)} | C _L = 0 pF; Select @ 66MHz | | 28 | 100 | mA |
| | I _{DD3.3(100)} | C _L = 0 pF; Select @ 100MHz | | 33 | 100 | |
| Power Down Supply Current | I _{DD3.3PD} | C _L = 0 pF | | 100 | 150 | μA |
| Input frequency | F _i | V _{DD} = 3.3 V; All outputs loaded | | 14.318 | | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | 36 | 45 | pF |
| Transition Time ¹ | T _{trans} | To 1st crossing of target Freq. | | | 3 | ms |
| Settling Time ¹ | T _s | From 1st crossing to 1% target Freq. | | 5 | | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target Freq. | | | 3 | ms |
| Skew ¹ | T _{CPU-PCI1} | V _T = 1.5 V; | 1.5 | 3 | 4 | ns |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|-------------------------|--|-----|-----|-----|-------|
| Operating Supply Current | I _{DD2.5(66)} | C _L = 0 pF; Select @ 66.8 MHz | | 3 | 25 | mA |
| | I _{DD2.5(100)} | C _L = 0 pF; Select @ 100 MHz | | 4 | 25 | mA |
| Power Down Supply Current | I _{DD2.5PD} | C _L = 0 pF | | | 100 | μA |
| Skew ¹ | t _{CPU-PCI2} | V _T = 1.5 V; V _{TL} = 1.25 V | 1.5 | 3 | 4 | ns |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPUCLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 10 - 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|---------------------------|---|------|-----|------|----------|
| Output Impedance | R_{DSP2B}^1 | $V_O = V_{DD}*(0.5)$ | 13.5 | | 45 | Ω |
| Output Impedance | R_{DSN2B}^1 | $V_O = V_{DD}*(0.5)$ | 13.5 | | 45 | Ω |
| Output High Voltage | V_{OH2B} | $I_{OH} = -12.0\text{ mA}$ | 2 | 2.3 | | V |
| Output Low Voltage | V_{OL2B} | $I_{OL} = 12\text{ mA}$ | | 0.2 | 0.4 | V |
| Output High Current | I_{OH2B} | $V_{OH} = 1.7\text{ V}$ | | -41 | -19 | mA |
| Output Low Current | I_{OL2B} | $V_{OL} = 0.7\text{ V}$ | 19 | 37 | | mA |
| Rise Time | t_{r2B}^1 | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.0\text{ V}$ | | 1.2 | 1.6 | ns |
| Fall Time | t_{f2B}^1 | $V_{OH} = 2.0\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | 1 | 1.6 | ns |
| Duty Cycle | d_{t2B}^1 | $V_T = 1.25\text{ V}$ | 45 | 50 | 55 | % |
| Skew | t_{sk2B}^1 | $V_T = 1.25\text{ V}$ | | 65 | 175 | ps |
| Jitter, Cycle-to-cycle | $t_{j\text{cyc-cyc}2B}^1$ | $V_T = 1.25\text{ V}$ | | 140 | 250 | ps |
| Jitter, One Sigma | t_{j1s2B}^1 | $V_T = 1.25\text{ V}$ | | 30 | 150 | ps |
| Jitter, Absolute | $t_{j\text{abs}2B}^1$ | $V_T = 1.25\text{ V}$ | -250 | 150 | +250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF0

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 3.3\text{ V} \pm 5\%$; $C_L = 10 - 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|--------------------|---|-----|------|-----|-------|
| Output Impedance ¹ | R_{DSP5} | $V_O = V_{DD}*(0.5)$ | 20 | | 60 | Ohm |
| Output Impedance ¹ | R_{DSN5} | $V_O = V_{DD}*(0.5)$ | 20 | | 60 | Ohm |
| Output High Voltage | V_{OH5} | $I_{OH} = -12\text{ mA}$ | 2.6 | 3.1 | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9\text{ mA}$ | | 0.17 | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0\text{ V}$ | | -44 | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8\text{ V}$ | 16 | 42 | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | | 0.9 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | 0.8 | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5\text{ V}$ | 45 | 53 | 55 | % |
| Jitter, One Sigma ¹ | t_{j1s5} | $V_T = 1.5\text{ V}$ | | 1 | 3 | % |
| Jitter, Absolute ¹ | $t_{j\text{abs}5}$ | $V_T = 1.5\text{ V}$ | | 3 | 5 | % |

¹Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - PCICLK** $T_A = 0 - 70^\circ\text{C}$; $V_{DD} = V_{DDL} = 3.3\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|--------------------|--|------|-----|-----|----------|
| Output Impedance ¹ | R _{DSP1} | $V_O = V_{DD} * (0.5)$ | 12 | | 55 | Ω |
| Output Impedance ¹ | R _{DSN1} | $V_O = V_{DD} * (0.5)$ | 12 | | 55 | Ω |
| Output High Voltage | V _{OH1} | I _{OH} = -11 mA | 2.6 | 3.1 | | V |
| Output Low Voltage | V _{OL1} | I _{OL} = 9.4 mA | | 0.1 | 0.4 | V |
| Output High Current | I _{OH1} | V _{OH} = 2.0 V | | -62 | -22 | mA |
| Output Low Current | I _{OL1} | V _{OL} = 0.8 V | 16 | 57 | | mA |
| Rise Time ¹ | t _{rl} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | | 1.1 | 2 | ns |
| Fall Time ¹ | t _{fl} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | | 1.3 | 2 | ns |
| Duty Cycle ¹ | d _{t1} | V _T = 1.5 V | 45 | 50 | 55 | % |
| Skew ¹ | t _{sk1} | V _T = 1.5 V | | 175 | 500 | ps |
| Jitter, One Sigma ¹ | t _{j1s1} | V _T = 1.5 V | | 13 | 150 | ps |
| Jitter, Absolute ¹ | t _{jabs1} | V _T = 1.5 V | -250 | 120 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.

ICS9148-18

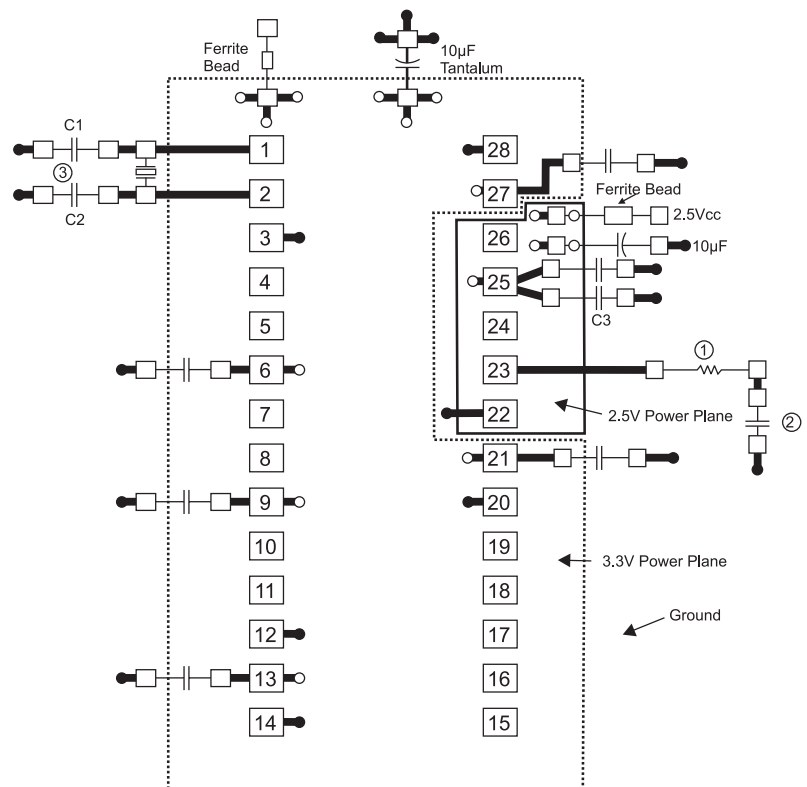


General Layout Precautions:

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

- 1 All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram
- 2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
- 3 Optional crystal load capacitors are recommended.



- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads

Capacitor Values:

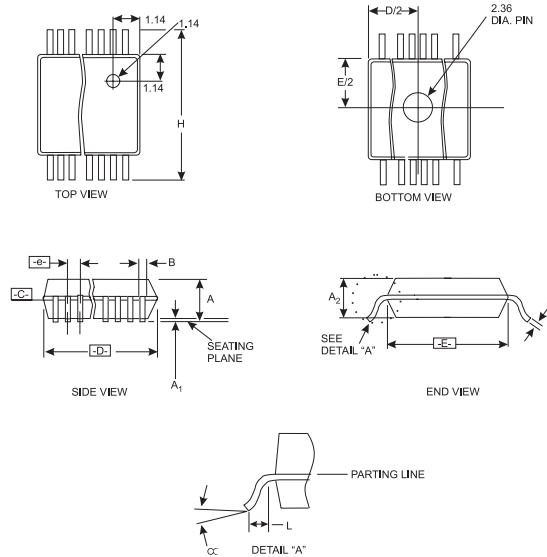
C1, C2 : Crystal load values determined by user

C3 : 100pF ceramic

All unmarked capacitors are 0.01µF ceramic



ICS9148-18



| SYMBOL | COMMON DIMENSIONS | | | VARIATIONS | D | | |
|--------|-------------------|------------|-------|----------------------|-------|-------|-------|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. |
| A | 0.068 | 0.073 | 0.078 | 14 | 0.239 | 0.244 | 0.249 |
| A1 | 0.002 | 0.005 | 0.008 | 16 | 0.239 | 0.244 | 0.249 |
| A2 | 0.066 | 0.068 | 0.070 | 20 | 0.278 | 0.284 | 0.289 |
| b | 0.010 | 0.012 | 0.015 | 24 | 0.318 | 0.323 | 0.328 |
| c | 0.004 | 0.006 | 0.008 | 28 | 0.397 | 0.402 | 0.407 |
| D | See Variations | | | 30 | 0.397 | 0.402 | 0.407 |
| E | 0.205 | 0.209 | 0.212 | Dimensions in inches | | | |
| e | | 0.0256 BSC | | | | | |
| H | 0.301 | 0.307 | 0.311 | | | | |
| L | 0.025 | 0.030 | 0.037 | | | | |
| N | See Variations | | | | | | |
| ∞ | 0° | 4° | 8° | | | | |

Ordering Information

ICS9148F-18

Example:

ICS XXXX F - PPP

