Integrated Circuit Systems, Inc.

ICS9150-01

Pentium Pro™ and SDRAM Frequency Generator

General Description

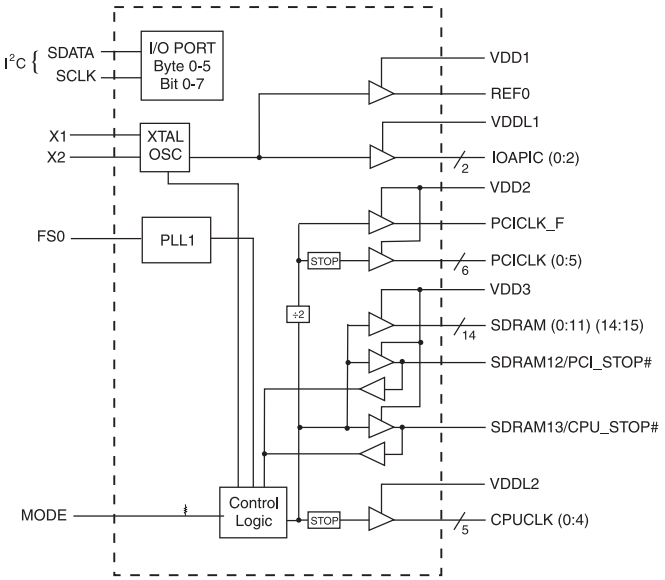
The **ICS9150-01** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro. Two different reference frequency multiplying factors are externally selectable with smooth frequency transitions. An output enable is provided for testability.

High drive PCICLK and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30 pF loads. CPUCLK outputs typically provide better than 1V/ns slew rate into 20 pF loads while maintaining 50 ±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

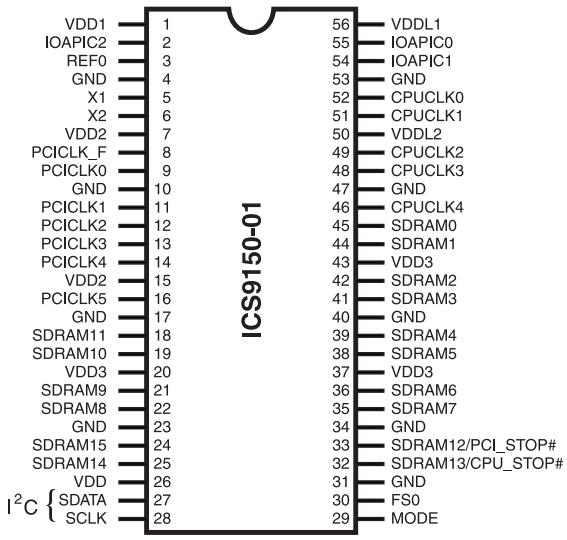
Features

- Generates five processor, six bus, one 14.31818MHz and 16 SDRAM clocks.
- Synchronous clocks skew matched to 250 ps window on PCLKs and 500ps window on BCLKs
- Test clock mode eases system design
- Selectable multiplying ratios
- Custom configurations available
- Output frequency ranges to 100 MHz (depending on option)
- 3.0V – 3.7V supply range
- PC serial configuration interface
- Power Management Control Input pins
- 56-pin SSOP package

Block Diagram



Pin Configuration



56-Pin SSOP

Functionality

FS0	CPUCLK, SDRAM (MHz)	X1, REF (MHz)	PCICLK (MHz)
0	60.0	14.318	30
1	66.6	14.318	33.3

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
3	REF0	OUT	14.318 MHz reference clock outputs.
4, 10, 17, 23, 31, 34, 40, 47, 53	GND	PWR	Ground.
5	X1	IN	14.318MHz input. Has internal load cap.
6	X2	OUT	Crystal output. Has internal load cap and feedback resistor to X1
29	MODE	IN	Mode select pin for enabling power management features, has pullup.
8	PCICLK_F	OUT	Free running BUS clock during PCI_STOP#=0.
9, 11, 12, 13 14, 16	PCICLK (0:5)	OUT	BUS clock outputs.
30	FS0	IN	Select pin for enabling 66.6 MHz or 60 MHz. CPU/SDRAM clock frequency
27	SDATA	IN	Serial data in for serial config port.
28	SCLK	IN	Clock input for serial config port.
1, 7, 15, 20, 26, 37, 43	VDD2, VDD1, VDD, VDD3	PWR	Nominal 3.3V power supply, see power groups for function.
50, 56	VDDL2, VDDL1	PWR	CPU and IOAPIC clock buffer power supply, either 2.5 or 3.3V nominal.
18, 19, 21, 22, 24, 25, 32, 33, 35, 36, 38, 39, 41, 42, 44, 45	SDRAM (0:11) (14:15)	OUT	SDRAM clocks (60/66.6MHz)
2, 54, 55	IOAPIC (0:2)	OUT	IOAPIC clock output. (14.31818 MHz) Poweredby VDDL1
46, 48, 49, 51, 52	CPUCLK (0:4)	OUT	CPU Output clocks. Powered by VDDL2 (60 or 66.6MHz)
32	SDRAM13	OUT	SDRAM clock (60/66.6 MHz)
	CPU_STOP#	IN	Halts CPUCLK clocks at logic "0" level when low.
33	SDRAM12	OUT	SDRAM clock (60/66.6 MHz)
	PCI_STOP#	IN	Halts PCICLK (0:5) at logic "0" level when low.

Power Groups

VDD = Supply for PLL core
VDD1 = REF 0, X1, X2
VDD2 = PCICLK_F, PCICLK (0:5)
VDD3 = SDRAM (0:11) (14:15), SDRAM13/CPU_STOP#, SDRAM12/PCI_STOP#
VDDL1 = IOAPIC (0:2)
VDDL2 = CPUCLK (0:4)

Power-On Conditions

SEL 66/60#	MODE	PIN #	DESCRIPTION	FUNCTION
1	1	52, 51, 49, 48, 46	CPUCLKs	66.6 MHz - w/serial config enable/disable
		45, 44, 42, 41, 39, 38, 36, 35, 22, 21, 19, 18, 33, 32, 25, 24	SDRAM	66.6 MHz - All SDRAM outputs
		9, 11, 12, 13, 14, 16, 8	PCICLKs	33.3 MHz - w/serial config enable/disable
0	1	52, 51, 49, 48, 46	CPUCLKs	60 MHz - w/serial config enable/disable
		45, 44, 42, 41, 39, 38, 36, 35, 22, 21, 19, 18, 33, 32, 25, 24	SDRAM	60 MHz - w/serial config enable/disable
		9, 11, 12, 13, 14, 16, 8	PCICLKs	30 MHz - w/serial config enable/disable
1	0	52, 51, 49, 48, 46	CPUCLKs	66.6 MHz - w/serial config enable/disable
		45, 44, 42, 41, 39, 38, 36, 35, 22, 21, 19, 18, 25, 24	SDRAM	66.6 MHz - All SDRAM outputs
		33	PCI_STOP#	Power Management, PCI (0:5) clocks stopped when low
		32	CPU_STOP#	Power Managemen, CPU clocks stopped when low
0	0	52, 51, 49, 48, 46	CPUCLKs	60 MHz - w/serial config enable/disable
		45, 44, 42, 41, 39, 38, 36, 35, 22, 21, 19, 18, 25, 24	SDRAM	60 MHz - w/serial config enable/disable
		33	PCI_STOP#	Power Management, PCI (0:5) clocks stopped when low
		32	CPU_STOP#	Power Managemen, CPU clocks stopped when low

Example:
a) if MODE = 1, pins 33 and 32 are configured as SDRAM12, and SDRAM13 respectively.
b) if MODE = 0, pins 33 and 32 are configured as PCI_STOP#, and CPU_STOP# respectively.

Power-On Default Conditions

At power-up and before device programming, all clocks will default to an enabled and “on” condition. The frequencies that are then produced are on the FS and MODE pin as shown in the table below.

CLOCK	DEFAULT CONDITION AT POWER-UP
REF 0	14.31818 MHz
IOAPIC (0:2)	14.31818 MHz

Technical Pin Function Descriptions

VDD(1,2,3)
This is the power supply to the internal core logic of the device as well as the clock output buffers for REF(0:1), PCICLK, and SDRAM(0:7).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

VDDL1,2
This is the power supplies for the CPUCLK and IOAPCI output buffers. The voltage level for these outputs may be 2.5 or 3.3volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet.

GND
This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

X1
This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. See the data tables for the value of this capacitor.

X2
This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor that is connected to ground. See the Data Sheet for the value of this capacitor.

CPUCLK (0:4)
These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks are controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them.

SDRAM(0:15)
These Output Clocks are use to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the SDRAM's output is controlled by the supply voltage that is applied to VDD3 of the device, operates at 3.3 volts.

IOAPIC (0:2)
These Outputs are fixed frequency Output Clocks that run at the Reference Input (typically 14.31818MHz) . Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3volts.

REF0
The REF Output is a fixed frequency Clock that runs at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F
This Output is equal to PCICLK(0:5) and is FREE RUNNING, and will not be stopped by PCI_STP#.

PCICLK (0:5)
These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 1/2 CPU frequency.

FS0
This Input pin controls the frequency of the Clocks at the CPU, PCICLK and SDRAM output pins. If a logic "1" value is present on this pin, the 66.6 MHz Clock will be selected. If a logic "0" is used, the 60MHz frequency will be selected. (This is the Power Management Mode)

MODE
This Input pin is used to select the Input function of the I/O pins. An active Low will place the I/O pins in the Input mode and enable those stop clock functions. (This is the Power Management Mode)

CPU_STOP#
This is a synchronous active Low Input pin used to stop the CPUCLK clocks in an active low state. All other Clocks including SDRAM clocks will continue to run while this function is enabled. The CPUCLK's will have a turn ON latency of at least 3 CPU clocks. This input pin only valid when MODE=0 (Power Management Mode)

PCI_STOP#
This is a synchronous active Low Input pin used to stop the PCICLK clocks in an active low state. It will not effect PCICLK_F nor any other outputs. This input pin only valid when MODE=0 (Power Management Mode)

I^2C
The SDATA and SCLOCK Inputs are use to program the device. The clock generator is a slave-receiver device in the I^2C protocol. It will allow read-back of the registers. See configuration map for register functions. The I^2C specification in Philips I^2C Peripherals Data Handbook (1996) should be followed.

General I²C serial interface information

A. For the clock generator to be addressed by an I²C controller, the following address must be sent as a start sequence, with an acknowledge bit between each byte.

Clock Generator Address (7 bits)	ACK	+ 8 bits dummy command code	ACK	+ 8 bits dummy Byte count	ACK
A(6:0) & R/W#					
D2(H)					

Then Byte 0, 1, 2, etc in sequence until STOP.

B. The clock generator is a slave/receiver I²C component. It can "read back "(in Philips I²C protocol) the data stored in the latches for verification. (set R/W# to 1 above). There is no BYTE count supported, so it does not meet the Intel SMB PIIX4 protocol.

Clock Generator Address (7 bits)	ACK	Byte 0	ACK	Byte 1	ACK
A(6:0) & R/W#					
D3(H)					

Byte 0, 1, 2, etc in sequence until STOP.

C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)

D. The input is operating at 3.3V logic levels.

E. The data byte format is 8 bit bytes.

F. To simplify the clock generator I²C interface, the protocol is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.

G In the power down mode (PWR_DWN# Low), the SDATA and SCLK pins are tristated and the internal data latches maintain all prior programming information.

H. At power-on, all registers are set to a default condition. See Byte 0 detail for default condition, Bytes 1 through 5 default to a 1 (Enabled output state)

Serial Configuration Command Bitmaps

Byte 0: Functional and Frequency Select Clock Register (default = 0)

BIT	PIN#	DESCRIPTION	PWD
Bit 7	-	Reserved	0
Bit 6	-	Must be 0 for normal operation	0
Bit 5	-	Must be 0 for normal operation	0
	-	In Spread Spectrum, Controls type (0=centered, 1=down spread)	
Bit 4	-	Must be 0 for normal operation	0
	-	In Spread Spectrum, Controls Controls Spreading % (0=1.8%, 1=0.6%)	
Bit 3	-	Reserved	0
Bit 2	-	Reserved	0
Bit 1 Bit 0	-	Bit1 Bit0 1 1 - Tri-State 1 0 - Spread Spectrum Enable 0 1 - Testmode 0 0 - Normal operation	0 0

Note: PWD = Power-Up Default

I²C is a trademark of Philips Corporation

Select Functions

FUNCTION DESCRIPTION	OUTPUTS				
	CPU	PCI, PCI_F	SDRAM	REF	IOAPIC
Tri - State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2[1]	TCLK/4[1]	TCLK/2[1]	TCLK[1]	TCLK[1]

Notes:
1. REF is a test clock on the X1 inputs during test mode.

Byte 1: CPU Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	46	1	CPUCLK4 (Act/Inact)
Bit 3	48	1	CPUCLK3 (Act/Inact)
Bit 2	49	1	CPUCLK2 (Act/Inact)
Bit 1	51	1	CPUCLK1 (Act/Inact)
Bit 0	52	1	CPUCLK0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 2: PCICLK Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	8	1	PCICLK_F (Act/Inact)
Bit 5	16	1	PCICLK5 (Act/Inact)
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	13	1	PCICLK3 (Act/Inact)
Bit 2	12	1	PCICLK2 (Act/Inact)
Bit 1	11	1	PCICLK1 (Act/Inact)
Bit 0	9	1	PCICLK0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 3: SDRAM Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	35	1	SDRAM7 (Act/Inact)
Bit 6	36	1	SDRAM6 (Act/Inact)
Bit 5	38	1	SDRAM5 (Act/Inact)
Bit 4	39	1	SDRAM4 (Act/Inact)
Bit 3	41	1	SDRAM3 (Act/Inact)
Bit 2	42	1	SDRAM2 (Act/Inact)
Bit 1	44	1	SDRAM1 (Act/Inact)
Bit 0	45	1	SDRAM0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4: SDRAM Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	24	1	SDRAM15 (Act/Inact)
Bit 6	25	1	SDRAM14 (Act/Inact)
Bit 5	32	1	SDRAM13 (Act/Inact) Desktop Only
Bit 4	33	1	SDRAM12 (Act/Inact) Desktop Only
Bit 3	18	1	SDRAM11 (Act/Inact)
Bit 2	19	1	SDRAM10 (Act/Inact)
Bit 1	21	1	SDRAM9 (Act/Inact)
Bit 0	22	1	SDRAM8 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 5: Peripheral Clock Register

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	2	1	IOAPIC2 (Act/Inact)
Bit 5	54	1	IOAPIC1 (Act/Inact)
Bit 4	55	1	IOAPIC0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	3	1	REF0 (Act/Inact)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 6: Optional Register for Future

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes:
1. Byte 6 is reserved by Integrated Circuit Systems for future applications.

Power Management

Clock Enable Configuration

CPU_STOP#	PCI_STOP#	CPUCLK	PCICLK	Other Clocks, SDRAM, REF, IOAPICs	Crystal	VCOs
0	0	Low	Low	Running	Running	Running
0	1	Low	33.3/30 MHz	Running	Running	Running
1	0	66.6/60 MHz	Low	Running	Running	Running
1	1	66.6/60 MHz	33.3/30 MHz	Running	Running	Running

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

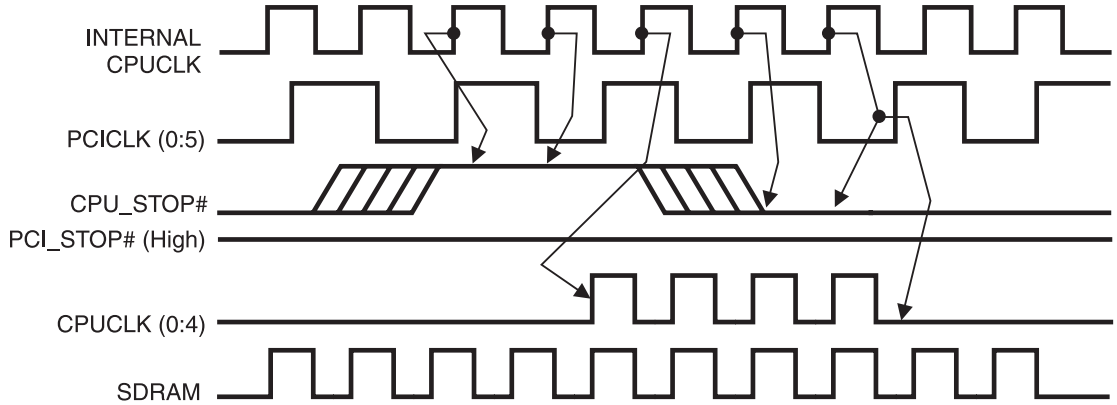
ICS9150-01 Power Management Requirements

SIGNAL	SIGNAL STATE	Latency No. of rising edges of free running PCICLK
CPU_ STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PCI_STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1

Notes.
1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.

CPU_STOP# Timing Diagram

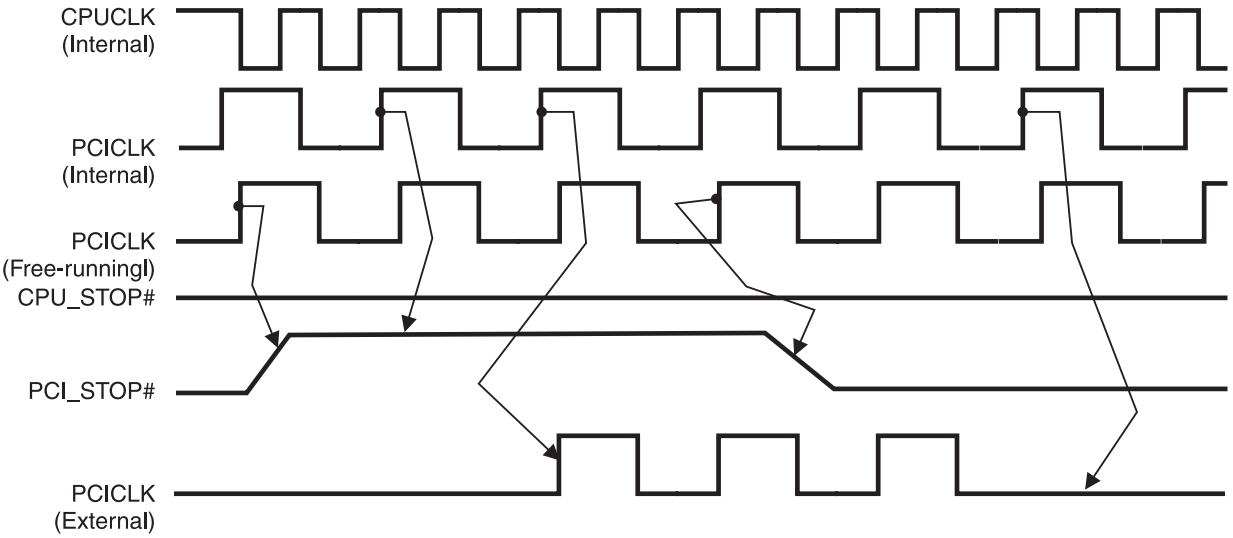
CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9150-01**. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9150-01.**
3. All other clocks continue to run undisturbed.
4. PCI_STOP# is shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9150-01**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9150-01** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9150 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9150.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage $V_{DD} = V_{DDL}$ = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M		75	95	mA
Outputs Disabled Supply Current	$I_{DD3.3OE}$	C_L = 0 pF; With input address to Vdd or GND		18	25	mA
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.		5		ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.		5	3	ms
Skew[1]	$T_{CPU-SDRAM2}$	V_T = 1.5 V		200	500	ps
	$T_{CPU-PCI2}$	V_T = 1.5 V	1	2	4	ns
	$T_{REF-IOAPIC}$	V_T = 1.5 V		900		ps

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP}$	C_L = 0 pF; Select @ 66M	6	8	9.5	mA
Skew[1]	$T_{CPU-SDRAM2}$	V_T = 1.5 V; V_{TL} = 1.25 V; SDRAM Leads		250	500	ps
	$T_{CPU-PCI2}$	V_T = 1.5 V; V_{TL} = 1.25 V; CPU Leads	1	2	4	ns
	$T_{REF-IOAPIC}$	V_T = 1.5 V; V_{TL} = 1.25 V; CPU Leads		860		ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	15		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	15		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.6		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.3	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-25	-16	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	26		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.7	2	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.5	2	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		60	250	ps
Jitter	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		150	250	ps
	t_{j1s2B}[1]	V_T = 1.25 V		30	150	ps
	t_{jabs2B}[1]	V_T = 1.25 V	-250	80	+250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	10		30	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	10		30	Ω
Output High Voltage	$V_{OH4\B}$	I_{OH} = -18 mA	2	2.4		V
Output Low Voltage	V_{OL4B}	I_{OL} = 18 mA		0.45	0.5	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-25	-16	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19	26		mA
Rise Time	t_{r4B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.4	1.6	ns
Fall Time	t_{f4B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.2	1.6	ns
Duty Cycle	d_{t4B}[1]	V_T = 1.25 V	40	54	60	%
Jitter	$t_{jcyc-cyc4B}$[1]	V_T = 1.25 V		1400		ps
	t_{j1s4B}[1]	V_T = 1.25 V		300	400	ps
	t_{jabs4B}[1]	V_T = 1.25 V	-1000	800	1000	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - REF0

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 45 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP7}	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output Impedance	R_{DSN7}	$V_O = V_{DD}*(0.5)$	10		24	Ω
Output High Voltage	V_{OH7}	I_{OH} = -30 mA	2.6	2.75		V
Output Low Voltage	V_{OL7}	I_{OL} = 23 mA		0.3	0.4	V
Output High Current	I_{OH7}	V_{OH} = 2.0 V		-62	-54	mA
Output Low Current	I_{OL7}	V_{OL} = 0.8 V	42	50		mA
Rise Time	T_{r7}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.9	2	ns
Fall Time	T_{f7}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		0.9	2	ns
Duty Cycle	D_{t7}[1]	V_T = 1.5 V	40	54	60	%
Jitter	$t_{jcyc-cyc7B}$[1]	V_T = 1.25 V		1400		ps
	t_{j1s7B}[1]	V_T = 1.25 V		350		ps
	t_{jabs7B}[1]	V_T = 1.25 V	-1000	900	1000	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	V_O = V_{DD}*(0.5)	12		55	Ω
Output Impedance	R_{DSN1}[1]	V_O = V_{DD}*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.6	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.15	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-65	-54	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	40	54		mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time	t_{fl}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		200	500	ps
Jitter	t_{j1s1}[1]	V_T = 1.5 V		10	150	ps
	t_{jabs1}[1]	V_T = 1.5 V	-250	65	250	ps

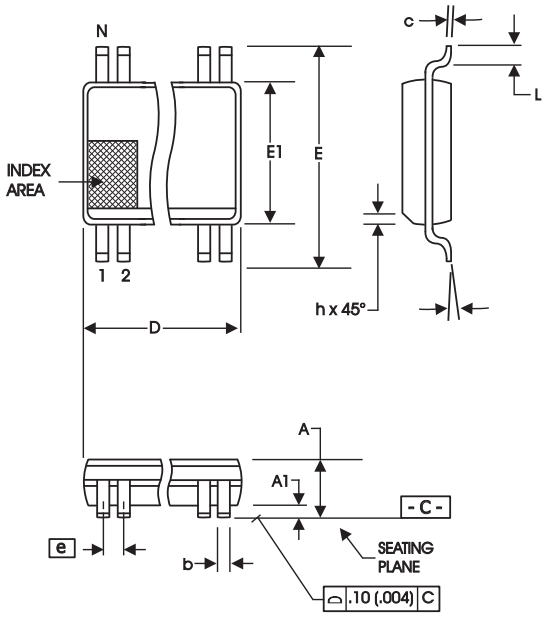
[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3}[1]	V_O = V_{DD}*(0.5)	10		24	Ω
Output Impedance	R_{DSN3}[1]	V_O = V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -30 mA	2.6	2.8		V
Output Low Voltage	V_{OL3}	I_{OL} = 23 mA		0.3	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-67	-54	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	40	55		mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.5	2	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.4	2	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45	50	55	%
Skew	T_{sk3}[1]	V_T = 1.5 V		200	500	ps
Jitter	T_{j1s3}[1]	V_T = 1.5 V		50	150	ps
	T_{jabs3}[1]	V_T = 1.5 V	-250	100	250	ps

[1]Guarenteed by design, not 100% tested in production.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9150F-01

Example:

ICS XXXX F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
F=SSOP

Device Type

Prefix
ICS, AV = Standard Device