



Frequency Timing Generator for Pentium II Systems

Recommended Application:

ALI1621/1632M style chipsets

Output Features:

- 2 - CPUs @2.5V, up to 140MHz.
- 7 - PCI @3.3V, (including one free running)
- 1 - 48MHz, @3.3V fixed.
- 2 - REF @3.3V, 14.318MHz.

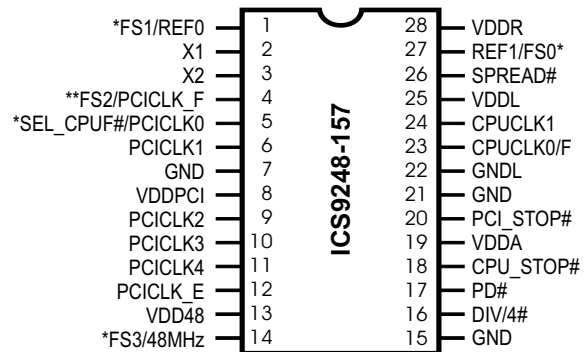
Features:

- Up to 140 MHz frequency support
- Support power management: CPU, PCI stop and Power down.
- Spread spectrum for EMI control (0.5% down spread).
- Uses external 14.318MHz crystal
- FS pins for frequency select

Key Specifications:

- CPU – CPU: <175ps
- PCI – PCI: <250ps
- CPU(early)-PCI: 1.5ns - 4ns
- PCI_E (early) - PCI: 2.1ns

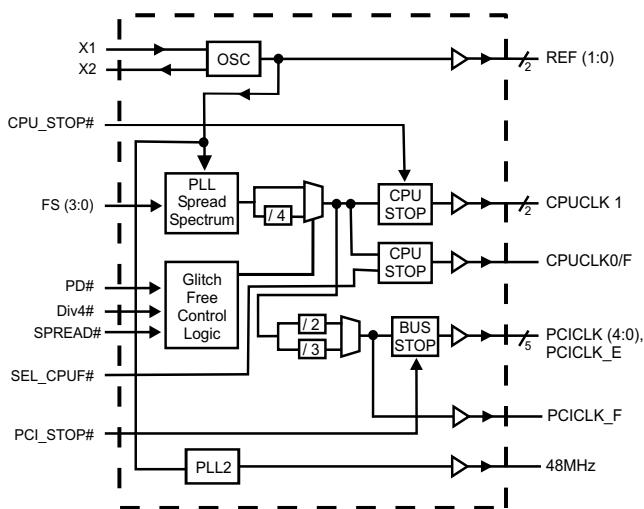
Pin Configuration



28 Pin 209mil SSOP

*These inputs have a 120K pull up to VDD
**These inputs have a 120K pull down to GND

Block Diagram



Functionality

| FS3 | FS2 | FS1 | FS0 | CPU | PCI |
|-----|-----|-----|-----|--------|-------|
| 0 | 0 | 0 | 0 | 33.33 | 16.66 |
| 0 | 0 | 0 | 1 | 63.33 | 31.66 |
| 0 | 0 | 1 | 0 | 69.99 | 35.00 |
| 0 | 0 | 1 | 1 | 66.66 | 33.33 |
| 0 | 1 | 0 | 0 | 97.00 | 32.33 |
| 0 | 1 | 1 | 0 | 91.50 | 30.50 |
| 0 | 1 | 1 | 1 | 83.33 | 27.77 |
| 1 | 0 | 0 | 0 | 50.00 | 16.66 |
| 1 | 0 | 0 | 1 | 95.25 | 31.75 |
| 1 | 0 | 1 | 0 | 105.00 | 35.00 |
| 1 | 0 | 1 | 1 | 100.00 | 33.33 |
| 1 | 1 | 0 | 0 | 66.66 | 16.66 |
| 1 | 1 | 0 | 1 | 126.35 | 31.66 |
| 1 | 1 | 1 | 0 | 139.65 | 35.00 |
| 1 | 1 | 1 | 1 | 133.33 | 33.33 |

ICS9248-157



General Description

The **ICS9248-157** is the Main clock solution for Notebook designs using the Intel ALI1621/1632M style chipset. Along with an SDRAM buffer such as the ICS9179-03, it provides all necessary clock signals for such a system.

Spread spectrum may be enabled by driving pin 26, **SPREAD#** active (Low) at power-on. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-157** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Pin Descriptions

| Pin number | Pin name | Type | Description |
|--------------|--------------|--------|---|
| 1 | FS1 | Input | Frequency select pin |
| | REF0 | Output | 3.3V, 14.318 MHz reference clock output. |
| 2 | X1 | Input | 14.318 MHz crystal input |
| 3 | X2 | Output | 14.318 MHz crystal output |
| 4 | FS2 | Input | Frequency select pin |
| | PCICLK_F | Output | 3.3 V free running PCI clock output, will not be stopped by the PCI_STOP# |
| 5 | SEL_CPUF# | Input | Active low input to select CPUCLK0/F (pin 23) either normal CPUCLK or Free running (not stoppable through CPU_STOP#) clock. |
| | PCICLK0 | Output | 3.3V PCI clock output |
| 11, 10, 9, 6 | PCICLK (4:1) | Output | 3.3 V PCI clock outputs, generating timing requirements |
| 7, 15, 21 | GND | Power | Ground for clock outputs |
| 8 | VDDPCI | Power | 3.3 V power for the PCI clock outputs |
| 12 | PCICLK_E | Output | Early PCICLK output, offset from other PCICLKs, stopped by PCI-STOP# |
| 13 | VDD48 | Power | 3.3 V power for 48 MHz clocks |
| 14 | FS3 | Input | Frequency select pin |
| | 48MHz | Output | Fixed 48MHz clock. |
| 16 | DIV4# | Input | Active low input, enables the CPUCLK and the PCICLK to run at 1/4 of the regular frequencies |
| 17 | PD# | Input | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 18 | CPU_STOP# | Input | Asynchronous active low input pin used to stop the CPUCLK in active low state, all other clocks will continue to run. The CPUCLK will have a "Turnon " latency of at least 3 CPU clocks. |
| 19 | VDDA | Power | 3.3 V power for the core |
| 20 | PCI-STOP# | Input | Synchronous active low input used to stop the PCICLK in active low state. It will not effect PCICLK_F or any other outputs. |
| 22 | GNDL | Power | Ground for the CPU and Host clock outputs |
| 23 | CPUCLK0/F | Output | 2.5V CPU clock output; can be selected to be free running by driving SEL_CPUF# low |
| 24 | CPUCLK1 | Output | 2.5 V CPU and Host clock outputs |
| 25 | VDDL | Power | 2.5 V power for the CPU and Host clock outputs |
| 26 | SPREAD# | Input | power-on spread spectrum enable option. Active low = spread spectrum clocking enable. Active high = spread spectrum clocking disable. |
| 27 | FS0 | Input | Frequency select pin |
| | REF1 | Output | 3.3V, 14.318 MHz reference clock output. |
| 28 | VDDR | Power | 3.3 V power for the REFCLK and crystal clock outputs |



Power Management

Clock Enable Configuration

| CPU_STOP# | PCI_STOP# | PWR_DWN# | CPUCLK | PCICLK | PCICLK_F | REF | Crystal | VCOs |
|-----------|-----------|----------|---------|---------|----------|---------|---------|---------|
| X | X | 0 | Low | Low | Low | Stopped | Off | Off |
| 0 | 0 | 1 | Low | Low | Running | Running | Running | Running |
| 0 | 1 | 1 | Low | Running | Running | Running | Running | Running |
| 1 | 0 | 1 | Running | Low | Running | Running | Running | Running |
| 1 | 1 | 1 | Running | Running | Running | Running | Running | Running |

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PD# pin will not cause clocks of a short or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

Power Management Requirements

| SIGNAL | SIGNAL STATE | Latency No. of rising edges of free running PCICLK |
|-----------|-----------------------------------|--|
| CPU_STOP# | 0 (Disabled) ² | 1 |
| | 1 (Enabled) ¹ | 1 |
| PCI_STOP# | 0 (Disabled) ² | 1 |
| | 1 (Enabled) ¹ | 1 |
| PD# | 1 (Normal Operation) ³ | 3ms |
| | 0 (Power Down) ⁴ | 2max |

Notes.

1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, PCICLK only.
The REF will be stopped independent of these.

Power Groups:

VDDA = PLL Core
VDD48 = 48MHz Core
VDDPCI = PCICLK
VDDL = CPUCLK
VDDR = Xtal & REF



Absolute Maximum Ratings

| | |
|-------------------------------|--------------------------------------|
| Supply Voltage | 5.5 V |
| Logic Inputs | GND -0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% VDDL = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | 2.0 | | μA |
| Input Low Current | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | -100 | | μA |
| Operating Supply Current | I _{DD3.3OP66} | C _L = 0 pF; Select @ 66MHz | | 60 | 180 | mA |
| | I _{DD3.3OP100} | C _L = 0 pF; Select @ 100MHz | | 66 | 180 | mA |
| Power Down Supply Current | I _{DD3.3PD} | C _L = 0 pF; With input address to Vdd or GND | | 70 | 600 | μA |
| Input frequency | F _i | V _{DD} = 3.3 V; | 11 | 14.318 | 16 | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | 36 | 45 | pF |
| Transition Time ¹ | T _{trans} | To 1st crossing of target Freq. | | | 3 | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target Freq. | | | 3 | ms |
| Skew ¹ | T _{CPU-PCI1} | V _T = 1.5 V; | 1.5 | 2.3 | 4 | ns |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|-------------------------|--|-----|-----|-----|-------|
| Operating Supply Current | I _{DD2.5OP66} | C _L = 0 pF; Select @ 66.8 MHz | | 16 | 72 | mA |
| | I _{DD2.5OP100} | C _L = 0 pF; Select @ 100 MHz | | 23 | 100 | mA |
| Skew ¹ | t _{CPU-PCI2} | V _T = 1.5 V; V _{TL} = 1.25 V | 1.5 | 3 | 4 | ns |

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Electrical Characteristics - CPUCLK

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-------------------------------------|--|------|------|------|-------|
| Output High Voltage | V _{OH2B} | I _{OH} = -12.0 mA | 2 | 2.3 | | V |
| Output Low Voltage | V _{OL2B} | I _{OL} = 12 mA | | 0.2 | 0.4 | V |
| Output High Current | I _{OH2B} | V _{OH} = 1.7 V | | -41 | -19 | mA |
| Output Low Current | I _{OL2B} | V _{OL} = 0.7 V | 19 | 37 | | mA |
| Rise Time | t _{r2B} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.0 V | | 0.99 | 1.6 | ns |
| Fall Time | t _{f2B} ¹ | V _{OH} = 2.0 V, V _{OL} = 0.4 V | | 1.05 | 1.6 | ns |
| Duty Cycle | d _{t2B} ¹ | V _T = 1.25 V | 45 | 50.3 | 55 | % |
| Skew | t _{sk2B} ¹ | V _T = 1.25 V | | 34 | 175 | ps |
| Jitter, Cycle-to-cycle | t _{jcc-cyc2B} ¹ | V _T = 1.25 V | | 203 | 250 | ps |
| Jitter, One Sigma | t _{j1s2B} ¹ | V _T = 1.25 V | | | 150 | ps |
| Jitter, Absolute | t _{jabs2B} ¹ | V _T = 1.25 V | -250 | | +250 | ps |

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Electrical Characteristics - PCICLK

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5% V_{DDL} = 2.5 V +/-5%; C_L = 30 pF

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-----------------------|--|------|-----|-----|-------|
| Output High Voltage | V _{OH1} | I _{OH} = -11 mA | 2.4 | 3.1 | | V |
| Output Low Voltage | V _{OL1} | I _{OL} = 9.4 mA | | 0.1 | 0.4 | V |
| Output High Current | I _{OH1} | V _{OH} = 2.0 V | | -62 | -22 | mA |
| Output Low Current | I _{OL1} | V _{OL} = 0.8 V | 16 | 57 | | mA |
| Rise Time ¹ | t _{r1} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | | 1.5 | 2 | ns |
| Fall Time ¹ | t _{f1} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | | 1.1 | 2 | ns |
| Duty Cycle ¹ | d _{t1} | V _T = 1.5 V | 45 | 50 | 55 | % |
| Skew ¹ | t _{sk1} | V _T = 1.5 V | | 290 | 500 | ps |
| Jitter, Cycle-to-cycle | t _{jcc-cyc1} | V _T = 1.25 V | | 200 | 500 | ps |
| Jitter, One Sigma ¹ | t _{j1s1} | V _T = 1.5 V | | | 150 | ps |
| Jitter, Absolute ¹ | t _{jabs1} | V _T = 1.5 V | -250 | | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - REF/48MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DDL} = 2.5\text{V} \pm 5\%$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 10 - 20\text{pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------|--|-----|------|-----|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -12\text{mA}$ | 2.6 | 3.1 | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9\text{mA}$ | | 0.17 | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0\text{V}$ | | -44 | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8\text{V}$ | 16 | 42 | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4\text{V}, V_{OH} = 2.4\text{V}$ | | 1.03 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4\text{V}, V_{OL} = 0.4\text{V}$ | | 0.9 | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5\text{V}$ | 45 | 52.9 | 55 | % |
| Jitter, One Sigma ¹ | t_{j1s5} | $V_T = 1.5\text{V}$ | | | 3 | % |
| Jitter, Absolute ¹ | t_{jabs5} | $V_T = 1.5\text{V}$ | | | 5 | % |

¹Guaranteed by design, not 100% tested in production.



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-157 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

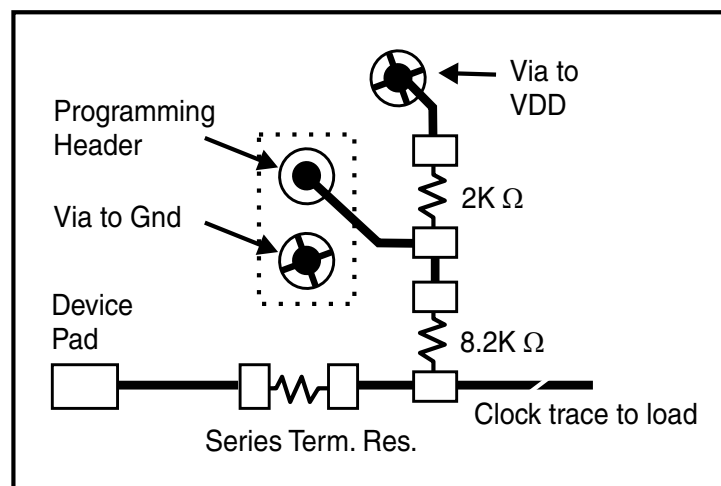
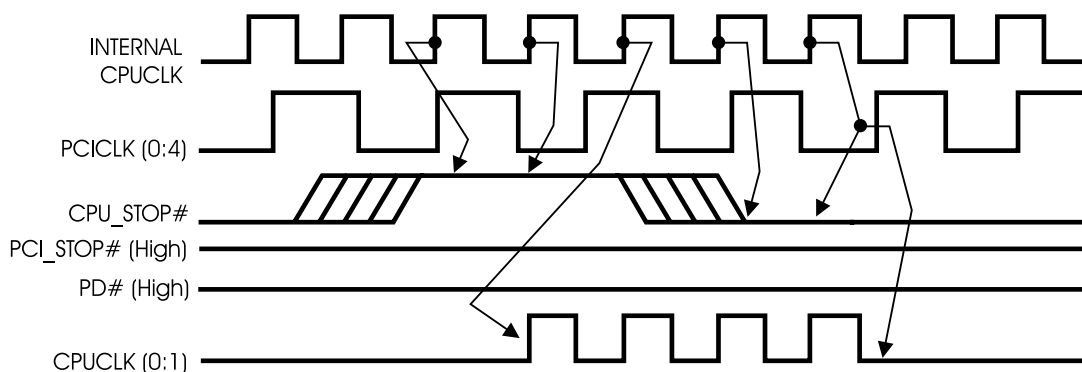


Fig. 1



CPU_STOP# Timing Diagram

CPUSTOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9248-157**. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



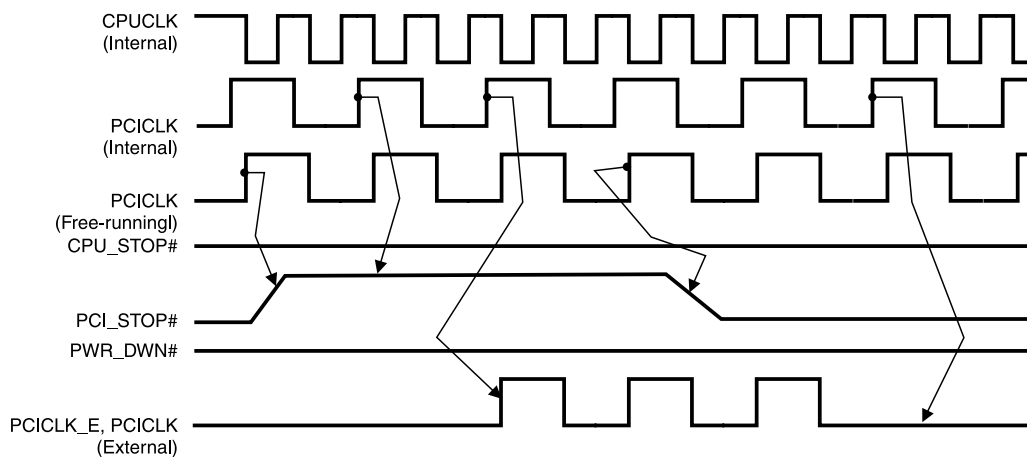
Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9248-157**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.



PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the ICS9248-157. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the ICS9248-157 internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



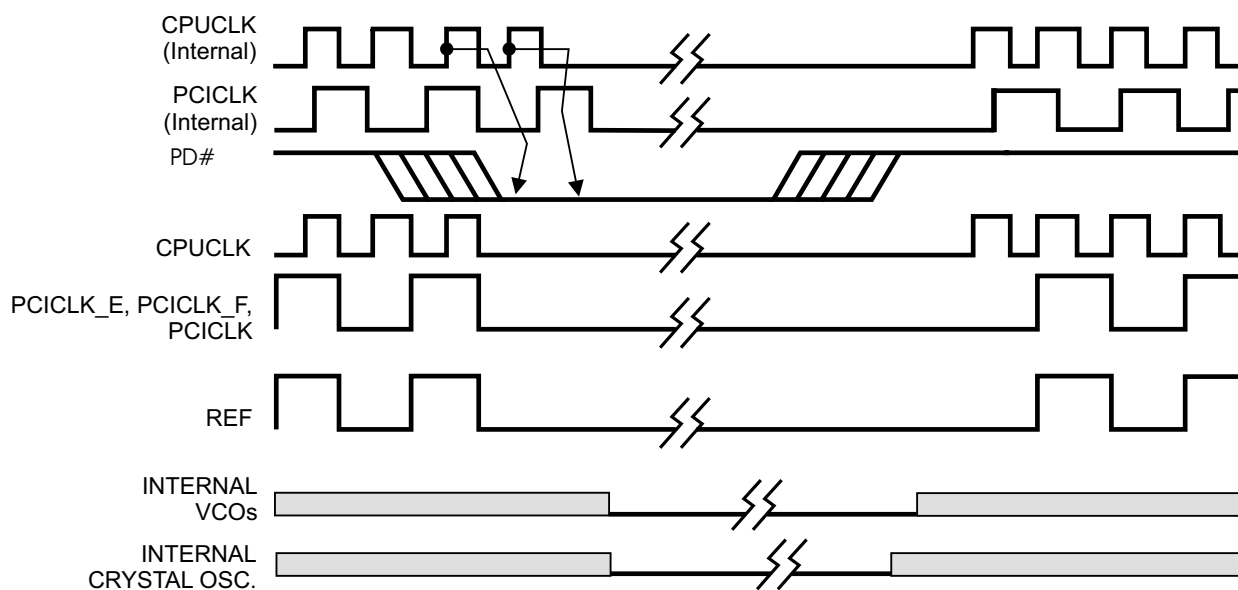
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.



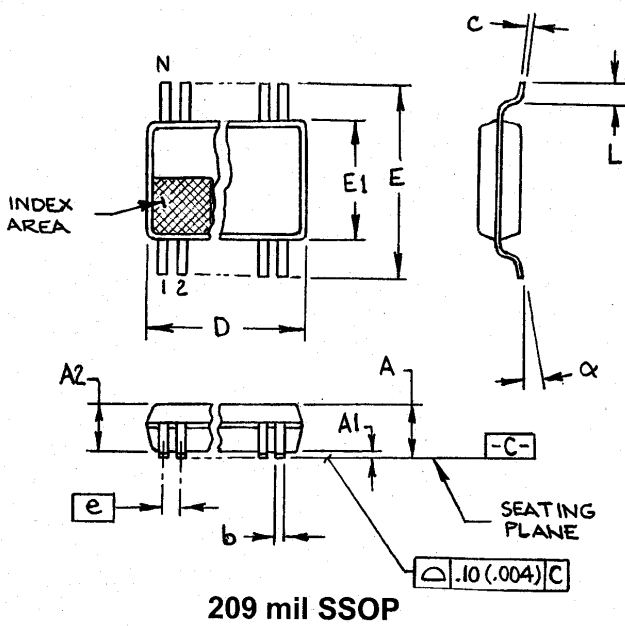
PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internally by the **ICS9248-157** prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the crystal oscillator. The power on latency is guaranteed to be less than 3ms. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9248.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.



| SYMBOL | In Millimeters | | In Inches | |
|--------|-------------------|-------------------|-------------------|-------------------|
| | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS |
| | MIN | MAX | MIN | MAX |
| A | - | 2.00 | - | .079 |
| A1 | 0.05 | - | .002 | - |
| A2 | 1.65 | 1.85 | .065 | .073 |
| b | 0.22 | 0.38 | .009 | .015 |
| c | 0.09 | 0.25 | .0035 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 7.40 | 8.20 | .291 | .323 |
| E1 | 5.00 | 5.60 | .197 | .220 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.55 | 0.95 | .022 | .037 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 28 | 9.90 | 10.50 | .390 | .413 |

MO-150 JEDEC 6/17/00 Rev B
Doc. # 10-0033

Ordering Information

ICS9248yF-157-T

Example:

ICS XXXX y F - PPP - T

