

Frequency Generator & Integrated Buffers for PENTIUM/Pro™

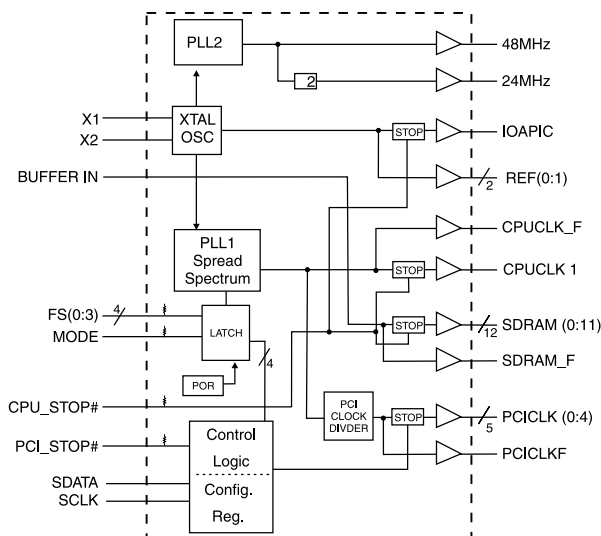
General Description

The ICS9248-39 generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro or Cyrix. Eight different reference frequency multiplying factors are externally selectable with smooth frequency transitions.

Features include two CPU, six PCI and thirteen SDRAM clocks. Two reference outputs are available equal to the crystal frequency. Plus the IOAPIC output powered by VDDL1. One 48 MHz for USB, and one 24 MHz clock for Super IO. Spread Spectrum built in at $\pm 0.5\%$ or $\pm 0.25\%$ modulation to reduce the EMI. Serial programming I²C interface allows changing functions, stop clock programming and Frequency selection. Additionally, the device meets the Pentium power-up stabilization, which requires that CPU and PCI clocks be stable within 2ms after power-up. It is not recommended to use I/O dual function pin for the slots (ISA, PIC, CPU, DIMM). The add on card might have a pull up or pull down.

High drive PCICLK and SDRAM outputs typically provide greater than 1 V/ns slew rate into 30pF loads. CPUCLK outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50 \pm 5% duty cycle. The REF and 24 and 48 MHz clock outputs typically provide better than 0.5V/ns slew rates into 20pF.

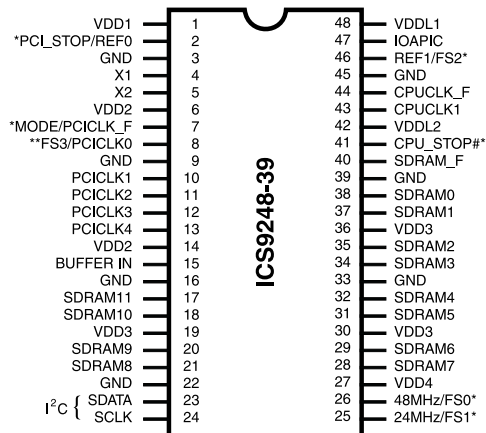
Block Diagram



Features

- 3.3V outputs: SDRAM, PCI, REF, 48/24MHz
- 2.5V outputs: CPU, IOAPIC
- 20 ohm CPU clock output impedance
- 20 ohm PCI clock output impedance
- Skew from CPU (earlier) to PCI clock - 1.5 to 4 ns, center 2.6 ns.
- No external load cap for C_L=18pF crystals
- ± 175 ps CPU clock skew
- 250ps (cycle to cycle) CPU jitter
- Smooth frequency switch, with selections from 66.8 to 150 MHz CPU.
- I²C interface for programming
- 3ms power up clock stable time
- Clock duty cycle 45-55%.
- 48 pin 300 mil SSOP package
- 3.3V operation, 5V tolerant inputs (with series R)
- <5ns propagation delay SDRAM from Buffer Input

Pin Configuration



48-Pin SSOP

- * Internal Pull-up Resistor of 240K to VDD
- ** Internal Pull-down resistor of 240K to GND

Power Groups

- VDD1 = REF (0:1), X1, X2
- VDD2 = PCICLK_F, PCICLK(0:4)
- VDD3 = SDRAM (0:12), supply for PLL core
- VDD4 = 24MHz, 48MHz
- VDDL1 = IOAPIC
- VDDL2 = CPUCLK 1, CPUCLK_F

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ICS9248-39



Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|--|------------------------|------|--|
| 1 | VDD1 | PWR | Ref (0:2), XTAL power supply, nominal 3.3V |
| 2 | REF0 | OUT | 14.318 Mhz reference clock.This REF output is the STRONGER buffer for ISA BUS loads |
| | PCI_STOP# ¹ | IN | Halts PCICLK(0:4) clocks at logic 0 level, when input low (In mobile mode, MODE=0) |
| 3,9,16,22,33,39,45 | GND | PWR | Ground |
| 4 | X1 | IN | Crystal input, has internal load cap (36pF) and feedback resistor from X2 |
| 5 | X2 | OUT | Crystal output, nominally 14.318MHz. Has internal load cap (36pF) |
| 6,14 | VDD2 | PWR | Supply for PCICLK_F and PCICLK (0:4), nominal 3.3V |
| 7 | PCICLK_F | OUT | Free running PCI clock not affected by PCI_STOP# for power management. |
| | MODE ^{1,2} | IN | Pin 2 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input. |
| 8 | FS3 | IN | Frequency select pin. Latched Input. Internal Pull-down to GND |
| | PCICLK0 | OUT | PCI clock outputs. Syncheronous to CPU clocks with 1-48ns skew (CPU early) |
| 10, 11, 12, 13 | PCICLK(1:4) | OUT | PCI clock outputs. Syncheronous to CPU clocks with 1-48ns skew (CPU early) |
| 15 | BUFFER IN | IN | Input to Fanout Buffers for SDRAM outputs. |
| 17, 18, 20, 21, 28, 29, 31, 32, 34, 35,37,38 | SDRAM (11:0) | OUT | SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset). |
| 19,30,36 | VDD3 | PWR | Supply for SDRAM (0:12) and CPU PLL Core, nominal 3.3V. |
| 23 | SDATA | IN | Data input for I ² C serial input, 5V tolerant input |
| 24 | SCLK | IN | Clock input of I ² C input, 5V tolerant input |
| 25 | 24MHz | OUT | 24MHz output clock |
| | FS1 ^{1,2} | IN | Frequency select pin. Latched Input. |
| 26 | 48MHz | OUT | 48MHz output clock |
| | FS0 ^{1,2} | IN | Frequency select pin. Latched Input |
| 27 | VDD4 | PWR | Power for 24 & 48MHz output buffers and fixed PLL core. |
| 40 | SDRAM_F | OUT | Free running SDRAM clock output. Not affected by CPU_STOP# |
| 41 | CPU_STOP# | IN | This asynchronous input halts CPUCLK1, IOAPIC & SDRAM (0:11) at logic "0" level when driven low. |
| 42 | VDDL2 | PWR | Supply for CPU clocks, either 2.5V or 3.3V nominal |
| 43 | CPUCLK1 | OUT | CPU clock outputs, powered by VDDL2. Low if CPU_STOP#=Low |
| 44 | CPUCLK_F | OUT | Free running CPU clock. Not affected by the CPU_STOP# |
| 46 | REF1 | OUT | 14.318 MHz reference clock. |
| | FS2 ^{1,2} | IN | Frequency select pin. Latched Input |
| 47 | IOAPIC | OUT | IOAPIC clock output. 14.318 MHz Powered by VDDL1. |
| 48 | VDDL1 | PWR | Supply for IOAPIC, either 2.5 or 3.3V nominal |

Notes:

- 1: Internal Pull-up Resistor of 240K to 3.3V on indicated inputs
- 2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.



Mode Pin - Power Management Input Control

| MODE, Pin 7 (Latched Input) | Pin 2 |
|--------------------------------|----------------------|
| 0 | PCI_STOP# (Input) |
| 1 | REF0 (Output) |

Functionality

$V_{DD1,2,3} = 3.3V \pm 5\%$, $V_{DDL1,2} = 2.5V \pm 5\%$ or $3.3 \pm 5\%$, $T_A = 0$ to $70^\circ C$
Crystal (X1, X2) = 14.31818MHz

| FS3 | FS2 | FS1 | FS0 | CPU (MHz) | PCICLK (MHz) |
|-----|-----|-----|-----|--------------|---------------|
| 1 | 1 | 1 | 1 | 133 | 33.3 (CPU/4) |
| 1 | 1 | 1 | 0 | 124 | 31 (CPU/4) |
| 1 | 1 | 0 | 1 | 150 | 37.5 (CPU/4) |
| 1 | 1 | 0 | 0 | 140 | 35 (CPU/4) |
| 1 | 0 | 1 | 1 | 105 | 35 (CPU/3) |
| 1 | 0 | 1 | 0 | 110 | 36.67 (CPU/3) |
| 1 | 0 | 0 | 1 | 115 | 38.33 (CPU/3) |
| 1 | 0 | 0 | 0 | 120 | 40.00 (CPU/3) |
| 0 | 1 | 1 | 1 | 100.3 | 33.43 (CPU/3) |
| 0 | 1 | 1 | 0 | 133 | 44.33 (CPU/3) |
| 0 | 1 | 0 | 1 | 112 | 37.33 (CPU/3) |
| 0 | 1 | 0 | 0 | 103 | 34.33 (CPU/2) |
| 0 | 0 | 1 | 1 | 66.8 | 33.40 (CPU/2) |
| 0 | 0 | 1 | 0 | 83.3 | 41.65 (CPU/2) |
| 0 | 0 | 0 | 1 | 75 | 37.5 (CPU/2) |
| 0 | 0 | 0 | 0 | 124 | 41.33 (CPU/3) |



Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

| Bit | Description | PWD |
|----------------------------------|--|-------|
| Bit 7 | 0 - $\pm 0.25\%$ Spread Spectrum Modulation 1 - $\pm 0.5\%$ Spread Spectrum Modulation | 0 |
| | Bit2 Bit6 Bit5 Bit4 CPU clock PCI | |
| Bit 2, Bit 6:4 | 0111 100.3 33.43 (CPU/3) | Note1 |
| | 0110 133 44.33 (CPU/3) | |
| | 0101 112 37.33 (CPU/3) | |
| | 0100 103 34.3 (CPU/3) | |
| | 0011 66.8 33.4 (CPU/2) | |
| | 0010 83.3 41.65(CPU/2) | |
| | 0001 75 37.5 (CPU/2) | |
| | 0000 124 41.33 (CPU/3) | |
| | 1111 133 33.25 (CPU/4) | |
| | 1110 124 31.00 (CPU/4) | |
| | 1101 150 37.50 (CPU/4) | |
| | 1100 140 35.00 (CPU/4) | |
| | 1011 105 35.00 (CPU/3) | |
| | 1010 110 36.67 (CPU/3) | |
| 1001 115 38.33 (CPU/3) | | |
| 1000 120 40.00 (CPU/3) | | |
| Bit 3 | 0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 6:4 (above) | 0 |
| Bit 1 | 0 - Normal 1 - Spread Spectrum Enabled (Center Spread) | 0 |
| Bit 0 | 0 - Running 1- Tristate all outputs | 0 |

Note 1. Default at Power-up will be for latched logic inputs to define frequency. Bits 4, 5, 6 are default to 000, and if bit 3 is written to a 1 to use Bits 6:4, then these should be defined to desired frequency at same write cycle.

Note: PWD = Power-Up Default

**Byte 1: CPU, Active/Inactive Register (1 = enable, 0 = disable)**

| Bit | Pin # | PWD | Description |
|-------|-------|-----|----------------------|
| Bit 7 | - | X | Latched FS2# |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | 40 | 1 | SDRAM12 (Act/Inact) |
| Bit 2 | - | 1 | (Reserved) |
| Bit 1 | 43 | 1 | CPUCLK1 (Act/Inact) |
| Bit 0 | 44 | 1 | CPUCLK_F (Act/Inact) |

Byte 2: PCI Active/Inactive Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|----------------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | 7 | 1 | PCICLK_F (Act/Inact) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | 13 | 1 | PCICLK4 (Act/Inact) |
| Bit 3 | 12 | 1 | PCICLK3 (Act/Inact) |
| Bit 2 | 11 | 1 | PCICLK2 (Act/Inact) |
| Bit 1 | 10 | 1 | PCICLK1 (Act/Inact) |
| Bit 0 | 8 | 1 | PCICLK0 (Act/Inact) |

Byte 3: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------------|-----|--------------------------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | X | Latched FS0# |
| Bit 5 | 26 | 1 | 48MHz (Act/Inact) |
| Bit 4 | 25 | 1 | 24 MHz (Act/Inact) |
| Bit 3 | - | 1 | (Reserved) |
| Bit 2 | 21,20,18,17 | 1 | SDRAM (8:11) (Active/Inactive) |
| Bit 1 | 32,31,29,28 | 1 | SDRAM (4:7) (Active/Inactive) |
| Bit 0 | 38,37,35,34 | 1 | SDRAM (0:3) (Active/Inactive) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.



Byte 4: Reserved Active/Inactive Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|--------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | - | 1 | (Reserved) |
| Bit 3 | - | X | Latched FS1# |
| Bit 2 | - | 1 | (Reserved) |
| Bit 1 | - | X | Latched FS3# |
| Bit 0 | - | 1 | (Reserved) |

Byte 5: Peripheral Active/Inactive Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|---------------------|
| Bit 7 | - | 1 | (Reserved) |
| Bit 6 | - | 1 | (Reserved) |
| Bit 5 | - | 1 | (Reserved) |
| Bit 4 | 47 | 1 | IOAPIC0 (Act/Inact) |
| Bit 3 | - | 1 | (Reserved) |
| Bit 2 | - | 1 | (Reserved) |
| Bit 1 | 46 | 1 | REF1 (Act/Inact) |
| Bit 0 | 2 | 1 | REF0 (Act/Inact) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.



Absolute Maximum Ratings

| | |
|---|--------------------------------------|
| Supply Voltage | 5.5 V |
| Logic Inputs | GND -0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Case Temperature | 115°C |
| Storage Temperature | -65°C to +150°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70° C; Supply Voltage V_{DD}, V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | 2.0 | | μA |
| Input Low Current | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | -100 | | μA |
| Operating Supply Current | I _{DD3.3OP66} | C _L = 0 pF; Select @ 66MHz | | 146 | 180 | mA |
| | I _{DD3.3OP100} | C _L = 0 pF; Select @ 100MHz | | 174 | | |
| Input frequency | F _i | V _{DD} = 3.3 V; | 12 | 14.318 | 16 | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | 36 | 45 | pF |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target Freq. | | | 3 | ms |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70° C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------|-------------------------|--|-----|-----|-----|-------|
| Operating Supply Current | I _{DD2.5OP66} | C _L = 0 pF; Select @ 66.8 MHz | | 4 | 72 | mA |
| | I _{DD2.5OP100} | C _L = 0 pF; Select @ 100 MHz | | 6 | 100 | |
| Skew1 | t _{CPU-PCI} | V _T = 1.5 V; V _{IL} = 1.25 V | 1.5 | 2.5 | 4 | ns |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPUCLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|---------------------------|---|------|------|------|-------|
| Output High Voltage | V_{OH2B} | $I_{OH} = -12.0\text{ mA}$ | 2 | 2.23 | | V |
| Output Low Voltage | V_{OL2B} | $I_{OL} = 12\text{ mA}$ | | 0.32 | 0.4 | V |
| Output High Current | I_{OH2B} | $V_{OH} = 1.7\text{ V}$ | | -32 | -19 | mA |
| Output Low Current | I_{OL2B} | $V_{OL} = 0.7\text{ V}$ | 19 | 25 | | mA |
| Rise Time | t_{r2B}^1 | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.0\text{ V}$ | | 1.48 | 1.6 | ns |
| Fall Time | t_{f2B}^1 | $V_{OH} = 2.0\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | 1.25 | 1.6 | ns |
| Duty Cycle | d_{t2B}^1 | $V_T = 1.25\text{ V}$ | 45 | 45 | 55 | % |
| Skew | t_{sk2B}^1 | $V_T = 1.25\text{ V}$ | | 125 | 175 | ps |
| Jitter, Cycle-to-cycle | $t_{j\text{cyc-cyc}2B}^1$ | $V_T = 1.25\text{ V}$ | | 225 | 250 | ps |
| Jitter, One Sigma | t_{j1s2B}^1 | $V_T = 1.25\text{ V}$ | | 36 | 150 | ps |
| Jitter, Absolute | t_{jabs2B}^1 | $V_T = 1.25\text{ V}$ | -250 | 130 | +250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|---------------------------|---|------|------|-----|-------|
| Output High Voltage | V_{OH1} | $I_{OH} = -11\text{ mA}$ | 2.4 | 3.05 | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 9.4\text{ mA}$ | | 0.17 | 0.4 | V |
| Output High Current | I_{OH1} | $V_{OH} = 2.0\text{ V}$ | | -52 | -22 | mA |
| Output Low Current | I_{OL1} | $V_{OL} = 0.8\text{ V}$ | 25 | 40 | | mA |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | | 2 | 2 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | 1.65 | 2 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5\text{ V}$ | 45 | 49 | 55 | % |
| Skew ¹ | t_{sk1} | $V_T = 1.5\text{ V}$ | | 240 | 500 | ps |
| Jitter, Cycle-to-cycle | $t_{j\text{cyc-cyc}1B}^1$ | $V_T = 1.5\text{ V}$ | | 210 | 250 | ps |
| Jitter, One Sigma ¹ | t_{j1s1} | $V_T = 1.5\text{ V}$ | | 18 | 150 | ps |
| Jitter, Absolute ¹ | t_{jabs1} | $V_T = 1.5\text{ V}$ | -500 | 90 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 30\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------|------------|---|-----|------|-----|-------|
| Output High Voltage | V_{OH3} | $I_{OH} = -28\text{ mA}$ | 2.4 | 2.9 | | V |
| Output Low Voltage | V_{OL3} | $I_{OL} = 23\text{ mA}$ | | 0.4 | 0.4 | V |
| Output High Current | I_{OH3} | $V_{OH} = 2.0\text{ V}$ | | -77 | -54 | mA |
| Output Low Current | I_{OL3} | $V_{OL} = 0.8\text{ V}$ | 41 | 41 | | mA |
| Rise Time | T_{r3}^1 | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | | 1.5 | 2 | ns |
| Fall Time | T_{f3}^1 | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | 1.8 | 2 | ns |
| Duty Cycle | D_{t3}^1 | $V_T = 1.5\text{ V}$ | 45 | 49.5 | 55 | % |
| Skew ¹ | T_{sk1} | $V_T = 1.5\text{ V}$ | | 190 | 500 | ps |
| Propagation Delay | T_{prop} | $V_T = 1.5\text{ V}$ | | 3 | 5 | ns |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|--------------|---|-----|------|-----|-------|
| Output High Voltage | V_{OH4B} | $I_{OH} = -12\text{ mA}$ | 2 | 2.12 | | V |
| Output Low Voltage | V_{OL4B} | $I_{OL} = 12\text{ mA}$ | | 0.32 | 0.4 | V |
| Output High Current | I_{OH4B} | $V_{OH} = 1.7\text{ V}$ | | -23 | -19 | mA |
| Output Low Current | I_{OL4B} | $V_{OL} = 0.7\text{ V}$ | 19 | 25 | | mA |
| Rise Time ¹ | T_{r4B} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.0\text{ V}$ | | 1.45 | 2 | ns |
| Fall Time ¹ | T_{f4B} | $V_{OH} = 2.0\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | 1.3 | 2 | ns |
| Duty Cycle ¹ | D_{t4B} | $V_T = 1.25\text{ V}$ | 45 | 51 | 55 | % |
| Jitter, One Sigma ¹ | T_{j1s4B} | $V_T = 1.25\text{ V}$ | | 0.2 | 0.5 | ns |
| Jitter, Absolute ¹ | T_{jabs4B} | $V_T = 1.25\text{ V}$ | -1 | 0.5 | 1 | ns |

¹Guaranteed by design, not 100% tested in production.

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Electrical Characteristics - 24MHz, 48MHz, REF(0:1)

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$, $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------|---|-----|------|-----|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -16\text{ mA}$ | 2.4 | 2.73 | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9\text{ mA}$ | | 0.23 | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0\text{ V}$ | | -32 | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8\text{ V}$ | 16 | 28 | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$ | | 1.8 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$ | | 1.8 | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5\text{ V}$ | 45 | 51 | 55 | % |
| Jitter, One Sigma ¹ | t_{j1s5} | $V_T = 1.5\text{ V}$ | | 0.2 | 0.5 | ns |
| Jitter, Absolute ¹ | t_{jabs5} | $V_T = 1.5\text{ V}$ | -1 | 0.5 | 1 | ns |

¹Guaranteed by design, not 100% tested in production.



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

| How to Write: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

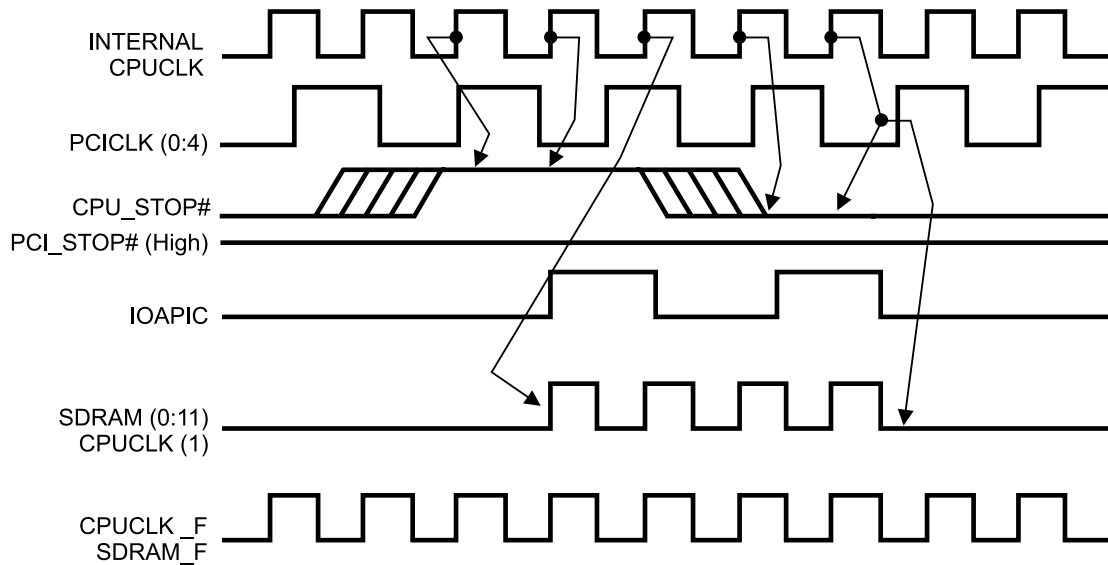
Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



CPU_STOP# Timing Diagram

CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS9248-39**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



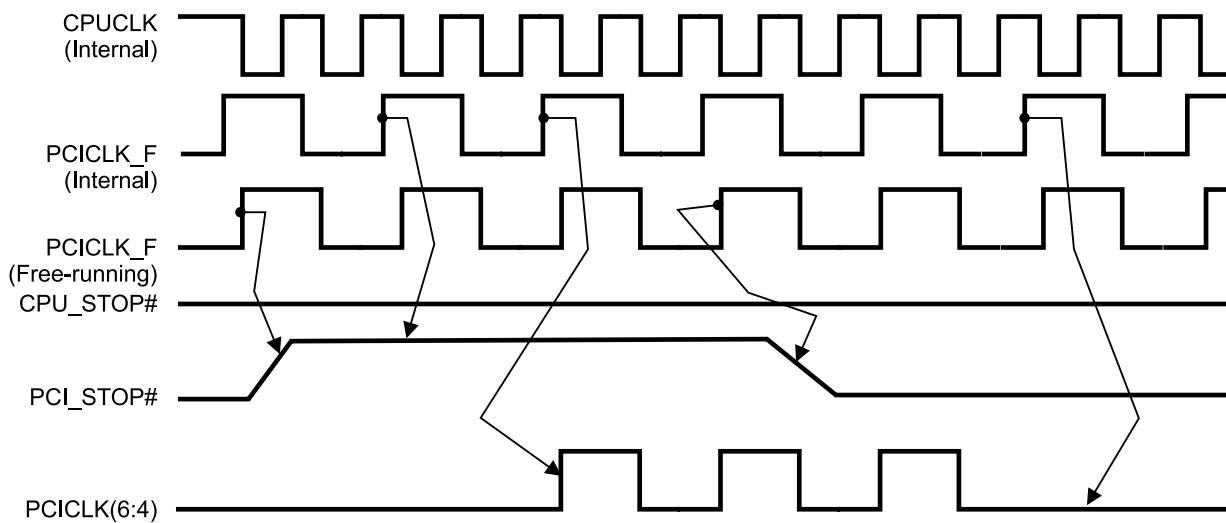
Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-39.
3. IOAPIC output is Stopped Glitch Free by CPUSTOP# going low.
4. SDRAM-F output is controlled by Buffer in signal, not affected by the **ICS9248-39** CPU_STOP# signal. SDRAM (0:11) are controlled as shown.
5. All other clocks continue to run undisturbed.



PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the ICS9248-39. It is used to turn off the PCICLK (0:4) clocks for low power operation. PCI_STOP# is synchronized by the ICS9248-39 internally. The minimum that the PCICLK (0:4) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:4) clocks. PCICLK (0:4) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:4) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

- 1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
- 2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
- 3. All other clocks continue to run undisturbed.
- 4. CPU_STOP# is shown in a high (true) state.



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-39 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

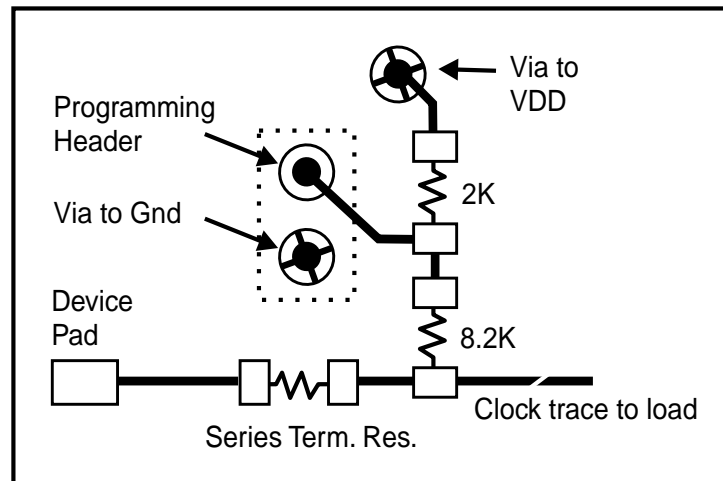


Fig. 1



General Layout Precautions:

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.

Notes:

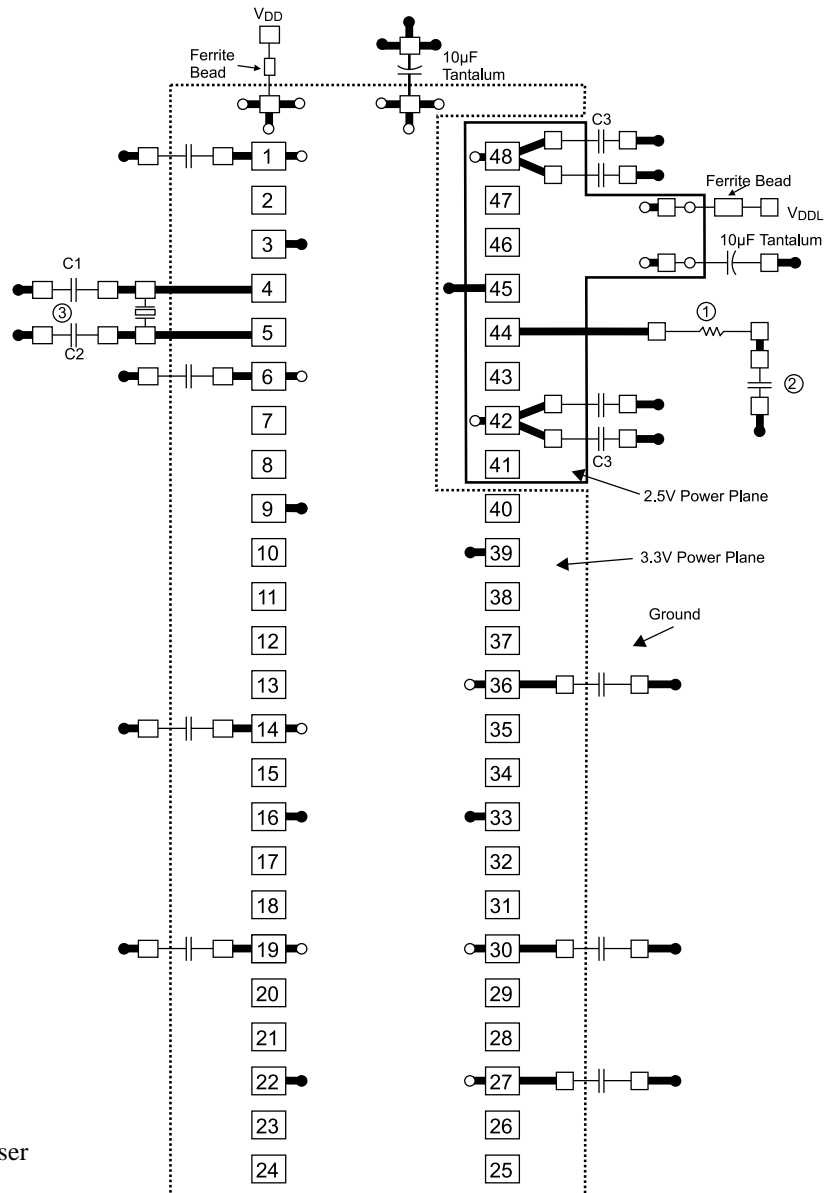
- 1 All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram
- 2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
- 3 Optional crystal load capacitors are recommended.

Capacitor Values:

C1, C2 : Crystal load values determined by user

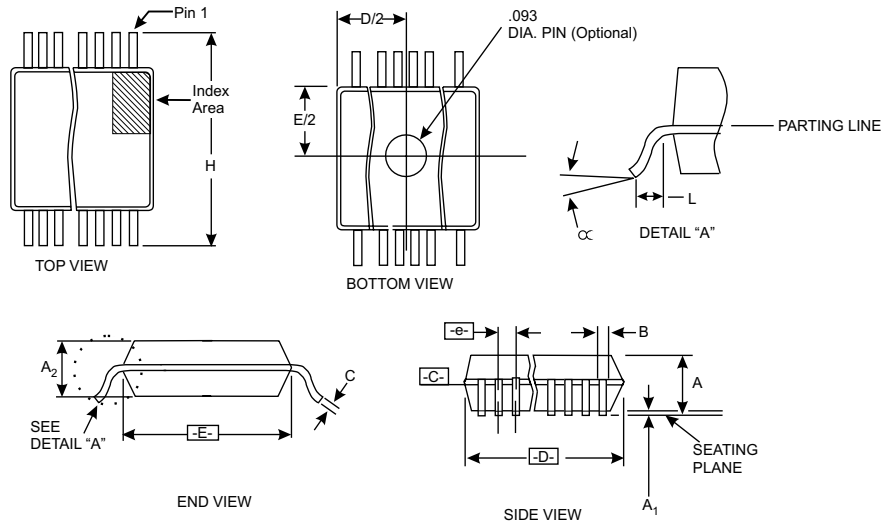
C3 : 100pF ceramic

All unmarked capacitors are 0.01 F ceramic



- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads

ICS9248-39



| SYMBOL | COMMON DIMENSIONS | | | VARIATIONS | D | | | N |
|--------|-------------------|------|-------|---|------|------|------|----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .095 | .102 | .110 | AC | .620 | .625 | .630 | 48 |
| A1 | .008 | .012 | .016 | "For current dimensional specifications, see JEDEC 95." | | | | |
| A2 | .087 | .090 | .094 | | | | | |
| B | .008 | - | .0135 | | | | | |
| C | .005 | - | .0085 | | | | | |
| D | See Variations | | | | | | | |
| E | .291 | .295 | .299 | | | | | |
| e | 0.025 BSC | | | | | | | |
| H | .395 | - | .420 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .020 | - | .040 | | | | | |
| N | See Variations | | | | | | | |
| ∞ | 0° | - | 8° | | | | | |

48 Pin 300 mil SSOP Package

Ordering Information

ICS9248yF-39

Example:

ICS XXXX y F - PPP

