

Frequency Timing Generator for PENTIUM II Systems

General Description

The ICS9248-77 is a main clock synthesizer chip for Pentium II based systems using Rambus Interface DRAMs. This chip provides all the clocks required for such a system when used with a Direct Rambus Clock Generator(DRCG) chip such as the ICS9212-01.

Spread Spectrum may be enabled by driving the SPREAD# pin active. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-77 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

The CPU/2 clocks are inputs to the DRCG.

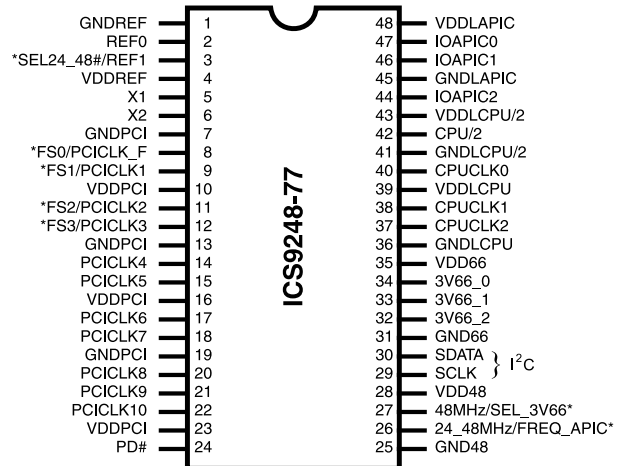
Features

- Generates the following system clocks:
 - 3 - CPUs @ 2.5V, up to 150MHz.
 - 3 - IOAPIC @ 2.5V, PCI or PCI/2
 - 3 - 3V66MHz @ 3.3V.
 - 11 - PCIs @ 3.3V.
 - 1 - 48MHz, @ 3.3V fixed.
 - 1 - 24MHz, @ 3.3V fixed.
 - 1 - CPU/2, @ 2.5V.
- ± .25% center spread, or 0 to -.5% down spread.
- Uses external 14.318MHz crystal.

Key Specification

- CPU Output Jitter: <250ps
- CPU/2 Output Jitter: <250ps
- IOAPIC Output Jitter: <500ps
- 48MHz, 3V66, PCI Output Jitter: <500ps
- Ref Output Jitter: <1000ps
- CPU Output Skew: <175ps
- IOAPIC Output Skew <250ps
- PCI Output Skew: <500ps
- 3V66 Output Skew <250ps
- CPU to 3V66 Output Offset: 0.0 - 1.5ns (CPU leads)
- 3V66 to PCI Output Offset: 1.5 - 4.0ns (3V66 leads)
- CPU to IOAPIC Output Offset 1.5 - 4.0ns (CPU leads)

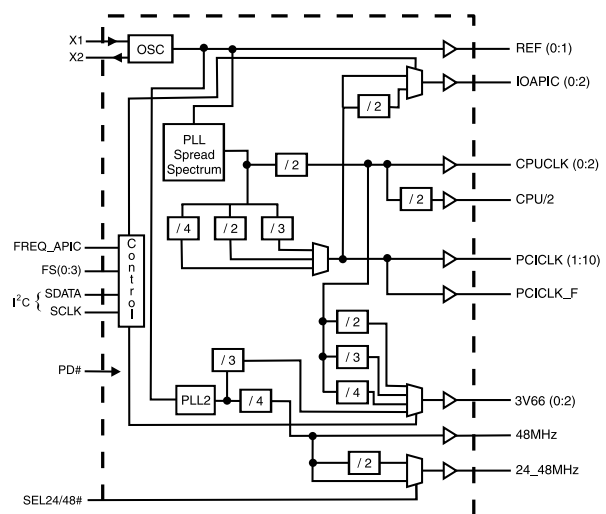
Pin Configuration



48-pin SSOP

* 120K ohm pull-up to VDD on indicated inputs.

Block Diagram



ICS9248-77



Power Groups:

VDDREF, GNDREF = REF, X1, X2

GNDPCI, VDDPCI = PCICLK

VDD66, GND66 = 3V66

VDD48, GND48 = 48MHz

VDDCOR, GNDCOR = PLL Core

VDDLCPU/2, GNDLCPU/2 = CPU/2

VDDLIOAPIC, GNDIOAPIC = IOAPIC

Pin Descriptions

| Pin number | Pin name | Type | Description |
|----------------------------|----------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 7, 13, 19, 25, 31 | GND | PWR | Ground pins |
| 2 | REF0 | OUT | 14.318MHz reference clock outputs at 3.3V |
| 3 | REF1 | OUT | 14.318MHz reference clock outputs at 3.3V |
| | SEL24_48 | IN | Logic input to select 24 or 48MHz for pin 26 output |
| 4, 10, 16, 23, 28, 35 | VDD | PWR | Power pins 3.3V |
| 5 | X1 | IN | XTAL_IN 14.318MHz crystal input |
| 6 | X2 | OUT | XTAL_OUT Crystal output |
| 8 | PCICLK_F | OUT | Free running PCI clock at 3.3V. Synchronous to CPU clocks. Not affected by the PCI_STOP# input. |
| | FS0 | IN | Logic - input for frequency selection |
| 9 | PCICLK1 | OUT | PCI clock output at 3.3V. Synchronous to CPU clocks. |
| | FS1 | IN | Logic - input for frequency selection |
| 11 | PCICLK2 | OUT | PCI clock output at 3.3V. Synchronous to CPU clocks. |
| | FS2 | IN | Logic - input for frequency selection |
| 12 | PCICLK3 | OUT | PCI clock output at 3.3V. Synchronous to CPU clocks. |
| | FS3 | IN | Logic - input for frequency selection |
| 14, 15, 17, 18, 20, 21, 22 | PCICLK [4:10] | OUT | PCI clock outputs at 3.3V. Synchronous to CPU clocks. |
| 24 | PD# | IN | This asynchronous input powers down the chip when drive active(Low). The internal PLLs are disabled and all the output clocks are held at a Low state. |
| 26 | 24_48MHz | OUT | 24 or 48MHz output selectable by SEL24_48# (0=48MHz 1=24MHz) |
| | FREQ_APIC | IN | Logic input for frequency selection of IOAPIC |
| 27 | 48MHz/SEL_3V66 | OUT/IN | Fixed 48MHz clock output. 3.3V / Logic input to select the frequency of the 3V66 outputs |
| 29 | SCLK | IN | Clock input of I ² C input |
| 30 | SDATA | IN | Data input for I ² C serial input. |
| 32, 33, 34 | 3V66[0:2] | OUT | 3.3V clock outputs. These outputs are stopped when CPU_STOP# is driven active.. |
| 36 | GNDLCPU | PWR | Ground pin for the CPUCLKs |
| 37, 38, 40 | CPUCLK[0:2] | OUT | Host bus clock output at 2.5V. |
| 39 | VDDLCPU | PWR | Power pin for the CPUCLKs. 2.5V |
| 41 | GNDLCPU/2 | PWR | Ground pin for the CPU/2 clocks. |
| 42 | CPU/2 | OUT | 2.5V clock outputs at 1/2 CPU frequency. |
| 43 | VDDLCPU/2 | PWR | Power pin for the CPU/2 clocks. 2.5V |
| 45 | GNDLIOAPIC | PWR | Ground pin for the IOAPIC outputs. |
| 44, 46, 47 | IOAPIC[0:2] | OUT | IOAPIC clocks at 2.5V. Synchronous with CPUCLKs |
| 48 | VDDLIOAPIC | PWR | Power pin for the IOAPIC outputs. 2.5V. |



Frequency Selection

| FS3 | FS2 | FS1 | FS0 | CPU MHz | CPU/2 MHz | PCI MHz | 3V66 MHz | | IOAPIC MHz | |
|-----|-----|-----|-----|---------|-----------|---------|------------|------------|-------------|-------------|
| | | | | | | | SEL_3V66=0 | SEL_3V66=1 | FREQ_APIC=0 | FREQ_APCI=1 |
| 0 | 0 | 0 | 0 | 105 | 52.5 | 35 | 70 | 70 | 17.5 | 35 |
| 0 | 0 | 0 | 1 | 75 | 37.5 | 37.5 | 64* | 75 | 18.75 | 37.5 |
| 0 | 0 | 1 | 0 | 100.3 | 50.15 | 33.4 | 66.6 | 66.6 | 16.7 | 33.4 |
| 0 | 0 | 1 | 1 | 66.8 | 33.4 | 33.4 | 66.6 | 66.6 | 16.67 | 33.4 |
| 0 | 1 | 0 | 0 | 110 | 55 | 36.6 | 64* | 73.3 | 18.3 | 36.6 |
| 0 | 1 | 0 | 1 | 115 | 57.5 | 38.3 | 64* | 76.6 | 19.16 | 38.3 |
| 0 | 1 | 1 | 0 | 117 | 58.5 | 39 | 64* | 78 | 19.5 | 39 |
| 0 | 1 | 1 | 1 | 120 | 60 | 40 | 64* | 80 | 20 | 40 |
| 1 | 0 | 0 | 0 | 125 | 62.5 | 41.6 | 64* | 83.3 | 20.8 | 41.6 |
| 1 | 0 | 0 | 1 | 127 | 63.5 | 42.3 | 64* | 84.6 | 21.16 | 42.3 |
| 1 | 0 | 1 | 0 | 133.3 | 66.5 | 33.3 | 66.6 | 66.6 | 16.6 | 33.3 |
| 1 | 0 | 1 | 1 | 135 | 67.5 | 33.75 | 67.5 | 67.5 | 16.8 | 33.75 |
| 1 | 1 | 0 | 0 | 137 | 68.5 | 34.25 | 68.5 | 68.5 | 17.125 | 34.25 |
| 1 | 1 | 0 | 1 | 140 | 70 | 35 | 70 | 70 | 17.5 | 35 |
| 1 | 1 | 1 | 0 | 145 | 72.5 | 36.25 | 64* | 72.5 | 18.125 | 36.25 |
| 1 | 1 | 1 | 1 | 150 | 75 | 37.5 | 64* | 75 | 18.75 | 37.5 |

Note:

* These output frequencies are Not synchronous to CPUCLK and Do Not have Spread Spectrum modulation.



Power Management Features:

| PD# | CPUCLK | CPU/2 | IOAPIC | 3V66 | PCI | PCL_F | REF. 48MHz | Osc | VCOs |
|-----|--------|-------|--------|------|-----|-------|---------------|-----|------|
| 0 | LOW | LOW | LOW | LOW | LOW | LOW | LOW | OFF | OFF |
| 1 | ON | ON | ON | ON | ON | ON | ON | ON | ON |

Note:

1. LOW means outputs held static LOW as per latency requirement next page.
2. On means active.
3. PD# pulled Low, impacts all outputs including REF and 48 MHz outputs.

Power Management Requirements:

| Signal | Signal State | Latency |
|--------|----------------------|-------------------------------|
| | | No. of rising edges of PCICLK |
| PD# | 1 (normal operation) | 3mS |
| | 0 (power down) | 2max. |

Note:

1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high to when the first valid clocks are driven from the device).



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte **one at a time**.
- Controller (host) sends a Stop bit

| How to Write: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



Serial Configuration Command Bitmap

Byte 0: Functionality and frequency select register (Default = 0)

| Bit | Description | | | | | | | PWD |
|-----------------|---------------------------------------------------------------------------------------------------------|--------|------------|------------|--------|-------------|-------------|--------|
| Bit 7 | 0 - $\pm 0.25\%$ Center Spread Spectrum | | | | | | | 0 |
| | 1 - Down Spread Spectrum 0 to -0.5% | | | | | | | |
| Bit (2, 6:4) | Bit (2, 6:4) | CPUCLK | 3V66 | | PCICLK | IOAPIC | | Note 1 |
| | | | 3V66_SEL=0 | 3V66_SEL=1 | | FREQ_APIC=0 | FREQ_APIC=1 | |
| | 0000 | 105 | 70 | 70 | 35 | 17.5 | 35 | |
| | 0001 | 75 | 64* | 75 | 37.5 | 18.75 | 37.5 | |
| | 0010 | 100.3 | 66.6 | 66.6 | 33.4 | 16.7 | 33.4 | |
| | 0011 | 66.8 | 66.6 | 66.6 | 33.4 | 16.67 | 33.4 | |
| | 0100 | 110 | 64* | 73.3 | 36.6 | 18.3 | 36.6 | |
| | 0101 | 115 | 64* | 76.6 | 38.3 | 19.16 | 38.3 | |
| | 0110 | 117 | 64* | 78 | 39 | 19.5 | 39 | |
| | 0111 | 120 | 64* | 80 | 40 | 20 | 40 | |
| | 1000 | 125 | 64* | 83.3 | 41.6 | 20.8 | 41.6 | |
| | 1001 | 127 | 64* | 84.6 | 42.3 | 21.16 | 42.3 | |
| | 1010 | 133.3 | 66.6 | 66.6 | 33.3 | 16.6 | 33.3 | |
| | 1011 | 135 | 67.5 | 67.5 | 33.75 | 16.8 | 33.75 | |
| | 1100 | 137 | 68.5 | 68.5 | 34.25 | 17.125 | 34.25 | |
| 1101 | 140 | 70 | 70 | 35 | 17.5 | 35 | | |
| 1110 | 145 | 64* | 72.5 | 36.25 | 18.125 | 36.25 | | |
| 1111 | 150 | 64* | 75 | 37.5 | 18.75 | 37.5 | | |
| Bit 3 | 0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2, 6:4 | | | | | | | 0 |
| Bit 1 | 0 - Normal 1 - Spread spectrum enabled | | | | | | | 0 |
| Bit 0 | 0 - Running 1 - Tristate all outputs | | | | | | | 0 |

Note 1: Default at power-up will be for latched logic inputs to define frequency.

* These output frequencies are not synchronous to CPUCLK and do not have Spread Spectrum modulation.



Byte 1: CPU, Active/Inactive Register
(1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 40 | 1 | CPUCLK 0 |
| Bit 6 | 38 | 1 | CPUCLK 1 |
| Bit 5 | 37 | 1 | CPUCLK 2 |
| Bit 4 | 42 | 1 | CPU/2 |
| Bit 3 | 47 | 1 | IOAPIC0 |
| Bit 2 | 46 | 1 | IOAPIC1 |
| Bit 1 | 2 | 1 | REF1 |
| Bit 0 | 3 | 1 | REF0 |

Note:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 2: PCI Active/Inactive Register
(1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 18 | 1 | PCICLK7 |
| Bit 6 | 17 | 1 | PCICLK6 |
| Bit 5 | 15 | 1 | PCICLK5 |
| Bit 4 | 14 | 1 | PCICLK4 |
| Bit 3 | 12 | 1 | PCICLK3 |
| Bit 2 | 11 | 1 | PCICLK2 |
| Bit 1 | 9 | 1 | PCICLK1 |
| Bit 0 | 8 | 1 | PCICLK_F |

Note:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 3: 3V66 Active/Inactive Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 34 | 1 | 3V66_0 |
| Bit 6 | 33 | 1 | 3V66_1 |
| Bit 5 | 32 | 1 | 3V66_2 |
| Bit 4 | - | X | FS1# |
| Bit 3 | - | 1 | (Reserved) |
| Bit 2 | - | 1 | (Reserved) |
| Bit 1 | - | X | FS3# |
| Bit 0 | - | X | FS2# |

Note:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 4: PCI Active/Inactive Register (1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|-------|-------|-----|-------------|
| Bit 7 | 26 | 1 | 24_48MHz |
| Bit 6 | 27 | 1 | 48MHz |
| Bit 5 | - | X | FS0 |
| Bit 4 | 22 | 1 | PCICLK10 |
| Bit 3 | 21 | 1 | PCICLK9 |
| Bit 2 | 20 | 1 | PCICLK8 |
| Bit 1 | - | 1 | (Reserved) |
| Bit 0 | - | 1 | (Reserved) |

Note:

1. Inactive means outputs are held LOW and are disabled from switching.

Byte 5: Active/Inactive Register
(1 = enable, 0 = disable)

| Bit | Pin # | PWD | Description |
|------|-------|-----|-----------------|
| Bit7 | - | 0 | Reserved (Note) |
| Bit6 | - | 0 | Reserved (Note) |
| Bit5 | - | 0 | Reserved (Note) |
| Bit4 | - | 0 | Reserved (Note) |
| Bit3 | - | 0 | Reserved (Note) |
| Bit2 | - | 1 | Reserved (Note) |
| Bit1 | - | 1 | Reserved (Note) |
| Bit0 | - | 0 | Reserved (Note) |

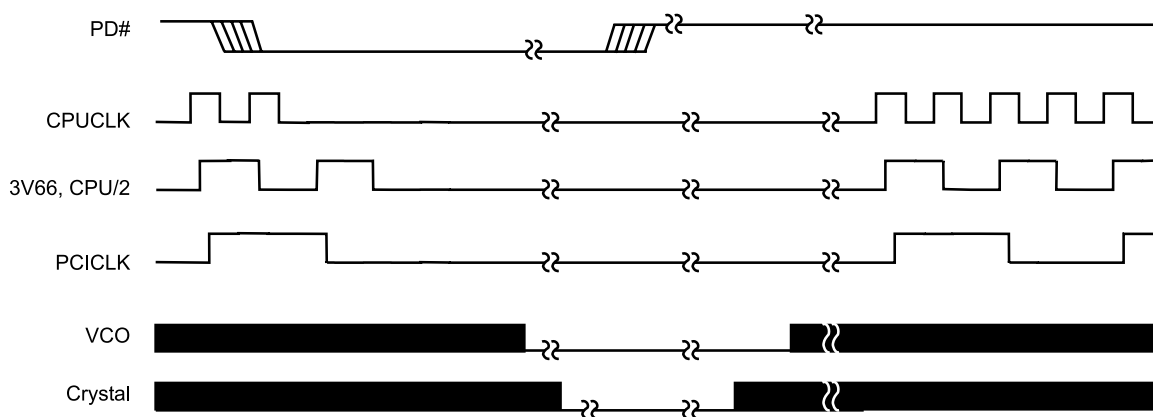
Note: Don't write into this register, writing into this register can cause malfunction



PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



Absolute Maximum Ratings

| | |
|-------------------------------------|-------------------------------------|
| Supply Voltage | 7.0 V |
| Logic Inputs | GND–0.5 V to V _{DD} +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | –65°C to +150°C |
| Case Temperature | 115°C |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70° C; V_{DD}, V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------|---------------------------------------------------------|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | | 0.1 | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | 2.0 | | μA |
| Input Low Current | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | -100 | | μA |
| Operating Supply Current | I _{DD3.3OP100} | C _L = 0 pF; Select @ 100 MHz | | 81 | 160 | mA |
| | I _{DD3.3OP133} | C _L = 0 pF; Select @ 133 MHz | | 85 | 160 | mA |
| Input frequency | F _i | V _{DD} = 3.3 V; | 11 | 14.318 | 16 | MHz |
| Input Capacitance ¹ | C _{IN} | Logic Inputs | | | 5 | pF |
| | C _{INX} | X1 & X2 pins | 27 | 36 | 45 | pF |
| Transition Time ¹ | T _{trans} | To 1st crossing of target Freq. | | | 3 | ms |
| Settling Time ¹ | T _s | From 1st crossing to 1% target Freq. | | 5 | 3 | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target Freq. | | | 3 | ms |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------|-------------------------|-----------------------------------------|-----|-----|-----|-------|
| Operating Supply Current | I _{DD2.5OP100} | C _L = 0 pF; Select @ 100 MHz | | 16 | 75 | mA |
| | I _{DD2.5OP133} | C _L = 0 pF; Select @ 133 MHz | | 19 | 90 | mA |
| Power Down Supply Current | I _{DD2.5PD} | C _L = 0 pF; PWRDWN# = 0 | | 0.1 | 100 | μA |

¹Guaranteed by design, not 100% tested in production.



Group Offset

| Group | Offset | Measurement Loads | Measure Points |
|---------------|----------------------|---------------------------|----------------------------|
| CPU to 3V66 | 0.0-1.5ns CPU leads | CPU @ 20pF, 3V66 @ 30pF | CPU @ 1.25V, 3V66 @ 1.5V |
| 3V66 to PCI | 1.5-4.0ns 3V66 leads | 3V66 @ 30pF, PCI @ 30pF | 3V66 @ 1.5V, PCI @ 1.5V |
| CPU to IOAPIC | 1.5-4.0ns CPU leads | CPU @ 20pF, IOAPIC @ 20pF | CPU @ 1.25V, IOAPIC @ 1.5V |

Note: 1. All offsets are to be measured at rising edges.

Electrical Characteristics - CPUCLK

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-------------------------------------|--------------------------------------------------|------|------|------|-------|
| Output High Voltage | V _{OH2B} | I _{OH} = -12.0 mA | 2 | 2.24 | | V |
| Output Low Voltage | V _{OL2B} | I _{OL} = 12.0 mA | | 0.31 | 0.4 | V |
| Output High Current | I _{OH2B} | V _{OH} = 1.7 V | | -31 | -19 | mA |
| Output Low Current | I _{OL2B} | V _{OL} = 0.7 V | 19 | 25 | | mA |
| Rise Time | t _{r2B} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.0 V | | 1.35 | 1.6 | ns |
| Fall Time | t _{f2B} ¹ | V _{OH} = 2.0 V, V _{OL} = 0.4 V | | 1.4 | 1.6 | ns |
| Duty Cycle | d _{t2B} ¹ | V _T = 1.25 V | 45 | 47 | 55 | % |
| Skew | t _{sk2B} ¹ | V _T = 1.25 V | | 63 | 175 | ps |
| Jitter, Cycle-to-cycle | t _{jcy-cyc2B} ¹ | V _T = 1.25 V | | 125 | 250 | ps |
| Jitter, One Sigma | t _{j1s2B} ¹ | V _T = 1.25 V | | 65 | 150 | ps |
| Jitter, Absolute | t _{jabs2B} ¹ | V _T = 1.25 V | -250 | 148 | +250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU/2

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|-------------------------------------|--------------------------------------------------|------|------|------|-------|
| Output High Voltage | V _{OH2B} | I _{OH} = -12.0 mA | 2 | 2.24 | | V |
| Output Low Voltage | V _{OL2B} | I _{OL} = 12.0 mA | | 0.31 | 0.4 | V |
| Output High Current | I _{OH2B} | V _{OH} = 1.7 V | | -31 | -19 | mA |
| Output Low Current | I _{OL2B} | V _{OL} = 0.7 V | 19 | 26 | | mA |
| Rise Time | t _{r2B} ¹ | V _{OL} = 0.4 V, V _{OH} = 2.0 V | | 1.2 | 1.6 | ns |
| Fall Time | t _{f2B} ¹ | V _{OH} = 2.0 V, V _{OL} = 0.4 V | | 1.2 | 1.6 | ns |
| Duty Cycle | d _{t2B} ¹ | V _T = 1.25 V | 45 | 49 | 55 | % |
| Jitter, Cycle-to-cycle | t _{jcy-cyc2B} ¹ | V _T = 1.25 V | | 125 | 250 | ps |
| Jitter, One Sigma | t _{j1s2B} ¹ | V _T = 1.25 V | | 50 | 150 | ps |
| Jitter, Absolute | t _{jabs2B} ¹ | V _T = 1.25 V | -250 | 97 | +250 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - 3V66

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-----------------------|--------------------------------------------------|------|------|-----|-------|
| Output High Voltage | V _{OH1} | I _{OH} = -11 mA | 2.4 | 3.1 | | V |
| Output Low Voltage | V _{OL1} | I _{OL} = 9.4 mA | | 0.17 | 0.4 | V |
| Output High Current | I _{OH1} | V _{OH} = 2.0 V | | -51 | -22 | mA |
| Output Low Current | I _{OL1} | V _{OL} = 0.8 V | 16 | 41 | | mA |
| Rise Time ¹ | t _{r1} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.5 | 1.8 | 2 | ns |
| Fall Time ¹ | t _{f1} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.5 | 1.6 | 2 | ns |
| Duty Cycle ¹ | d _{t1} | V _T = 1.5 V | 45 | 49 | 55 | % |
| Skew ¹ | t _{sk1} | V _T = 1.5 V | | 50 | 250 | ps |
| Jitter, Cycle-to-cycle ¹ | T _{jvc-cvc1} | V _T = 1.5 V | | 299 | 500 | ps |
| Jitter, One Sigma ¹ | t _{j1s1} | V _T = 1.5 V | | 87 | 150 | ps |
| Jitter, Absolute ¹ | t _{jabs1} | V _T = 1.5 V | -500 | 235 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-----------------------|--------------------------------------------------|------|------|-----|-------|
| Output High Voltage | V _{OH1} | I _{OH} = -11 mA | 2.4 | 3.1 | | V |
| Output Low Voltage | V _{OL1} | I _{OL} = 9.4 mA | | 0.16 | 0.4 | V |
| Output High Current | I _{OH1} | V _{OH} = 2.0 V | | -50 | -22 | mA |
| Output Low Current | I _{OL1} | V _{OL} = 0.8 V | 16 | 42 | | mA |
| Rise Time ¹ | t _{r1} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | | 2 | 2 | ns |
| Fall Time ¹ | t _{f1} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | | 1.74 | 2 | ns |
| Duty Cycle ¹ | d _{t1} | V _T = 1.5 V | 45 | 49 | 55 | % |
| Skew ¹ | t _{sk1} | V _T = 1.5 V | | 290 | 500 | ps |
| Jitter, Cycle-to-cycle ¹ | T _{jvc-cvc1} | V _T = 1.5 V | | 290 | 500 | ps |
| Jitter, One Sigma ¹ | t _{j1s1} | V _T = 1.5 V | | 30 | 150 | ps |
| Jitter, Absolute ¹ | t _{jabs1} | V _T = 1.5 V | -250 | 121 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - 48 MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|--------------------------------------------------|-----|------|-----|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -16 \text{ mA}$ | 2.4 | 2.62 | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9 \text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0 \text{ V}$ | | -27 | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8 \text{ V}$ | 16 | 22 | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | | 2.1 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | | 2.2 | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5 \text{ V}$ | 45 | 51 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | $T_{jvc-cyc5}$ | $V_T = 1.5 \text{ V}$ | | 488 | 500 | ps |
| Jitter, One Sigma ¹ | t_{j1s5} | $V_T = 1.5 \text{ V}$ | | 0.29 | 3 | % |
| Jitter, Absolute ¹ | t_{jabs5} | $V_T = 1.5 \text{ V}$ | -5 | 1.05 | 5 | % |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise stated)

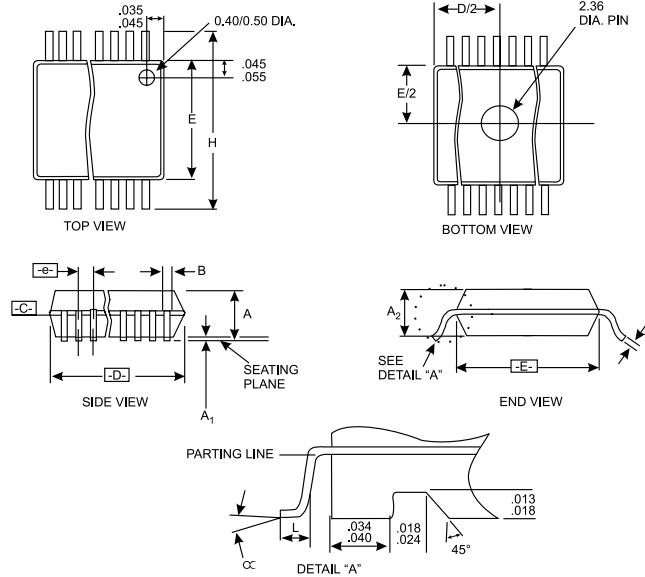
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|--------------------------------------------------|-----|------|------|-------|
| Output High Voltage | V_{OH5} | $I_{OH} = -16 \text{ mA}$ | 2.4 | 2.6 | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 9 \text{ mA}$ | | 0.3 | 0.4 | V |
| Output High Current | I_{OH5} | $V_{OH} = 2.0 \text{ V}$ | | -26 | -22 | mA |
| Output Low Current | I_{OL5} | $V_{OL} = 0.8 \text{ V}$ | 16 | 22 | | mA |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | | 2.2 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | | 2.2 | 4 | ns |
| Duty Cycle ¹ | d_{t5} | $V_T = 1.5 \text{ V}$ | 45 | 52 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | $T_{jvc-cyc5}$ | $V_T = 1.5 \text{ V}$ | | 600 | 1000 | ps |
| Jitter, One Sigma ¹ | t_{j1s5} | $V_T = 1.5 \text{ V}$ | | 0.44 | 3 | % |
| Jitter, Absolute ¹ | t_{jabs5} | $V_T = 1.5 \text{ V}$ | -5 | 0.94 | 5 | % |

¹Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - IOAPIC** $T_A = 0 - 70^\circ \text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$, $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-----------------|-----------------------------------------------------|------|------|-----|-------|
| Output High Voltage | V_{OH4B} | $I_{OH} = -12.0 \text{ mA}$ | 2 | 2.24 | | V |
| Output Low Voltage | V_{OL4B} | $I_{OL} = 12.0 \text{ mA}$ | | 0.31 | 0.4 | V |
| Output High Current | I_{OH4B} | $V_{OH} = 1.7 \text{ V}$ | | -31 | -19 | mA |
| Output Low Current | I_{OL4B} | $V_{OL} = 0.7 \text{ V}$ | 19 | 26 | | mA |
| Rise Time ¹ | T_{r4B} | $V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.0 \text{ V}$ | | 1.46 | 2 | ns |
| Fall Time ¹ | T_{f4B} | $V_{OH} = 2.0 \text{ V}$, $V_{OL} = 0.4 \text{ V}$ | | 1.44 | 2 | ns |
| Duty Cycle ¹ | D_{t4B} | $V_T = 1.25 \text{ V}$ | 45 | 49 | 55 | % |
| Skew ¹ | t_{sk4B} | $V_T = 1.25 \text{ V}$ | | 139 | 250 | ps |
| Jitter, Cycle-to-cycle ¹ | $T_{jcc-cyc4B}$ | $V_T = 1.25 \text{ V}$ | | 167 | 500 | ps |
| Jitter, One Sigma ¹ | T_{j1s4B} | $V_T = 1.25 \text{ V}$ | | 30 | 150 | ps |
| Jitter, Absolute ¹ | T_{jabs4B} | $V_T = 1.25 \text{ V}$ | -250 | 104 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



SSOP Package

| SYMBOL | COMMON DIMENSIONS | | | VARIATIONS | D | | | N |
|--------|-------------------|------|-------|------------|------|------|------|----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .095 | .101 | .110 | AC | .620 | .625 | .630 | 48 |
| A1 | .008 | .012 | .016 | | | | | |
| A2 | .088 | .090 | .092 | | | | | |
| B | .008 | .010 | .0135 | | | | | |
| C | .005 | - | .010 | | | | | |
| D | See Variations | | | | | | | |
| E | .292 | .296 | .299 | | | | | |
| e | 0.025 BSC | | | | | | | |
| H | .400 | .406 | .410 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .024 | .032 | .040 | | | | | |
| N | See Variations | | | | | | | |
| ∞ | 0° | 5° | 8° | | | | | |
| X | .085 | .093 | .100 | | | | | |

Ordering Information

ICS9248yF-77

Example:

ICS XXXX y F - PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type

F=SSOP

Revision Designator

Device Type (consists of 3 or 4 digit numbers)

Prefix

ICS, AV = Standard Device