Integrated Circuit Systems, Inc.

ICS9250-16

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:

810/810E type chipset.

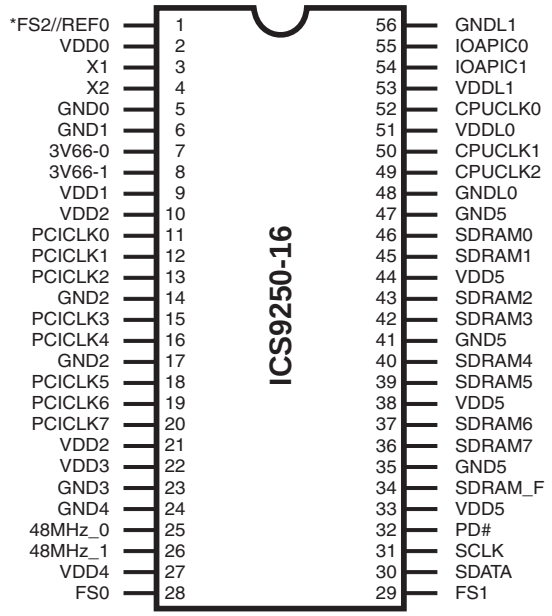
Output Features:

- 3 CPU (2.5V) 66.6/133.3MHz (up to 150MHz achievable through I^2C)
- 9 SDRAM (3.3V) @ 133.3MHz (up to 150MHz achievable through I^2C)
- 8 PCI (3.3 V) @33.3MHz
- 2 IOAPIC (2.5V) @ 33.3MHz
- 2 Hublink clocks (3.3 V) @ 66.6MHz
- 2 USB (3.3V) @ 48MHz (Non spread spectrum)
- 1 REF (3.3V) @ 14.318MHz

Features:

- Supports spread spectrum modulation, down spread 0 to -0.5% and ± 0.25% center spread.
- I^2C support for power management
- Efficient power management scheme through PD#
- Uses external 14.138MHz crystal
- Alternate frequency selections available through I^2C control.

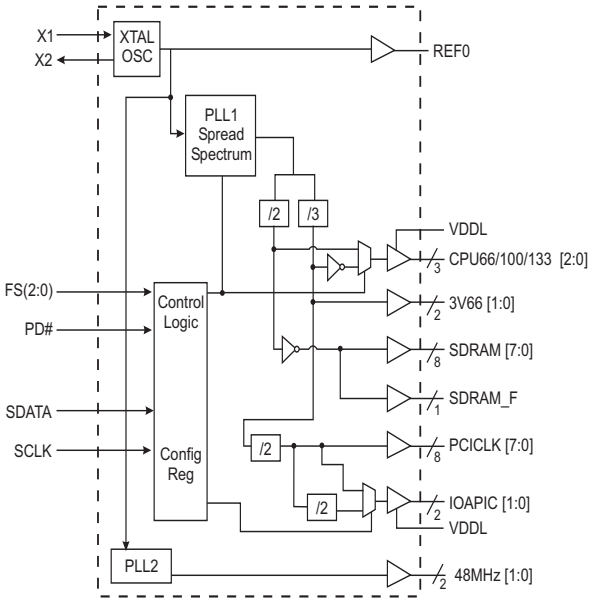
Pin Configuration



56-Pin 300mil SSOP

* This input has a 50KΩ pull-down to GND.

Block Diagram



Functionality

FS2	FS1	FS0	Function
X	0	0	Tristate
X	0	1	Test
0	1	0	Active CPU = 66MHz SDRAM = 100MHz
0	1	1	Active CPU = 100MHz SDRAM = 100MHz
1	1	1	Active CPU = 133MHz SDRAM = 100MHz
1	1	0	(Special Condition) Active CPU = 133MHz SDRAM = 133MHz

General Description

The **ICS9250-16** is a single chip clock solution for 810/810E type chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-16 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

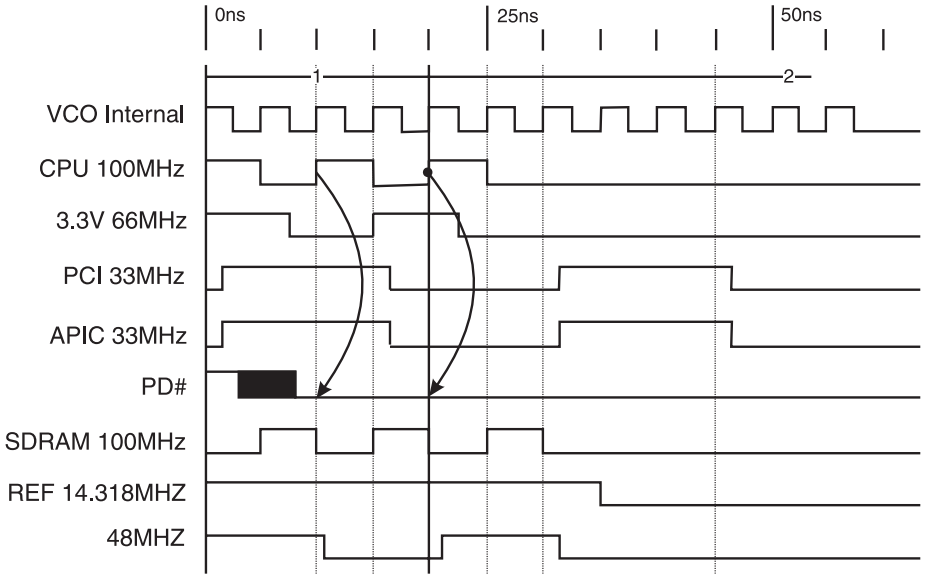
Power Groups

VDD0, GND0 = REF & Crystal
VDD1, GND1 = 3V66 (0:1)
VDD2, GND2 = PCICLK(0:7)
VDD3, GND3 = PLL core
VDD4, GND4 = 48MHz (0:1)
VDD5, GND5 = SDRAM_F, SDRAM (0:7)
VDDL0, GNDL0 = CPUCLK (0:2)
VDDL1, GNDL1 = IOAPIC (0:1)

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FS2	IN	Function Select pin. Determines CPU frequency, all output functionality (with 50KΩ pull-down).
	REF0	OUT	3.3V, 14.318MHz reference clock output.
3	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
5, 6, 14, 17, 23, 24, 35, 41, 47	GND (0:5)	PWR	Ground pins for 3.3V supply
8, 7	3V66 [1:0]	OUT	3.3V Fixed 66MHz clock outputs for HUB
2, 9, 10, 21, 22, 27, 33, 38, 44	VDD (0:5)	PWR	3.3V power supply
20,19,18,16, 15,13,12,11	PCICLK[7:0]	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
25, 26	48MHz (0:1)	OUT	3.3V Fixed 48MHz clock outputs for USB
28, 29	FS (0:1)	IN	Function Select pins. Determines CPU frequency, all output functionality. Please refer to Functionality table on page 3.
30	SDATA	IN	Data input for I^2C serial input.
31	SCLK	IN	Clock input of I^2C input
32	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
36, 37, 39, 40, 42, 43, 45, 46	SDRAM [7:0]	OUT	3.3V output running 100MHz. All SDRAM outputs can be turned off through I^2C
34	SDRAM_F	OUT	3.3V free running 100MHz SDRAM, cannot be turned off through I^2C
56,48	GNDL [1:0]	PWR	Ground for 2.5V power supply for CPU & APIC
49,50,52	CPUCLK [2:0]	OUT	2.5V Host bus clock output. 66MHz, 100MHz or 133MHz depending on FS (0:2) pins.
51, 53	VDDL (0:1)	PWR	2.5V power supply for CPU & IOAPIC
54, 55	IOAPIC [1:0]	OUT	2.5V clock outputs running at 33.3MHz.

Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz

Maximum Allowed Current

810E Condition	Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 2.625V All static inputs = Vddq3 or GND	Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 3.465V All static inputs = Vddq3 or GND
Powerdown Mode (PWRDWN# = 0	10mA	10mA
Full Active 66MHz SEL1, 0 = 10	70mA	310mA
Full Active 100MHz SEL1, 0 = 11	100mA	300mA

Clock Enable Configuration

PD#	CPUCLK	SDRAM	IOAPIC	66MHz	PCICLK	REF, 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Byte 5: ICS Reserved Functionality and frequency select register (Default as noted in PWD)

Bit	Desctiption								PWD
Bit7	ICS RESERVED BIT (Needs to be 0 clock to operate normal)								0
Bit6	ICS RESERVED BIT (Needs to be 0 clock to operate normal)								0
Bit5	ICS RESERVED BIT (Needs to be 0 clock to operate normal)								0
Bit (3,0)	Bit (3,0)				CPUCLK MHz	SDRAM MHz	3V66 MHz	PCICLK MHz	XXXX Note 1
	FS2 (HW)	FS0 (HW)	SEL1 (Bit3)	SEL0 (Bit0)					
	0	0	0	0	66.67	100.00	66.60	33.30	
	0	0	0	1	70.00	105.00	70.00	35.00	
	0	0	1	0	72.67	109.00	72.67	36.33	
	0	0	1	1	74.67	112.00	74.66	37.33	
	0	1	0	0	100.00	100.00	66.60	33.30	
	0	1	0	1	105.00	105.00	70.00	35.00	
	0	1	1	0	109.00	109.00	72.67	36.33	
	0	1	1	1	112.01	112.00	74.66	37.33	
	1	0	0	0	133.34	133.34	88.66	44.33	
	1	0	0	1	140.00	105.00	70.00	35.00	
	1	0	1	0	120.00	90.00	60.00	30.00	
	1	0	1	1	124.00	124.00	82.66	41.33	
	1	1	0	0	133.34	100.00	66.60	33.30	
	1	1	0	1	150.00	150.00	75.00	37.50	
	1	1	1	0	140.00	140.00	70.00	35.00	
	1	1	1	1	132.99	132.99	66.60	33.30	
Bit4	0 = Down Spread Spread Spectrum 0 to -.5% 1 = Center Spread Spread Spectrum ± .25%								0
Bit2	Not used (Needs to be 1 for normal clock operation)								1
Bit1	Not used (Needs to be 1 for normal clock operation)								1

Note1: Default at power-up will be for Bit 3 and Bit 0 to be 00, with external hardware selection of FS0, FS2 defining specific frequency.

Byte 0: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7		Reserved ID	0	(Active/Inactive)
Bit 6		Reserved ID	0	(Active/Inactive)
Bit 5		Reserved ID	0	(Active/Inactive)
Bit 4		Reserved ID	1	(Active/Inactive)
Bit 3		SpreadSpectrum (1=On/0=Off)	1	(Active/Inactive)
Bit 2	26	48MHz 1	1	(Active/Inactive)
Bit 1	25	48MHz 0	1	(Active/Inactive)
Bit 0	49	CPUCLK2	1	(Active/Inactive)

Notes:
1. **Do not write in ID bits, these bits are for ICS internal use only.**
2. Bit 0 will always read back 0. If readback/rewrite procedure is to perform, user will need to ensure a "1" is written to Bit 0 for CPUCLK2 to maintain running status.

Byte 1: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	36	SDRAM7	1	(Active/Inactive)
Bit 6	37	SDRAM6	1	(Active/Inactive)
Bit 5	39	SDRAM5	1	(Active/Inactive)
Bit 4	40	SDRAM4	1	(Active/Inactive)
Bit 3	42	SDRAM3	1	(Active/Inactive)
Bit 2	43	SDRAM2	1	(Active/Inactive)
Bit 1	45	SDRAM1	1	(Active/Inactive)
Bit 0	46	SDRAM0	1	(Active/Inactive)

Byte 2: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	20	PCICLK7	1	(Active/Inactive)
Bit 6	19	PCICLK6	1	(Active/Inactive)
Bit 5	18	PCICLK5	1	(Active/Inactive)
Bit 4	16	PCICLK4	1	(Active/Inactive)
Bit 3	15	PCICLK3	1	(Active/Inactive)
Bit 2	13	PCICLK2	1	(Active/Inactive)
Bit 1	12	PCICLK1	1	(Active/Inactive)
Bit 0	-	Reserved	1	(Active/Inactive)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Byte 3: Reserved Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	Reserved	0	(Active/Inactive)
Bit 6	-	Reserved	0	(Active/Inactive)
Bit 5	-	Reserved	0	(Active/Inactive)
Bit 4	-	Reserved	0	(Active/Inactive)
Bit 3	-	Reserved	0	(Active/Inactive)
Bit 2	-	Reserved	0	(Active/Inactive)
Bit 1	-	Reserved	0	(Active/Inactive)
Bit 0	-	Reserved	0	(Active/Inactive)

Byte 4: Reserved Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	Reserved	0	(Active/Inactive)
Bit 6	-	Reserved	0	(Active/Inactive)
Bit 5	-	Reserved	0	(Active/Inactive)
Bit 4	-	Reserved	0	(Active/Inactive)
Bit 3	-	Reserved	0	(Active/Inactive)
Bit 2	-	Reserved	0	(Active/Inactive)
Bit 1	-	Reserved	0	(Active/Inactive)
Bit 0	-	Reserved	0	(Active/Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Absolute Maximum Ratings

Core Supply Voltage ..... 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2		µA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66 MHz		97	110	mA
		C_L = 0 pF; Select @ 100 MHz		91	105	
		C_L = 0 pF; Select @ 133 MHz		100	130	
		C_L = Max loads; Select @ 66 MHz		275	310	mA
		C_L = Max loads; Select @ 100 MHz		267	300	
		C_L = Max loads; Select @ 133 MHz		278	350	
	$I_{DD2.5OP}$	C_L = 0 pF; Select @ 66 MHz		8	10	mA
		C_L = 0 pF; Select @ 100 MHz		11	15	
		C_L = 0 pF; Select @ 133 MHz		13	20	
		C_L = Max loads; Select @ 66 MHz		22	70	mA
		C_L = Max loads; Select @ 100 MHz		31	100	
		C_L = Max loads; Select @ 133 MHz		37	130	
Powerdown Current	$I_{DD3.3PD}$	C_L = Max loads		220	400	µA
	$I_{DD.25PD}$	Input address VDD or GND		<1	10	
Input Frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Pin Inductance	L_{pin}			7		nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance		6		pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			5	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			5	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			5	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5	16	45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5	21	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH @ MIN}$ = 1.0 V	-27	-68		mA
		$V_{OH @ MAX}$ = 2.375 V		-9	-27	
Output Low Current	I_{OL2B}	$V_{OL @ MIN}$ = 1.2 V	27	54		mA
		$V_{OL @ MAX}$ = 0.3 V		11	30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.1	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.1	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V, 66, 100 MHz	45	49	55	
		V_T = 1.25 V, 133 MHz	40	48	55	%
Skew window[1]	t_{sk2B}	V_T = 1.25 V		65	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V		90	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1B}[1]	$V_O = V_{DD}*(0.5)$	12	14	55	Ω
Output Impedance	R_{DSN1B}[1]	$V_O = V_{DD}*(0.5)$	12	14.5	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	$V_{OH @ MIN}$ = 1.0 V	-33	-108		mA
		$V_{OH @ MAX}$ = 3.135 V		-9	-33	
Output Low Current	I_{OL1}	$V_{OL @ MIN}$ = 1.95 V	30	95		mA
		$V_{OL @ MAX}$ = 0.4 V		29	38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.2	1.6	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.2	1.6	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	49	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		65	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		120	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP4B}[1]	$V_O = V_{DD}*(0.5)$	9	16	30	Ω
Output Impedance	R_{DSN4B}[1]	$V_O = V_{DD}*(0.5)$	9	20	30	Ω
Output High Voltage	V_{OH4B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH4B}	$V_{OH @ MIN}$ = 1.0 V	-27	-68		mA
		$V_{OH @ MAX}$ = 2.375 V		-9	-27	
Output Low Current	I_{OL4B}	$V_{OL @ MIN}$ = 1.2 V	27	54		mA
		$V_{OL @ MAX}$ = 0.3 V		11	30	
Rise Time[1]	t_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.1	1.6	ns
Fall Time[1]	t_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.1	1.6	ns
Duty Cycle[1]	d_{t4B}	V_T = 1.25 V	45	49	55	%
Skew window[1]	t_{sk4B}	V_T = 1.25 V		81	250	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc4B}$	V_T = 1.25 V		150	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3B}[1]	$V_O = V_{DD}*(0.5)$	10	12	24	Ω
Output Impedance	R_{DSN3B}[1]	$V_O = V_{DD}*(0.5)$	10	15	24	Ω
Output High Current	I_{OH3}	$V_{OH @ MIN}$ = 2.0 V	-54	-92		mA
		$V_{OH @ MAX}$ = 3.135 V		-16	-46	
Output Low Current	I_{OL3}	$V_{OL @ MIN}$ = 1.0 V	54	68		mA
		$V_{OL @ MAX}$ = 0.4 V		29	53	
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1	1.6	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.5	1.6	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45	52	55	%
Skew window[1]	t_{sk3}	V_T = 1.5 V		85	250	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc3}$	V_T = 1.5 V, 66, 100 MHz		120	250	ps
		V_T = 1.5 V, 133 MHz		150	300	

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1B}[1]	$V_O = V_{DD}*(0.5)$	12	15	55	Ω
Output Impedance	R_{DSN1B}[1]	$V_O = V_{DD}*(0.5)$	12	15	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	$V_{OH @ MIN}$ = 1.0 V	-33	-106		mA
		$V_{OH @ MAX}$ = 3.135 V		-14	-33	
Output Low Current	I_{OL1}	$V_{OL @ MIN}$ = 1.95 V	30	94		mA
		$V_{OL @ MAX}$ = 0.4 V		29	38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.3	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.4	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	51	55	%
Skew window[1]	t_{sk1}	V_T = 1.5 V		250	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		150	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz_0 (Pin 25)

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5B}[1]	$V_O = V_{DD}*(0.5)$	20	29	60	Ω
Output Impedance	R_{DSN5B}[1]	$V_O = V_{DD}*(0.5)$	20	27	60	Ω
Output High Voltage	V_{OH15}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH5}	$V_{OH @ MIN}$ = 1.0 V	-29	-54		mA
		$V_{OH @ MAX}$ = 3.135 V		-11	-23	
Output Low Current	I_{OL5}	$V_{OL @ MIN}$ = 1.95 V	29	54		mA
		$V_{OL @ MAX}$ = 0.4 V		16	27	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.3	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.6	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	53	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, Fixed clocks		130	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, Ref clocks		465	1000	ps

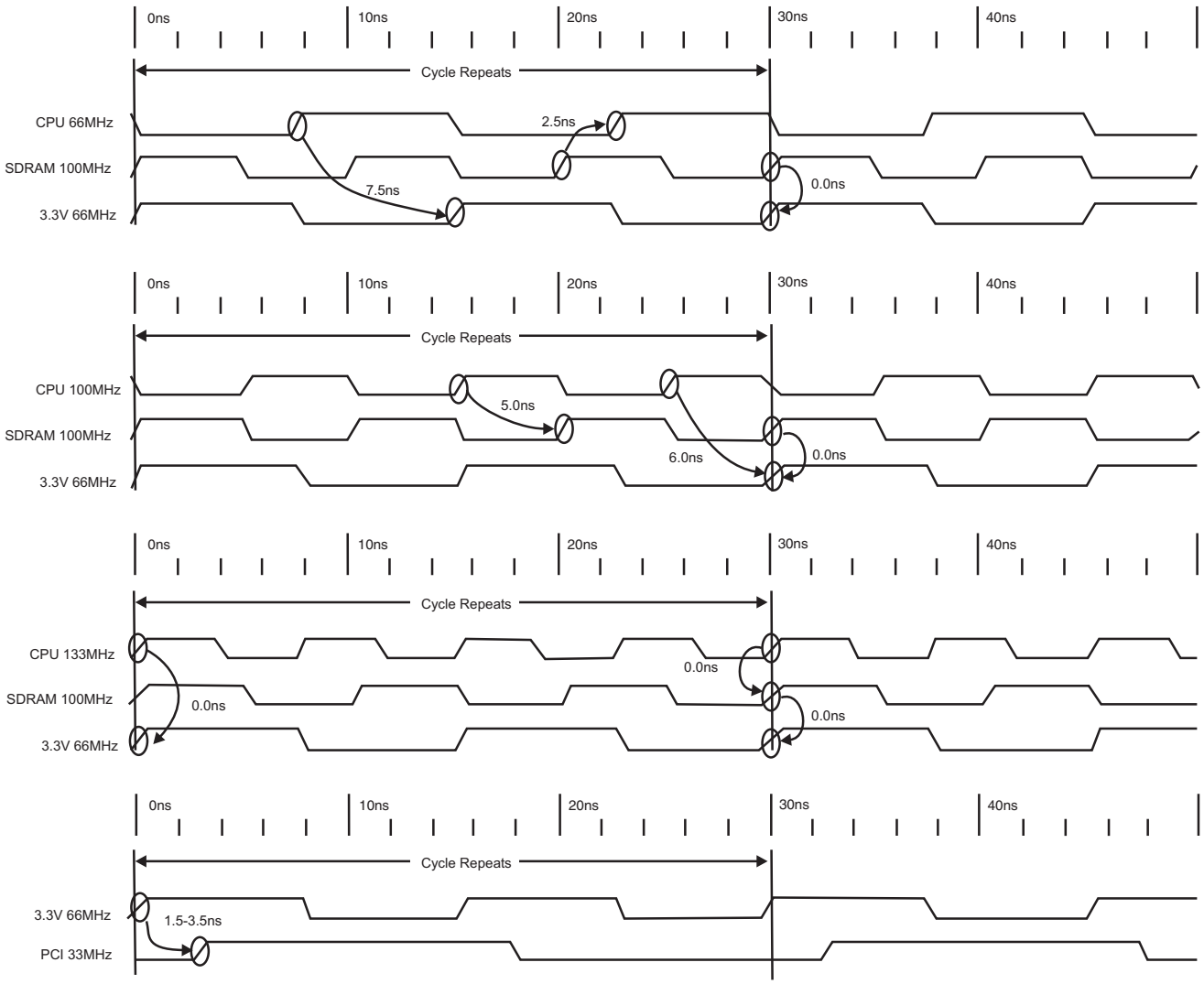
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz_1 (Pin 26)

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP3B}[1]	$V_O = V_{DD}*(0.5)$	10	15	24	Ω
Output Impedance	R_{DSN3B}[1]	$V_O = V_{DD}*(0.5)$	10	15	24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH3}	$V_{OH @ MIN}$ = 2.0 V	-54	-82		mA
		$V_{OH @ MAX}$ = 3.135 V		-20	-46	
Output Low Current	I_{OL3}	$V_{OL @ MIN}$ = 1.0 V	54	95		mA
		$V_{OL @ MAX}$ = 0.4 V		28	53	
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	1.1	1.6	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.3	1.6	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45	53	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc3B}$	V_T = 1.5 V		130	250	ps

[1]Guaranteed by design, not 100% tested in production.



Group Offset Waveforms

Group Skews (CPU = 66 MHz)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%
CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF
Refer to Group Offset Waveform diagram for definition of transition edges.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CPU to SDRAM Skew[1]	$T_{sk1\ CPU-SDRAM}$	CPU @ 1.25 V, SDRAM @ 1.5 V	-3	-2.6	-2	ns
Skew Window[1]	$T_{w1\ CPU-SDRAM}$		0	150	500	ps
CPU to 3V66 Skew[1]	$T_{sk1\ CPU-3V66}$	CPU @ 1.25 V, 3V66 @ 1.5 V	7	7.2	8	ns
Skew Window[1]	$T_{w1\ CPU-3V66}$		0	130	500	ps
SDRAM to 3V66 Skew[1]	$T_{sk1\ SDRAM-3V66}$	SDRAM, 3V66 @ 1.5 V	-500	100	500	ps
Skew Window[1]	$T_{w1\ SDRAM-3V66}$		0	155	500	ps
3V66 to PCI Skew[1]	$T_{sk1\ 3V66-PCI}$	3V66, PCI @ 1.5 V	1.5	2.4	3.5	ns
Skew Window[1]	$T_{w1\ 3V66-PCI}$		0	275	500	ps
IOAPIC to PCI Skew[1]	$T_{sk1\ IOAPIC-PCI}$	IOAPIC @ 1.25 V, PCI @ 1.5 V	-1	-0.4	1	ns
Skew Window[1]	$T_{w1\ IOAPIC-PCI}$		0	0.25	1	ns

[1]Guaranteed by design, not 100% tested in production.

Group Skews (CPU = 100 MHz)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%
CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF
Refer to Group Offset Waveform diagram for definition of transition edges.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CPU to SDRAM Skew[1]	$T_{sk2\ CPU-SDRAM}$	CPU @ 1.25 V, SDRAM @ 1.5 V	4.5	4.9	5.5	ns
Skew Window[1]	$T_{w2\ CPU-SDRAM}$		0	140	500	ps
CPU to 3V66 Skew[1]	$T_{sk2\ CPU-3V66}$	CPU @ 1.25 V, 3V66 @ 1.5 V	4.5	4.8	5.5	ns
Skew Window[1]	$T_{w2\ CPU-3V66}$		0	150	500	ps
SDRAM to 3V66 Skew[1]	$T_{sk2\ SDRAM-3V66}$	SDRAM, 3V66 @ 1.5 V	-500	100	500	ps
Skew Window[1]	$T_{w2\ SDRAM-3V66}$		0	155	500	ps
3V66 to PCI Skew[1]	$T_{sk2\ 3V66-PCI}$	3V66, PCI @ 1.5 V	1.5	2.4	3.5	ns
Skew Window[1]	$T_{w2\ 3V66-PCI}$		0	275	500	ps
IOAPIC to PCI Skew[1]	$T_{sk2\ IOAPIC-PCI}$	IOAPIC @ 1.25 V, PCI @ 1.5 V	-1	-0.4	1	ns
Skew Window[1]	$T_{w2\ IOAPIC-PCI}$		0	0.25	1	ns

[1]Guaranteed by design, not 100% tested in production.

[1]Guaranteed by design, not 100% tested in production.

Group Skews (CPU = 133 MHz)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%
CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF
Refer to Group Offset Waveform diagram for definition of transition edges.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CPU to SDRAM Skew[1]	$T_{sk3\ CPU-SDRAM}$	CPU @ 1.25 V, SDRAM @ 1.5 V	-500	70	500	ps
Skew Window[1]	$T_{w3\ CPU-SDRAM}$		0	125	500	ps
CPU to 3V66 Skew[1]	$T_{sk3\ CPU-3V66}$	CPU @ 1.25 V, 3V66 @ 1.5 V	-500	-145	500	ps
Skew Window[1]	$T_{w3\ CPU-3V66}$		0	220	500	ps
SDRAM to 3V66 Skew[1]	$T_{sk3\ SDRAM-3V66}$	SDRAM, 3V66 @ 1.5 V	-500	100	500	ps
Skew Window[1]	$T_{w3\ SDRAM-3V66}$		0	155	500	ps
3V66 to PCI Skew[1]	$T_{sk3\ 3V66-PCI}$	3V66, PCI @ 1.5 V	1.5	2.4	3.5	ns
Skew Window[1]	$T_{w3\ 3V66-PCI}$		0	275	500	ps
IOAPIC to PCI Skew[1]	$T_{sk3\ IOAPIC-PCI}$	IOAPIC @ 1.25 V, PCI @ 1.5 V	-1	-0.4	1	ns
Skew Window[1]	$T_{w3\ IOAPIC-PCI}$		0	0.25	1	ns

[1]Guaranteed by design, not 100% tested in production.

General Layout Precautions:

1) Use a ground plane on the top routing layer of the PCB in all areas not used by traces.

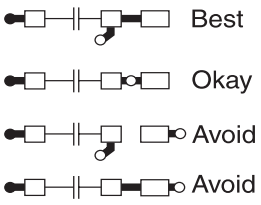
2) Make all power traces and ground traces as wide as the via pad for lower inductance.

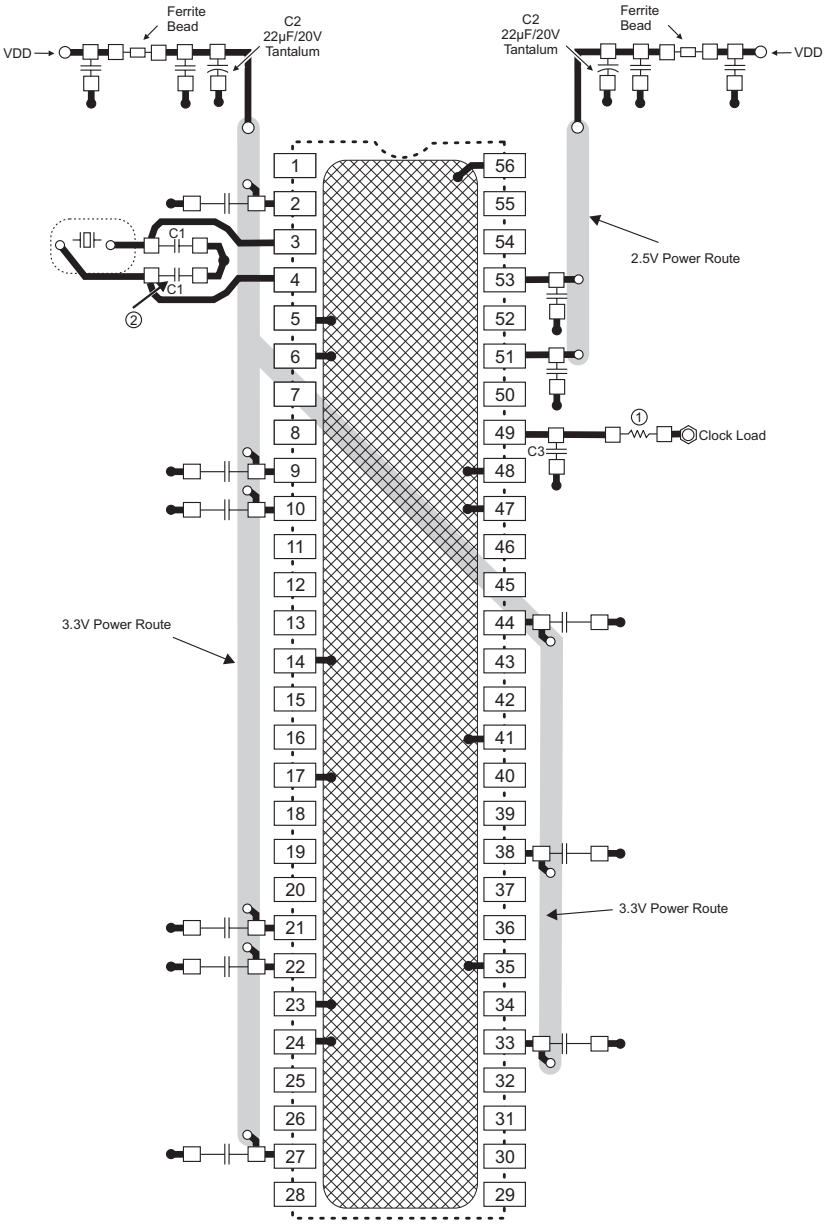
Notes:

① All clock outputs should have provisions for a 15pf capacitor between the clock output and series terminating resistor. Not shown in all places to improve readability of diagram.

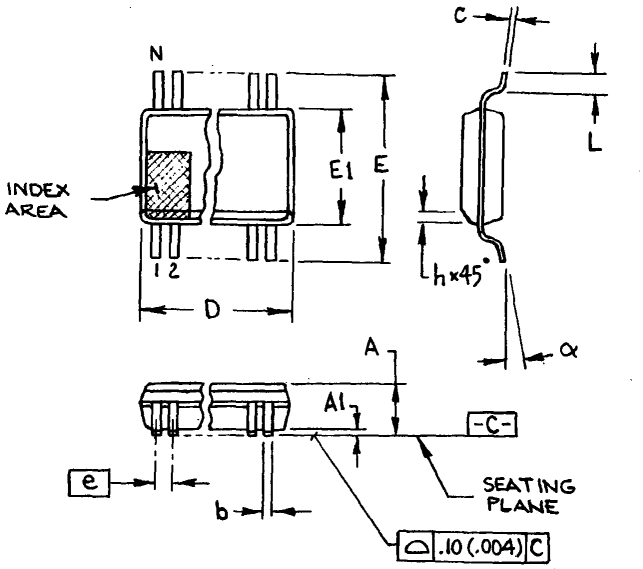
② Optional crystal load capacitors are recommended. They should be included in the layout but not inserted unless needed.

Connections to VDD:





= Routed Power
= Ground Connection Key (component side copper)
= Ground Plane Connection
= Power Route Connection
= Solder Pads
= Clock Load



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.398	9.652	.370	.380
34	11.303	11.557	.445	.455
48	15.748	16.002	.620	.630
56	18.288	18.542	.720	.730
64	20.828	21.082	.820	.830

JEDEC MO-118 6/1/00
DOC# 10-0034 REVB

Ordering Information

ICS9250yF-16-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device