

**Frequency Generator & Integrated Buffers for Celeron & PII/III™**

**Recommended Application:**

810/810E type chipset. Provides three CPU speeds (66.6, 100, 133MHz) with SDRAM = 133.3MHz.

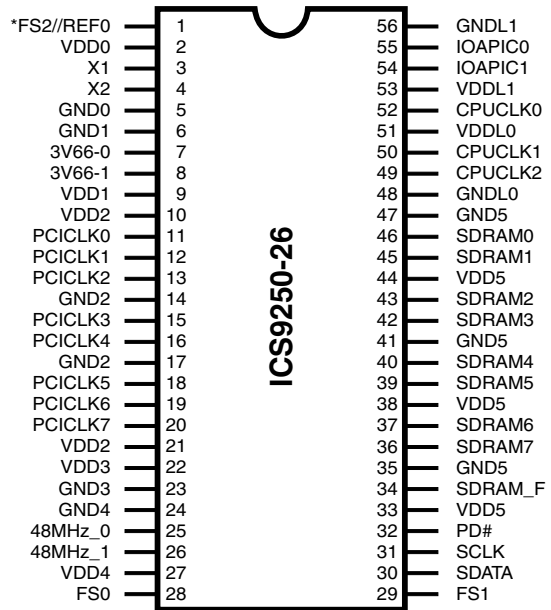
**Output Features:**

- 3 CPU (2.5V) 66.6/133.3MHz (up to 150MHz achievable through I<sup>2</sup>C)
- 9 SDRAM (3.3V) @ 133.3MHz (up to 150MHz achievable through I<sup>2</sup>C)
- 8 PCI (3.3 V) @33.3MHz
- 2 IOAPIC (2.5V) @ 33.3 MHz
- 2 Hublink clocks (3.3 V) @ 66.6 MHz
- 2 USB (3.3V) @ 48 MHz ( Non spread spectrum)
- 1 REF (3.3V) @ 14.318 MHz

**Features:**

- Supports spread spectrum modulation , down spread 0 to -0.5% and ± 0.25% center spread.
- I<sup>2</sup>C support for power management
- Efficient power management scheme through PD#
- Uses external 14.138 MHz crystal
- Alternate frequency selections available through I<sup>2</sup>C control.

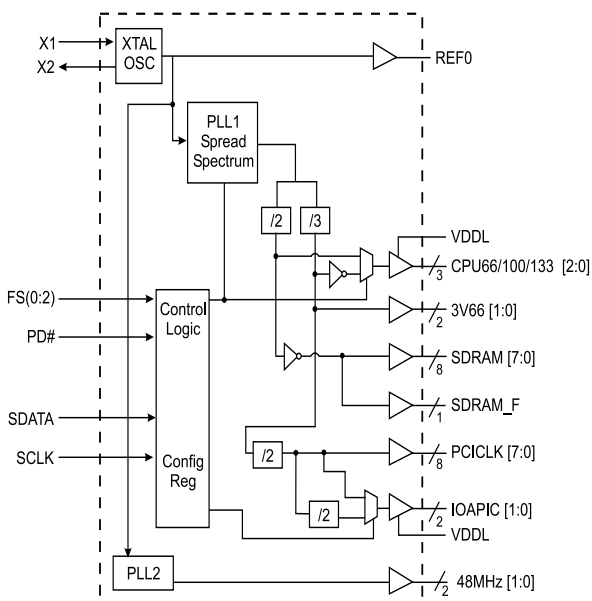
**Pin Configuration**



**56-Pin 300mil SSOP**

\* This input has a 120KΩ pull-down to GND.

**Block Diagram**



**Functionality**

| FS2 | FS1 | FS0 | Function   |
|-----|-----|-----|--|
| X   | 0   | 0   | Tristate   |
| X   | 0   | 1   | Test   |
| 0   | 1   | 0   | Active CPU = 66MHz<br>SDRAM = 100MHz                         |
| 0   | 1   | 1   | Active CPU = 100MHz<br>SDRAM = 100MHz                        |
| 1   | 1   | 1   | Active CPU = 133MHz<br>SDRAM = 100MHz                        |
| 1   | 1   | 0   | (Special Condition)<br>Active CPU = 133MHz<br>SDRAM = 133MHz |

# ICS9250-26



## General Description

The ICS9250-26 is a single chip clock solution for 810/810E type chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I<sup>2</sup>C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-26 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

## Pin Configuration

| PIN NUMBER                           | PIN NAME     | TYPE | DESCRIPTION   |
|--------------------------------------|--------------|------|---|
| 1                                    | FS2          | OUT  | Function Select pin. Determines CPU frequency, all output functionality (with 50Ω)  |
|                                      | REF0         | OUT  | 3.3V, 14.318MHz reference clock output.   |
| 3                                    | X1           | OUT  | Crystal input, has internal load cap (33pF) and feedback resistor from X2   |
| 4                                    | X2           | OUT  | Crystal output, nominally 14.318MHz. Has internal load cap (33pF)   |
| 47, 41, 35, 24, 23, 17, 14, 6, 5     | GND (5:0)    | PWR  | Ground pins for 3.3V supply   |
| 8, 7                                 | 3V66 [1:0]   | OUT  | 3.3V Fixed 66MHz clock outputs for HUB  |
| 44, 38, 33, 27, 22, 21, 10, 10, 9, 2 | VDD (5:0)    | PWR  | 3.3V power supply   |
| 20,19,18,16, 15,13,12,11             | PCICLK (7:0) | OUT  | 3.3V PCI clock outputs, with Synchronous CPUCLKS  |
| 26, 25                               | 48MHz (1:0)  | OUT  | 3.3V Fixed 48MHz clock outputs for USB  |
| 29, 28                               | FS (1:0)     | OUT  | Function Select pins. Determines CPU frequency, all output functionality. Please refer to Functionality table on page 3.  |
| 30                                   | SDATA        | IN   | Data input for I <sup>2</sup> C serial input.   |
| 31                                   | SCLK         | IN   | Clock input of I <sup>2</sup> C input   |
| 32                                   | PD#          | IN   | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 36, 37, 39, 40, 42, 43, 45, 46       | SDRAM (7:0)  | OUT  | 3.3V output running 100MHz. All SDRAM outputs can be turned off through I <sup>2</sup> C  |
| 34                                   | SDRAM_F      | OUT  | 3.3V free running 100MHz SDRAM not affected by I <sup>2</sup> C   |
| 56,48                                | GNDL (1:0)   | PWR  | Ground for 2.5V power supply for CPU & APIC   |
| 52, 50, 49                           | CPUCLK (2:0) | OUT  | 2.5V Host bus clock output. 66MHz or 100MHz 133MHz depending on FS pins   |
| 51, 53                               | VDDL (1:0)   | PWR  | 2.5V power supply for CPU & IOAPIC  |
| 54, 55                               | IOAPIC (1:0) | OUT  | 2.5V clock outputs running at 33.3MHz.  |



### Maximum Allowed Current

| <b>810E Condition</b>                     | Max 2.5V supply consumption<br>Max discrete cap loads,<br>Vddq2 = 2.625V<br>All static inputs = Vddq3 or GND | Max 2.5V supply consumption<br>Max discrete cap loads,<br>Vddq2 = 3.465V<br>All static inputs = Vddq3 or GND |
|---|--|--|
| <b>Powerdown Mode</b><br>(PWRDWN# = 0)    | 10mA   | 10mA   |
| <b>Full Active 66MHz</b><br>SEL1, 0 = 10  | 70mA   | 280mA  |
| <b>Full Active 100MHz</b><br>SEL1, 0 = 11 | 100mA  | 280mA  |

### Clock Enable Configuration

| PD# | CPUCLK | SDRAM | IOAPIC | 66MHz | PCICLK | REF,<br>48MHz | Osc | VCOs |
|-----|--------|-------|--------|-------|--------|---------------|-----|------|
| 0   | LOW    | LOW   | LOW    | LOW   | LOW    | LOW           | OFF | OFF  |
| 1   | ON     | ON    | ON     | ON    | ON     | ON            | ON  | ON   |

### Power Groups\*

VDD0, GND0 = REF & Crystal  
VDD1, GND1 = 3V66  
VDD2, GND2 = PCICLK  
VDD3, GND3 = PLL core  
VDD4, GND4 = 48MHz  
VDD5, GND5 = SDRAM\_F, SDRAM  
VDDL0, GNDL0 = CPUCLK  
VDDL1, GNDL1 = IOAPIC

\* To ensure the processor will power up to the desired frequency, the 3.3V supply to the ICS9250-26 needs to reach a stable condition before the 2.5V supply does. In most systems, the power up ramp of the 2.5V is slower than the 3.3V ramp. For those instances, no special requirements are necessary.



## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming.  
For more information, contact ICS for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

| How to Write:             |                      |
|---------------------------|----------------------|
| Controller (Host)         | ICS (Slave/Receiver) |
| Start Bit                 |                      |
| Address D2 <sub>(H)</sub> |                      |
|                           | <b>ACK</b>           |
| Dummy Command Code        |                      |
|                           | <b>ACK</b>           |
| Dummy Byte Count          |                      |
|                           | <b>ACK</b>           |
| Byte 0                    |                      |
|                           | <b>ACK</b>           |
| Byte 1                    |                      |
|                           | <b>ACK</b>           |
| Byte 2                    |                      |
|                           | <b>ACK</b>           |
| Byte 3                    |                      |
|                           | <b>ACK</b>           |
| Byte 4                    |                      |
|                           | <b>ACK</b>           |
| Byte 5                    |                      |
|                           | <b>ACK</b>           |
| Stop Bit                  |                      |

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read:              |                      |
|---------------------------|----------------------|
| Controller (Host)         | ICS (Slave/Receiver) |
| Start Bit                 |                      |
| Address D3 <sub>(H)</sub> |                      |
|                           | <b>ACK</b>           |
|                           | <b>Byte Count</b>    |
| ACK                       |                      |
|                           | <b>Byte 0</b>        |
| ACK                       |                      |
|                           | <b>Byte 1</b>        |
| ACK                       |                      |
|                           | <b>Byte 2</b>        |
| ACK                       |                      |
|                           | <b>Byte 3</b>        |
| ACK                       |                      |
|                           | <b>Byte 4</b>        |
| ACK                       |                      |
|                           | <b>Byte 5</b>        |
| ACK                       |                      |
| Stop Bit                  |                      |

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



**Byte 5: ICS Reserved Functionality and frequency select register (Default as noted in PWD)**

| Bit       | Description   |             |                |                |               |              |             |               | PWD            |
|-----------|---|-------------|----------------|----------------|---------------|--------------|-------------|---------------|----------------|
| Bit7      | ICS RESERVED BIT (Needs to be 0 clock to operate normal)                                  |             |                |                |               |              |             |               | 0              |
| Bit6      | ICS RESERVED BIT (Needs to be 0 clock to operate normal)                                  |             |                |                |               |              |             |               | 0              |
| Bit5      | ICS RESERVED BIT (Needs to be 0 clock to operate normal)                                  |             |                |                |               |              |             |               | 0              |
| Bit (3,0) | Bit (3,0)   |             |                |                | CPUCLK<br>MHz | SDRAM<br>MHz | 3V66<br>MHz | PCICLK<br>MHz | XXXX<br>Note 1 |
|           | FS2<br>(HW)   | FS0<br>(HW) | SEL1<br>(Bit3) | SEL0<br>(Bit0) |               |              |             |               |                |
|           | 0   | 0           | 0              | 0              | 66.67         | 100.00       | 66.60       | 33.30         |                |
|           | 0   | 0           | 0              | 1              | 70.00         | 105.00       | 70.00       | 35.00         |                |
|           | 0   | 0           | 1              | 0              | 72.67         | 109.00       | 72.67       | 36.33         |                |
|           | 0   | 0           | 1              | 1              | 74.67         | 112.00       | 74.66       | 37.33         |                |
|           | 0   | 1           | 0              | 0              | 100.00        | 100.00       | 66.60       | 33.30         |                |
|           | 0   | 1           | 0              | 1              | 105.00        | 105.00       | 70.00       | 35.00         |                |
|           | 0   | 1           | 1              | 0              | 109.00        | 109.00       | 72.67       | 36.33         |                |
|           | 0   | 1           | 1              | 1              | 112.01        | 112.00       | 74.66       | 37.33         |                |
|           | 1   | 0           | 0              | 0              | 133.34        | 133.34       | 88.66       | 44.33         |                |
|           | 1   | 0           | 0              | 1              | 140.00        | 105.00       | 70.00       | 35.00         |                |
|           | 1   | 0           | 1              | 0              | 120.00        | 90.00        | 60.00       | 30.00         |                |
|           | 1   | 0           | 1              | 1              | 124.00        | 124.00       | 82.66       | 41.33         |                |
|           | 1   | 1           | 0              | 0              | 133.34        | 100.00       | 66.60       | 33.30         |                |
|           | 1   | 1           | 0              | 1              | 150.00        | 150.00       | 75.00       | 37.50         |                |
| 1         | 1   | 1           | 0              | 140.00         | 140.00        | 70.00        | 35.00       |               |                |
| 1         | 1   | 1           | 1              | 132.99         | 132.99        | 66.60        | 33.30       |               |                |
| Bit4      | 0 = Down Spread Spread Spectrum 0 to -.5%<br>1 = Center Spread Spread Spectrum $\pm$ .25% |             |                |                |               |              |             |               | 0              |
| Bit2      | Not used (Needs to be 1 for normal clock operation)                                       |             |                |                |               |              |             |               | 1              |
| Bit1      | Not used (Needs to be 1 for normal clock operation)                                       |             |                |                |               |              |             |               | 1              |

**Note1:** Default at power-up will be for Bit 3 and Bit 0 to be 00, with external hardware selection of FS0, FS2 defining specific frequency.

# ICS9250-26



## Byte 0: Control Register (1 = enable, 0 = disable)

| Bit   | Pin# | Name                           | PWD | Description       |
|-------|------|--------------------------------|-----|-------------------|
| Bit 7 |      | Reserved ID                    | 0   | (Active/Inactive) |
| Bit 6 |      | Reserved ID                    | 0   | (Active/Inactive) |
| Bit 5 |      | Reserved ID                    | 0   | (Active/Inactive) |
| Bit 4 |      | Reserved ID                    | 1   | (Active/Inactive) |
| Bit 3 |      | SpreadSpectrum<br>(1=On/0=Off) | 1   | (Active/Inactive) |
| Bit 2 | 26   | 48MHz 1                        | 1   | (Active/Inactive) |
| Bit 1 | 25   | 48MHz 0                        | 1   | (Active/Inactive) |
| Bit 0 | 49   | CPUCLK2                        | 0   | (Active/Inactive) |

Note: Do not write in ID bits, these bits are for ICS internal use only.  
Must write a '1' in bit 0 after read back.

## Byte 1: Control Register (1 = enable, 0 = disable)

| Bit   | Pin# | Name   | PWD | Description       |
|-------|------|--------|-----|-------------------|
| Bit 7 | 36   | SDRAM7 | 1   | (Active/Inactive) |
| Bit 6 | 37   | SDRAM6 | 1   | (Active/Inactive) |
| Bit 5 | 39   | SDRAM5 | 1   | (Active/Inactive) |
| Bit 4 | 40   | SDRAM4 | 1   | (Active/Inactive) |
| Bit 3 | 42   | SDRAM3 | 1   | (Active/Inactive) |
| Bit 2 | 43   | SDRAM2 | 1   | (Active/Inactive) |
| Bit 1 | 45   | SDRAM1 | 1   | (Active/Inactive) |
| Bit 0 | 46   | SDRAM0 | 1   | (Active/Inactive) |

## Byte 2: Control Register (1 = enable, 0 = disable)

| Bit   | Pin# | Name     | PWD | Description       |
|-------|------|----------|-----|-------------------|
| Bit 7 | 20   | PCICLK7  | 1   | (Active/Inactive) |
| Bit 6 | 19   | PCICLK6  | 1   | (Active/Inactive) |
| Bit 5 | 18   | PCICLK5  | 1   | (Active/Inactive) |
| Bit 4 | 16   | PCICLK4  | 1   | (Active/Inactive) |
| Bit 3 | 15   | PCICLK3  | 1   | (Active/Inactive) |
| Bit 2 | 13   | PCICLK2  | 1   | (Active/Inactive) |
| Bit 1 | 12   | PCICLK1  | 1   | (Active/Inactive) |
| Bit 0 | -    | Reserved | 1   | (Active/Inactive) |

### Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default



**Byte 3: Reserved Register**  
(1 = enable, 0 = disable)

| Bit   | Pin# | Name     | PWD | Description       |
|-------|------|----------|-----|-------------------|
| Bit 7 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 6 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 5 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 4 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 3 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 2 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 1 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 0 | -    | Reserved | 0   | (Active/Inactive) |

**Byte 4: Reserved Register**  
(1 = enable, 0 = disable)

| Bit   | Pin# | Name     | PWD | Description       |
|-------|------|----------|-----|-------------------|
| Bit 7 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 6 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 5 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 4 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 3 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 2 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 1 | -    | Reserved | 0   | (Active/Inactive) |
| Bit 0 | -    | Reserved | 0   | (Active/Inactive) |

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default



## Absolute Maximum Ratings

|                               |                                      |
|-------------------------------|--------------------------------------|
| Core Supply Voltage           | 4.6 V                                |
| I/O Supply Voltage            | 3.6V                                 |
| Logic Inputs                  | GND -0.5 V to V <sub>DD</sub> +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C                         |
| Storage Temperature           | -65°C to +150°C                      |
| Case Temperature              | 115°C                                |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Paramete

T<sub>A</sub> = 0 - 70C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER                                    | SYMBOL                | CONDITIONS  | MIN                  | TYP    | MAX                  | UNITS |    |
|--|-----------------------|---|----------------------|--------|----------------------|-------|----|
| Input High Voltage                           | V <sub>IH</sub>       |   | 2                    |        | V <sub>DD</sub> +0.3 | V     |    |
| Input Low Voltage                            | V <sub>IL</sub>       |   | V <sub>SS</sub> -0.3 |        | 0.8                  | V     |    |
| Input High Current                           | I <sub>IH</sub>       | V <sub>IN</sub> = V <sub>DD</sub>                       | -5                   |        | 5                    | μA    |    |
| Input Low Current                            | I <sub>IL1</sub>      | V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors | -5                   | 2      |                      | μA    |    |
|  | I <sub>IL2</sub>      | V <sub>IN</sub> = 0 V; Inputs with pull-up resistors    | -200                 | -100   |                      |       |    |
| Operating Supply Current                     | I <sub>DD3.3OP</sub>  | C <sub>L</sub> = 0 pF; Select @ 66 MHz                  |                      | 97     | 110                  | mA    |    |
|  |                       | C <sub>L</sub> = 0 pF; Select @ 100 MHz                 |                      | 91     | 105                  |       |    |
|  |                       | C <sub>L</sub> = 0 pF; Select @ 133 MHz                 |                      | 100    | 130                  |       |    |
|  |                       | C <sub>L</sub> = Max loads; Select @ 66 MHz             |                      | 275    | 310                  | mA    |    |
|  |                       | C <sub>L</sub> = Max loads; Select @ 100 MHz            |                      | 267    | 300                  |       |    |
|  |                       | C <sub>L</sub> = Max loads; Select @ 133 MHz            |                      | 278    | 350                  |       |    |
|  | I <sub>DD2.5OP</sub>  | C <sub>L</sub> = 0 pF; Select @ 66 MHz                  |                      |        | 8                    | 10    | mA |
|  |                       | C <sub>L</sub> = 0 pF; Select @ 100 MHz                 |                      |        | 11                   | 15    |    |
|  |                       | C <sub>L</sub> = 0 pF; Select @ 133 MHz                 |                      |        | 13                   | 20    |    |
|  |                       | C <sub>L</sub> = Max loads; Select @ 66 MHz             |                      |        | 22                   | 70    | mA |
| C <sub>L</sub> = Max loads; Select @ 100 MHz |                       |   |                      | 31     | 100                  |       |    |
| C <sub>L</sub> = Max loads; Select @ 133 MHz |                       |   | 37                   | 130    |                      |       |    |
| Powerdown Current                            | I <sub>DD3.3PD</sub>  | C <sub>L</sub> = Max loads                              |                      | 220    | 400                  | μA    |    |
|  | I <sub>DD2.5PD</sub>  | Input address V <sub>DD</sub> or GND                    |                      | <1     | 10                   |       |    |
| Input Frequency                              | F <sub>i</sub>        | V <sub>DD</sub> = 3.3 V                                 | 12                   | 14.318 | 16                   | MHz   |    |
| Pin Inductance                               | L <sub>pin</sub>      |   |                      | 7      |                      | nH    |    |
| Input Capacitance <sup>1</sup>               | C <sub>IN</sub>       | Logic Inputs  |                      |        | 5                    | pF    |    |
|  | C <sub>OUT</sub>      | Output pin capacitance                                  |                      | 6      |                      | pF    |    |
|  | C <sub>INX</sub>      | X1 & X2 pins  | 27                   |        | 45                   | pF    |    |
| Transition time <sup>1</sup>                 | T <sub>trans</sub>    | To 1st crossing of target frequency                     |                      |        | 5                    | ms    |    |
| Settling time <sup>1</sup>                   | T <sub>s</sub>        | From 1st crossing to 1% target frequency                |                      |        | 5                    | ms    |    |
| Clk Stabilization <sup>1</sup>               | T <sub>STAB</sub>     | From V <sub>DD</sub> = 3.3 V to 1% target frequency     |                      |        | 5                    | ms    |    |
| Delay <sup>1</sup>                           | t <sub>PZH,tPZL</sub> | Output enable delay (all outputs)                       | 1                    |        | 10                   | ns    |    |
|  | t <sub>PHZ,tPLZ</sub> | Output disable delay (all outputs)                      | 1                    |        | 10                   | ns    |    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.





### Electrical Characteristics - CPU

T<sub>A</sub> = 0 - 70C; V<sub>DDL</sub> = 2.5 V +/-5%; C<sub>L</sub> = 10-20 pF (unless otherwise specified)

| PARAMETER                           | SYMBOL                          | CONDITIONS                                       | MIN  | TYP | MAX | UNITS |
|-------------------------------------|---------------------------------|--|------|-----|-----|-------|
| Output Impedance                    | R <sub>DSP2B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 13.5 | 16  | 45  | Ω     |
| Output Impedance                    | R <sub>DSN2B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 13.5 | 21  | 45  | Ω     |
| Output High Voltage                 | V <sub>OH2B</sub>               | I <sub>OH</sub> = -1 mA                          | 2    |     |     | V     |
| Output Low Voltage                  | V <sub>OL2B</sub>               | I <sub>OL</sub> = 1 mA                           |      |     | 0.4 | V     |
| Output High Current                 | I <sub>OH2B</sub>               | V <sub>OH @ MIN</sub> = 1.0 V                    | -27  | -68 |     | mA    |
|                                     |                                 | V <sub>OH @ MAX</sub> = 2.375 V                  |      | -9  | -27 |       |
| Output Low Current                  | I <sub>OL2B</sub>               | V <sub>OL @ MIN</sub> = 1.2 V                    | 27   | 54  |     | mA    |
|                                     |                                 | V <sub>OL @ MAX</sub> = 0.3 V                    |      | 11  | 30  |       |
| Rise Time <sup>1</sup>              | t <sub>r2B</sub>                | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.0 V | 0.4  | 1.1 | 1.6 | ns    |
| Fall Time <sup>1</sup>              | t <sub>f2B</sub>                | V <sub>OH</sub> = 2.0 V, V <sub>OL</sub> = 0.4 V | 0.4  | 1.1 | 1.6 | ns    |
| Duty Cycle <sup>1</sup>             | d <sub>t2B</sub>                | V <sub>T</sub> = 1.25 V, 66, 100 MHz             | 45   | 49  | 55  | %     |
|                                     |                                 | V <sub>T</sub> = 1.25 V, 133 MHz                 | 40   | 48  | 55  |       |
| Skew window <sup>1</sup>            | t <sub>sk2B</sub>               | V <sub>T</sub> = 1.25 V                          |      | 65  | 175 | ps    |
| Jitter, Cycle-to-cycle <sup>1</sup> | t <sub>jyc-cyc2B</sub>          | V <sub>T</sub> = 1.25 V                          |      | 90  | 250 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - 3V66

T<sub>A</sub> = 0 - 70C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 10-20 pF (unless otherwise specified)

| PARAMETER                           | SYMBOL                          | CONDITIONS                                       | MIN | TYP  | MAX  | UNITS |
|-------------------------------------|---------------------------------|--|-----|------|------|-------|
| Output Impedance                    | R <sub>DSP1B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 12  | 14   | 55   | Ω     |
| Output Impedance                    | R <sub>DSN1B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 12  | 14.5 | 55   | Ω     |
| Output High Voltage                 | V <sub>OH1</sub>                | I <sub>OH</sub> = -1 mA                          | 2.4 |      |      | V     |
| Output Low Voltage                  | V <sub>OL1</sub>                | I <sub>OL</sub> = 1 mA                           |     |      | 0.55 | V     |
| Output High Current                 | I <sub>OH1</sub>                | V <sub>OH @ MIN</sub> = 1.0 V                    | -33 | -108 |      | mA    |
|                                     |                                 | V <sub>OH @ MAX</sub> = 3.135 V                  |     | -9   | -33  |       |
| Output Low Current                  | I <sub>OL1</sub>                | V <sub>OL @ MIN</sub> = 1.95 V                   | 30  | 95   |      | mA    |
|                                     |                                 | V <sub>OL @ MAX</sub> = 0.4 V                    |     | 29   | 38   |       |
| Rise Time <sup>1</sup>              | t <sub>r1</sub>                 | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V | 0.4 | 1.2  | 1.6  | ns    |
| Fall Time <sup>1</sup>              | t <sub>f1</sub>                 | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V | 0.4 | 1.2  | 1.6  | ns    |
| Duty Cycle <sup>1</sup>             | d <sub>t1</sub>                 | V <sub>T</sub> = 1.5 V                           | 45  | 49   | 55   | %     |
| Skew window <sup>1</sup>            | t <sub>sk1</sub>                | V <sub>T</sub> = 1.5 V                           |     | 65   | 175  | ps    |
| Jitter, Cycle-to-cycle <sup>1</sup> | t <sub>jyc-cyc1</sub>           | V <sub>T</sub> = 1.5 V                           |     | 120  | 500  | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - IOAPIC

T<sub>A</sub> = 0 - 70°C; V<sub>DDL</sub> = 2.5 V +/-5%; C<sub>L</sub> = 10-20 pF (unless otherwise specified)

| PARAMETER                           | SYMBOL                          | CONDITIONS                                       | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------------------------|--|-----|-----|-----|-------|
| Output Impedance                    | R <sub>DSP4B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> * (0.5)         | 9   | 16  | 30  | Ω     |
| Output Impedance                    | R <sub>DSN4B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> * (0.5)         | 9   | 20  | 30  | Ω     |
| Output High Voltage                 | V <sub>OH4B</sub>               | I <sub>OH</sub> = -1 mA                          | 2   |     |     | V     |
| Output Low Voltage                  | V <sub>OL4B</sub>               | I <sub>OL</sub> = 1 mA                           |     |     | 0.4 | V     |
| Output High Current                 | I <sub>OH4B</sub>               | V <sub>OH</sub> @ MIN = 1.0 V                    | -27 | -68 |     | mA    |
|                                     |                                 | V <sub>OH</sub> @ MAX = 2.375 V                  |     | -9  | -27 |       |
| Output Low Current                  | I <sub>OL4B</sub>               | V <sub>OL</sub> @ MIN = 1.2 V                    | 27  | 54  |     | mA    |
|                                     |                                 | V <sub>OL</sub> @ MAX = 0.3 V                    |     | 11  | 30  |       |
| Rise Time <sup>1</sup>              | t <sub>r4B</sub>                | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.0 V | 0.4 | 1.1 | 1.6 | ns    |
| Fall Time <sup>1</sup>              | t <sub>f4B</sub>                | V <sub>OH</sub> = 2.0 V, V <sub>OL</sub> = 0.4 V | 0.4 | 1.1 | 1.6 | ns    |
| Duty Cycle <sup>1</sup>             | d <sub>t4B</sub>                | V <sub>T</sub> = 1.25 V                          | 45  | 49  | 55  | %     |
| Skew window <sup>1</sup>            | t <sub>sk4B</sub>               | V <sub>T</sub> = 1.25 V                          |     | 25  | 250 | ps    |
| Jitter, Cycle-to-cycle <sup>1</sup> | t <sub>jeyc-cyc4B</sub>         | V <sub>T</sub> = 1.25 V                          |     | 150 | 500 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - SDRAM

T<sub>A</sub> = 0 - 70°C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 20-30 pF (unless otherwise specified)

| PARAMETER                           | SYMBOL                          | CONDITIONS                                       | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------------------------|--|-----|-----|-----|-------|
| Output Impedance                    | R <sub>DSP3B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> * (0.5)         | 10  | 12  | 24  | Ω     |
| Output Impedance                    | R <sub>DSN3B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> * (0.5)         | 10  | 15  | 24  | Ω     |
| Output High Current                 | I <sub>OH3</sub>                | V <sub>OH</sub> @ MIN = 2.0 V                    | -54 | -92 |     | mA    |
|                                     |                                 | V <sub>OH</sub> @ MAX = 3.135 V                  |     | -16 | -46 |       |
| Output Low Current                  | I <sub>OL3</sub>                | V <sub>OL</sub> @ MIN = 1.0 V                    | 54  | 68  |     | mA    |
|                                     |                                 | V <sub>OL</sub> @ MAX = 0.4 V                    |     | 29  | 53  |       |
| Rise Time <sup>1</sup>              | t <sub>r3</sub>                 | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V | 0.4 | 1   | 1.6 | ns    |
| Fall Time <sup>1</sup>              | t <sub>f3</sub>                 | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V | 0.4 | 1.5 | 1.6 | ns    |
| Duty Cycle <sup>1</sup>             | d <sub>3</sub>                  | V <sub>T</sub> = 1.5 V                           | 45  | 52  | 55  | %     |
| Skew window <sup>1</sup>            | t <sub>sk3</sub>                | V <sub>T</sub> = 1.5 V                           |     | 85  | 250 | ps    |
| Jitter, Cycle-to-cycle <sup>1</sup> | t <sub>jycyc-cyc3</sub>         | V <sub>T</sub> = 1.5 V, 66, 100 MHz              |     | 120 | 250 | ps    |
|                                     |                                 | V <sub>T</sub> = 1.5 V, 133 MHz                  |     | 150 | 300 |       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



**Electrical Characteristics - PCI**

T<sub>A</sub> = 0 - 70C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 10-30 pF (unless otherwise specified)

| PARAMETER                           | SYMBOL                          | CONDITIONS                                       | MIN | TYP  | MAX  | UNITS |
|-------------------------------------|---------------------------------|--|-----|------|------|-------|
| Output Impedance                    | R <sub>DSP1B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 12  | 15   | 55   | Ω     |
| Output Impedance                    | R <sub>DSN1B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 12  | 15   | 55   | Ω     |
| Output High Voltage                 | V <sub>OH1</sub>                | I <sub>OH</sub> = -1 mA                          | 2.4 |      |      | V     |
| Output Low Voltage                  | V <sub>OL1</sub>                | I <sub>OL</sub> = 1 mA                           |     |      | 0.55 | V     |
| Output High Current                 | I <sub>OH1</sub>                | V <sub>OH @ MIN</sub> = 1.0 V                    | -33 | -106 |      | mA    |
|                                     |                                 | V <sub>OH @ MAX</sub> = 3.135 V                  |     | -14  | -33  |       |
| Output Low Current                  | I <sub>OL1</sub>                | V <sub>OL @ MIN</sub> = 1.95 V                   | 30  | 94   |      | mA    |
|                                     |                                 | V <sub>OL @ MAX</sub> = 0.4 V                    |     | 29   | 38   |       |
| Rise Time <sup>1</sup>              | t <sub>r1</sub>                 | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V | 0.4 | 1.3  | 2    | ns    |
| Fall Time <sup>1</sup>              | t <sub>f1</sub>                 | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V | 0.4 | 1.4  | 2    | ns    |
| Duty Cycle <sup>1</sup>             | d <sub>t1</sub>                 | V <sub>T</sub> = 1.5 V                           | 45  | 51   | 55   | %     |
| Skew window <sup>1</sup>            | t <sub>sk1</sub>                | V <sub>T</sub> = 1.5 V                           |     | 250  | 500  | ps    |
| Jitter, Cycle-to-cycle <sup>1</sup> | t <sub>jyc-cyc1</sub>           | V <sub>T</sub> = 1.5 V                           |     | 150  | 500  | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - REF, 48MHz\_0 (Pin 25)**

T<sub>A</sub> = 0 - 70C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 10-20 pF (unless otherwise specified)

| PARAMETER                           | SYMBOL                          | CONDITIONS                                       | MIN | TYP | MAX  | UNITS |
|-------------------------------------|---------------------------------|--|-----|-----|------|-------|
| Output Impedance                    | R <sub>DSP5B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 20  | 29  | 60   | Ω     |
| Output Impedance                    | R <sub>DSN5B</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 20  | 27  | 60   | Ω     |
| Output High Voltage                 | V <sub>OH5</sub>                | I <sub>OH</sub> = -1 mA                          | 2.4 |     |      | V     |
| Output Low Voltage                  | V <sub>OL5</sub>                | I <sub>OL</sub> = 1 mA                           |     |     | 0.55 | V     |
| Output High Current                 | I <sub>OH5</sub>                | V <sub>OH @ MIN</sub> = 1.0 V                    | -29 | -54 |      | mA    |
|                                     |                                 | V <sub>OH @ MAX</sub> = 3.135 V                  |     | -11 | -23  |       |
| Output Low Current                  | I <sub>OL5</sub>                | V <sub>OL @ MIN</sub> = 1.95 V                   | 29  | 54  |      | mA    |
|                                     |                                 | V <sub>OL @ MAX</sub> = 0.4 V                    |     | 16  | 27   |       |
| Rise Time <sup>1</sup>              | t <sub>r5</sub>                 | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V | 0.4 | 1.1 | 4    | ns    |
| Fall Time <sup>1</sup>              | t <sub>f5</sub>                 | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V | 0.4 | 1.6 | 4    | ns    |
| Duty Cycle <sup>1</sup>             | d <sub>t5</sub>                 | V <sub>T</sub> = 1.5 V                           | 45  | 53  | 55   | %     |
| Jitter, Cycle-to-cycle <sup>1</sup> | t <sub>jyc-cyc5</sub>           | V <sub>T</sub> = 1.5 V, Fixed clocks             |     | 130 | 500  | ps    |
| Jitter, Cycle-to-cycle <sup>1</sup> | t <sub>jyc-cyc5</sub>           | V <sub>T</sub> = 1.5 V, Ref clocks               |     | 650 | 1000 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - 48MHz\_1 (Pin 26)

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 20\text{-}30\text{ pF}$  (unless otherwise specified)

| PARAMETER                           | SYMBOL          | CONDITIONS                                     | MIN | TYP | MAX  | UNITS    |
|-------------------------------------|-----------------|--|-----|-----|------|----------|
| Output Impedance                    | $R_{DSP3B}^1$   | $V_O = V_{DD} \cdot (0.5)$                     | 10  | 15  | 24   | $\Omega$ |
| Output Impedance                    | $R_{DSN3B}^1$   | $V_O = V_{DD} \cdot (0.5)$                     | 10  | 15  | 24   | $\Omega$ |
| Output High Voltage                 | $V_{OH3}$       | $I_{OH} = -1\text{ mA}$                        | 2.4 |     |      | V        |
| Output Low Voltage                  | $V_{OL3}$       | $I_{OL} = 1\text{ mA}$                         |     |     | 0.55 | V        |
| Output High Current                 | $I_{OH3}$       | $V_{OH @ MIN} = 2.0\text{ V}$                  | -54 | -82 |      | mA       |
|                                     |                 | $V_{OH @ MAX} = 3.135\text{ V}$                |     | -20 | -46  |          |
| Output Low Current                  | $I_{OL3}$       | $V_{OL @ MIN} = 1.0\text{ V}$                  | 54  | 95  |      | mA       |
|                                     |                 | $V_{OL @ MAX} = 0.4\text{ V}$                  |     | 28  | 53   |          |
| Rise Time <sup>1</sup>              | $t_{r3}$        | $V_{OL} = 0.4\text{ V}, V_{OH} = 2.4\text{ V}$ | 0.4 | 1.1 | 1.6  | ns       |
| Fall Time <sup>1</sup>              | $t_{f3}$        | $V_{OH} = 2.4\text{ V}, V_{OL} = 0.4\text{ V}$ | 0.4 | 1.3 | 1.6  | ns       |
| Duty Cycle <sup>1</sup>             | $d_{t3}$        | $V_T = 1.5\text{ V}$                           | 45  | 53  | 55   | %        |
| Jitter, Cycle-to-cycle <sup>1</sup> | $t_{jyc-cyc3B}$ | $V_T = 1.5\text{ V}$                           |     | 130 | 250  | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Group Skews (CPU = 66 MHz)

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5\text{ V} \pm 5\%$

CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF

Refer to Group Offset Waveform diagram for definition of transition edges.

| PARAMETER                | SYMBOL                     | CONDITIONS                   | MIN  | TYP  | MAX | UNITS |
|--------------------------|----------------------------|------------------------------|------|------|-----|-------|
| CPU to SDRAM             | Skew <sup>1</sup>          | CPU @ 1.25 V, SDRAM @ 1.5 V  | -3   | -2.6 | -2  | ns    |
| Skew Window <sup>1</sup> | $T_{w1\text{ CPU-SDRAM}}$  |                              | 0    | 150  | 500 | ps    |
| CPU to 3V66              | Skew <sup>1</sup>          | CPU @ 1.25 V, 3V66 @ 1.5 V   | 7    | 7.2  | 8   | ns    |
| Skew Window <sup>1</sup> | $T_{w1\text{ CPU-3V66}}$   |                              | 0    | 130  | 500 | ps    |
| SDRAM to 3V66            | Skew <sup>1</sup>          | SDRAM, 3V66 @ 1.5 V          | -500 | 100  | 500 | ps    |
| Skew Window <sup>1</sup> | $T_{w1\text{ SDRAM-3V66}}$ |                              | 0    | 155  | 500 | ps    |
| 3V66 to PCI              | Skew <sup>1</sup>          | 3V66, PCI @ 1.5 V            | 1.5  | 2.4  | 3.5 | ns    |
| Skew Window <sup>1</sup> | $T_{w1\text{ 3V66-PCI}}$   |                              | 0    | 275  | 500 | ps    |
| IOAPIC to PCI            | Skew <sup>1</sup>          | IOAPIC @ 1.25 V, PCI @ 1.5 V | -1   | -0.4 | 1   | ns    |
| Skew Window <sup>1</sup> | $T_{w1\text{ IOAPIC-PCI}}$ |                              | 0    | 0.25 | 1   | ns    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



### Group Skews (CPU = 100 MHz)

$T_A = 0 - 70^\circ \text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5 \text{ V} \pm 5\%$

CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF

Refer to Group Offset Waveform diagram for definition of transition edges.

| PARAMETER                       | SYMBOL                       | CONDITIONS                   | MIN  | TYP  | MAX | UNITS |
|---------------------------------|------------------------------|------------------------------|------|------|-----|-------|
| CPU to SDRAM Skew <sup>1</sup>  | $T_{sk2 \text{ CPU-SDRAM}}$  | CPU @ 1.25 V, SDRAM @ 1.5 V  | 4.5  | 4.9  | 5.5 | ns    |
| Skew Window <sup>1</sup>        | $T_{w2 \text{ CPU-SDRAM}}$   |                              | 0    | 140  | 500 | ps    |
| CPU to 3V66 Skew <sup>1</sup>   | $T_{sk2 \text{ CPU-3V66}}$   | CPU @ 1.25 V, 3V66 @ 1.5 V   | 4.5  | 4.8  | 5.5 | ns    |
| Skew Window <sup>1</sup>        | $T_{w2 \text{ CPU-3V66}}$    |                              | 0    | 150  | 500 | ps    |
| SDRAM to 3V66 Skew <sup>1</sup> | $T_{sk2 \text{ SDRAM-3V66}}$ | SDRAM, 3V66 @ 1.5 V          | -500 | 100  | 500 | ps    |
| Skew Window <sup>1</sup>        | $T_{w2 \text{ SDRAM-3V66}}$  |                              | 0    | 155  | 500 | ps    |
| 3V66 to PCI Skew <sup>1</sup>   | $T_{sk2 \text{ 3V66-PCI}}$   | 3V66, PCI @ 1.5 V            | 1.5  | 2.4  | 3.5 | ns    |
| Skew Window <sup>1</sup>        | $T_{w2 \text{ 3V66-PCI}}$    |                              | 0    | 275  | 500 | ps    |
| IOAPIC to PCI Skew <sup>1</sup> | $T_{sk2 \text{ IOAPIC-PCI}}$ | IOAPIC @ 1.25 V, PCI @ 1.5 V | -1   | -0.4 | 1   | ns    |
| Skew Window <sup>1</sup>        | $T_{w2 \text{ IOAPIC-PCI}}$  |                              | 0    | 0.25 | 1   | ns    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Group Skews (CPU = 133 MHz)

$T_A = 0 - 70^\circ \text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5 \text{ V} \pm 5\%$

CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF

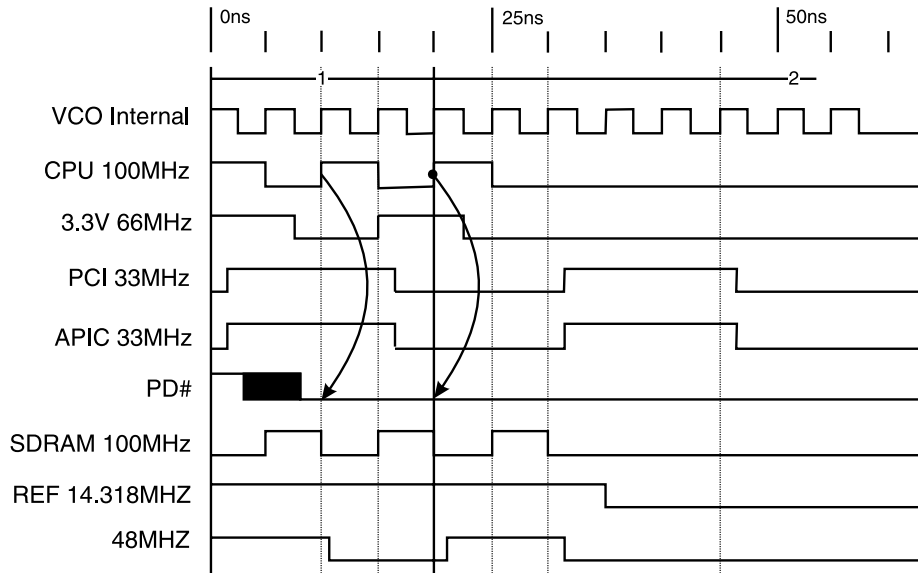
Refer to Group Offset Waveform diagram for definition of transition edges.

| PARAMETER                       | SYMBOL                       | CONDITIONS                   | MIN  | TYP  | MAX | UNITS |
|---------------------------------|------------------------------|------------------------------|------|------|-----|-------|
| CPU to SDRAM Skew <sup>1</sup>  | $T_{sk3 \text{ CPU-SDRAM}}$  | CPU @ 1.25 V, SDRAM @ 1.5 V  | -500 | 70   | 500 | ps    |
| Skew Window <sup>1</sup>        | $T_{w3 \text{ CPU-SDRAM}}$   |                              | 0    | 125  | 500 | ps    |
| CPU to 3V66 Skew <sup>1</sup>   | $T_{sk3 \text{ CPU-3V66}}$   | CPU @ 1.25 V, 3V66 @ 1.5 V   | -500 | -145 | 500 | ps    |
| Skew Window <sup>1</sup>        | $T_{w3 \text{ CPU-3V66}}$    |                              | 0    | 220  | 500 | ps    |
| SDRAM to 3V66 Skew <sup>1</sup> | $T_{sk3 \text{ SDRAM-3V66}}$ | SDRAM, 3V66 @ 1.5 V          | -500 | 100  | 500 | ps    |
| Skew Window <sup>1</sup>        | $T_{w3 \text{ SDRAM-3V66}}$  |                              | 0    | 155  | 500 | ps    |
| 3V66 to PCI Skew <sup>1</sup>   | $T_{sk3 \text{ 3V66-PCI}}$   | 3V66, PCI @ 1.5 V            | 1.5  | 2.4  | 3.5 | ns    |
| Skew Window <sup>1</sup>        | $T_{w3 \text{ 3V66-PCI}}$    |                              | 0    | 275  | 500 | ps    |
| IOAPIC to PCI Skew <sup>1</sup> | $T_{sk3 \text{ IOAPIC-PCI}}$ | IOAPIC @ 1.25 V, PCI @ 1.5 V | -1   | -0.4 | 1   | ns    |
| Skew Window <sup>1</sup>        | $T_{w3 \text{ IOAPIC-PCI}}$  |                              | 0    | 0.25 | 1   | ns    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



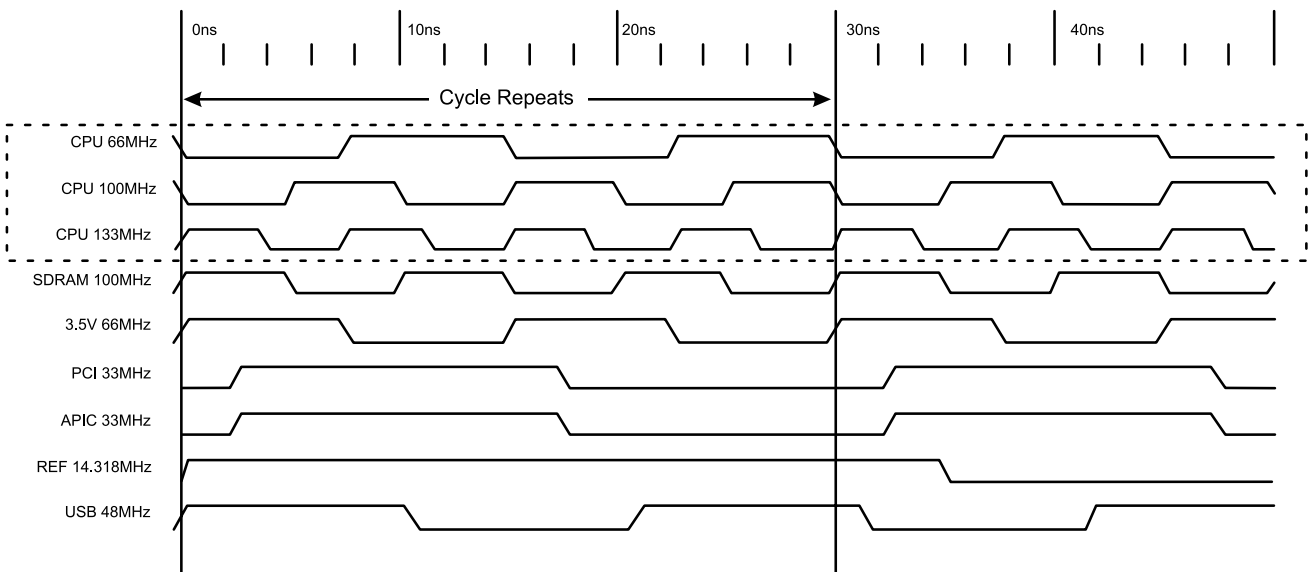
## Power Down Waveform

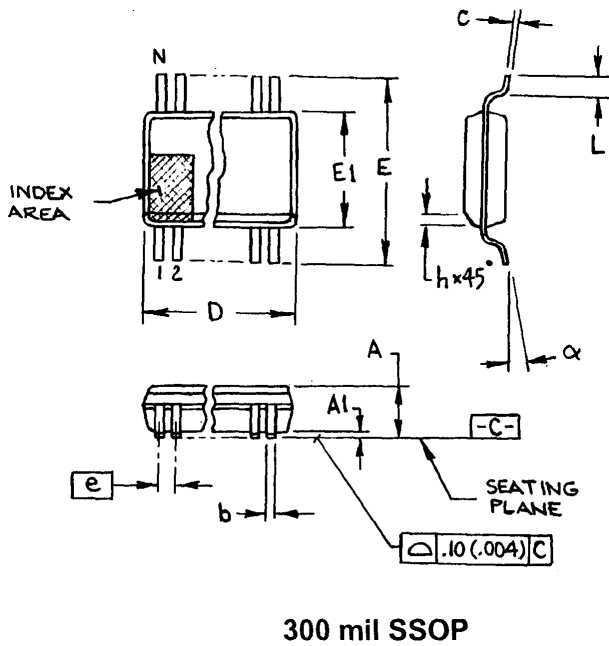


**Note**

1. After PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low transition.
2. Power-up latency <3ms.
3. Waveform shown for 100MHz

## Group Offset Waveforms





| SYMBOL | In Millimeters<br>COMMON DIMENSIONS |        | In Inches<br>COMMON DIMENSIONS |       |
|--------|-------------------------------------|--------|--------------------------------|-------|
|        | MIN                                 | MAX    | MIN                            | MAX   |
| A      | 2.413                               | 2.794  | .095                           | .110  |
| A1     | 0.203                               | 0.406  | .008                           | .016  |
| b      | 0.203                               | 0.343  | .008                           | .0135 |
| c      | 0.127                               | 0.254  | .005                           | .010  |
| D      | SEE VARIATIONS                      |        | SEE VARIATIONS                 |       |
| E      | 10.033                              | 10.668 | .395                           | .420  |
| E1     | 7.391                               | 7.595  | .291                           | .299  |
| e      | 0.635 BASIC                         |        | 0.025 BASIC                    |       |
| h      | 0.381                               | 0.635  | .015                           | .025  |
| L      | 0.508                               | 1.016  | .020                           | .040  |
| N      | SEE VARIATIONS                      |        | SEE VARIATIONS                 |       |
| α      | 0°                                  | 8°     | 0°                             | 8°    |

VARIATIONS

| N  | D mm.  |        | D (inch) |      |
|----|--------|--------|----------|------|
|    | MIN    | MAX    | MIN      | MAX  |
| 56 | 18.288 | 18.542 | .720     | .730 |

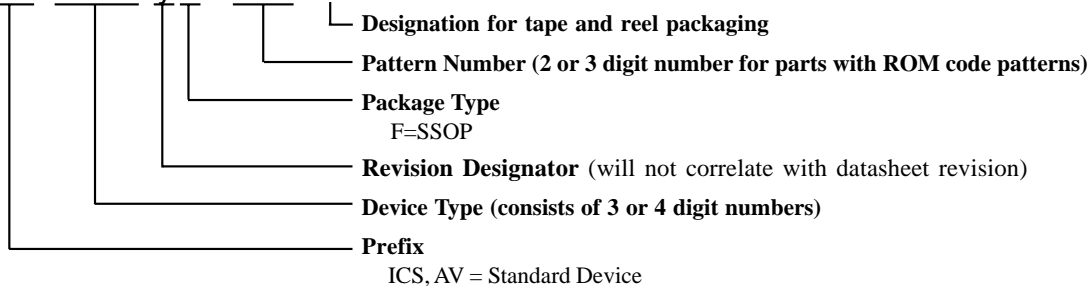
JEDEC MO-118  
DOC# 10-0034  
6/1/00  
REV B

### Ordering Information

ICS9250yF-26-T

Example:

ICS XXXX y F - PPP - T



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