

Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:

810/810E and 815 type chipset.

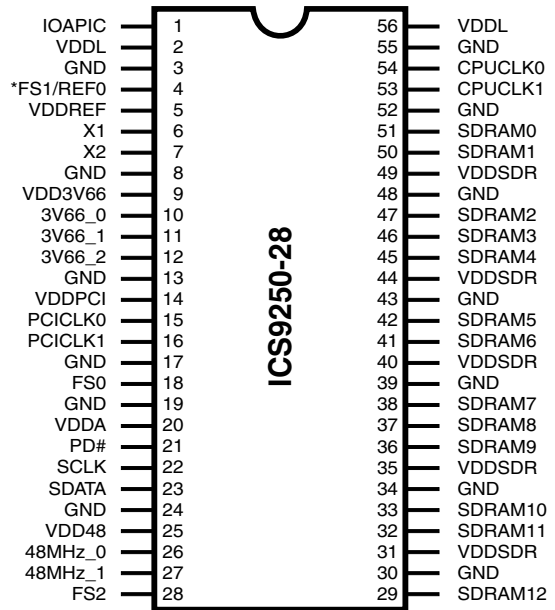
Output Features:

- 2 CPU (2.5V) (up to 133MHz achievable through I²C)
- 13 SDRAM (3.3V) (up to 133MHz achievable through I²C)
- 2 PCI (3.3 V) @33.3MHz
- 1 IOAPIC (2.5V) @ 33.3 MHz
- 3 Hublink clocks (3.3 V) @ 66.6 MHz
- 2 (3.3V) @ 48 MHz (Non spread spectrum)
- 1 REF (3.3V) @ 14.318 MHz

Features:

- Supports spread spectrum modulation, 0 to -0.5% down spread.
- I²C support for power management
- Efficient power management scheme through PD#
- Uses external 14.138 MHz crystal
- Alternate frequency selections available through I²C control.

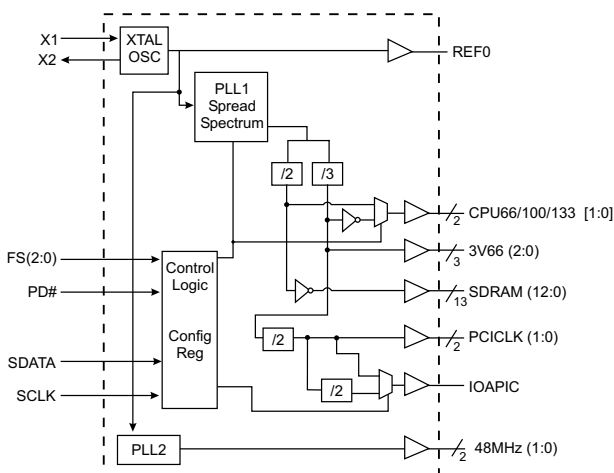
Pin Configuration



56-Pin 300mil SSOP

* This input has a 50KΩ pull-down to GND.

Block Diagram



Functionality

| FS2 | FS0 | FS1 | Function |
|-----|-----|-----|---------------------------------------|
| 0 | 0 | X | Tristate |
| 0 | 1 | X | Test |
| 1 | 0 | 0 | Active CPU = 66MHz SDRAM = 100MHz |
| 1 | 1 | 0 | Active CPU = 100MHz SDRAM = 100MHz |
| 1 | 0 | 1 | Active CPU = 133MHz SDRAM = 133MHz |
| 1 | 1 | 1 | Active CPU = 133MHz SDRAM = 100MHz |

Power Groups

Analog
VDDREF = X1, X2
VDDA = PLL1
VDD48 = PLL2

Digital
VDD3V66, VDDPCI
VDDSDR, VDDL

ICS9250-28



General Description

The **ICS9250-28** is part of a two chip clock solution for 810/810E and 815 type chipset. Combined with the ICS9112-17, the **ICS9250-28** provides all necessary clock signals for such a system.

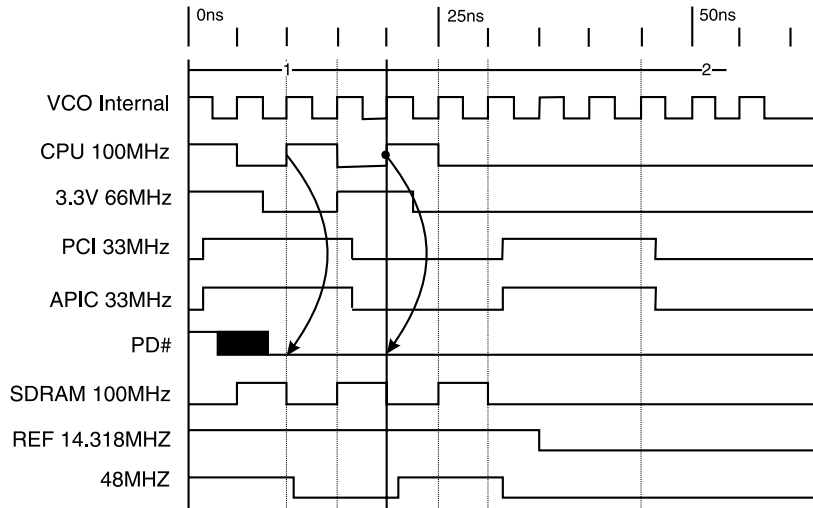
Spread spectrum may be enabled through I²C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-28 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Pin Configuration

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|--|--------------|------|---|
| 1 | IOAPIC | OUT | 2.5V clock output running at 33.3MHz. |
| 2, 56 | VDDL | PWR | 2.5V power supply for CPU & IOAPIC |
| 4 | FS1 | IN | Function Select pin. Determines CPU frequency, all output functionality |
| | REF0 | OUT | 3.3V, 14.318MHz reference clock output. |
| 5, 9, 14, 20, 25, 31, 35, 40, 44, 49 | VDD | PWR | 3.3V power supply |
| 6 | X1 | IN | Crystal input, has internal load cap (33pF) and feedback resistor from X2 |
| 7 | X2 | OUT | Crystal output, nominally 14.318MHz. Has internal load cap (33pF) |
| 3, 8, 13, 17, 19, 24, 30, 34, 39, 43, 48, 52, 55 | GND | PWR | Ground pins for 3.3V supply |
| 12, 11, 10 | 3V66 (2:0) | OUT | 3.3V Fixed 66MHz clock outputs for HUB |
| 28, 18 | FS (2, 0) | IN | Function Select pins. Determines CPU frequency, all output functionality. Please refer to Functionality table on page 3. |
| 16, 15 | PCICLK[1:0] | OUT | 3.3V PCI clock outputs |
| 21 | PD# | IN | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 22 | SCLK | IN | Clock pin of I ² C circuitry 5V tolerant |
| 23 | SDATA | I/O | Data pin for I ² C circuitry 5V tolerant |
| 26, 27 | 48MHz_0 | OUT | 3.3V Fixed 48MHz clock outputs. |
| 29, 32, 33, 36, 37, 38, 41, 42, 45, 46, 47, 50, 51 | SDRAM (12:0) | OUT | 3.3V output running 100MHz. All SDRAM outputs can be turned off through I ² C |
| 54, 53 | CPUCLK (1:0) | OUT | 2.5V Host bus clock output. 66MHz, 100MHz or 133MHz depending on FS (2:0) pins. |



Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consecutive rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low transition.
2. Power-up latency <3ms.
3. Waveform shown for 100MHz

Maximum Allowed Current

| 815 Condition | Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 2.625V All static inputs = Vddq3 or GND | Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 3.465V All static inputs = Vddq3 or GND |
|--|--|--|
| Powerdown Mode (PWRDWN# = 0) | 10mA | 10mA |
| Full Active 66MHz FS[2:0] = 010 | 70mA | 400mA |
| Full Active 100MHz FS[2:0] = 011 | 100mA | 400mA |
| Full Active 133MHz FS[2:0] = 111 | 130mA | 450mA |

Clock Enable Configuration

| PD# | CPUCLK | SDRAM | IOAPIC | 66MHz | PCICLK | REF, 48MHz | Osc | VCOs |
|-----|--------|-------|--------|-------|--------|---------------|-----|------|
| 0 | LOW | LOW | LOW | LOW | LOW | LOW | OFF | OFF |
| 1 | ON | ON | ON | ON | ON | ON | ON | ON |



Truth Table

| FS2 | FS0 | FS1 | CPU | SDRAM | 3V66 | PCI | 48MHz | REF | IOAPIC |
|-----|-----|-----|----------|----------|----------|----------|----------|------------|----------|
| 0 | 0 | X | Tristate | Tristate | Tristate | Tristate | Tristate | Tristate | Tristate |
| 0 | 1 | X | TCLK/2 | TCLK/2 | TCLK/3 | TCLK/6 | TCLK/2 | TCLK | TCLK/6 |
| 1 | 0 | 0 | 66.6 MHz | 100 MHz | 66.6 MHz | 33.3 MHz | 48 MHz | 14.318 MHz | 33.3 MHz |
| 1 | 1 | 0 | 100 MHz | 100 MHz | 66.6 MHz | 33.3 MHz | 48 MHz | 14.318 MHz | 33.3 MHz |
| 1 | 0 | 1 | 133 MHz | 133 MHz | 66.6 MHz | 33.3 MHz | 48 MHz | 14.318 MHz | 33.3 MHz |
| 1 | 1 | 1 | 133 MHz | 100 MHz | 66.6 MHz | 33.3 MHz | 48 MHz | 14.318 MHz | 33.3 MHz |

Byte 3: ICS Reserved Functionality and frequency select register (Default as noted in PWD)

| Bit | Description | | | | | | | | PWD |
|-------|---------------------------|-----|--------|------------|-----------|----------|------------|------------|-------------|
| Bit7 | ICS Reserved bit (Note 2) | | | | | | | | 0 |
| Bit6 | ICS Reserved bit (Note 2) | | | | | | | | 0 |
| Bit5 | ICS Reserved bit (Note 2) | | | | | | | | 0 |
| Bit4 | ICS Reserved bit (Note 2) | | | | | | | | 0 |
| Bit3 | ICS Reserved bit (Note 2) | | | | | | | | 0 |
| Bit2 | Undefined bit (Note 3) | | | | | | | | X |
| Bit1 | Undefined bit (Note 3) | | | | | | | | X |
| Bit 0 | Bit 0 | FS0 | FS1 | CPUCLK MHz | SDRAM MHz | 3V66 MHz | PCICLK MHz | IOAPIC MHz | 0 Note 1 |
| | 0 | 0 | 0 | 66.66 | 100.0 | 66.66 | 33.33 | 33.33 | |
| | 0 | 1 | 0 | 100.0 | 100.0 | 66.66 | 33.33 | 33.33 | |
| | 0 | 0 | 1 | 133.32 | 133.32 | 66.66 | 33.33 | 33.33 | |
| | 0 | 1 | 1 | 133.32 | 100.0 | 66.66 | 33.33 | 33.33 | |
| | 1 | 0 | 0 | 66.66 | 100.0 | 66.66 | 33.33 | 33.33 | |
| | 1 | 1 | 0 | 100.0 | 100.0 | 66.66 | 33.33 | 33.33 | |
| | 1 | 0 | 1 | 133.32 | 133.32 | 66.66 | 33.33 | 33.33 | |
| 1 | 1 | 1 | 133.32 | 133.32 | 66.66 | 33.33 | 33.33 | | |

Note 1: For system operation, the BSEL lines of the CPU will program FS0, FS2 for the appropriate CPU speed, always with SDRAM = 100MHz. After BIOS verifies the SDRAM is PC133 speed, then bit 0 can be written from the default 0 to 1 to change the SDRAM output frequency from 100MHz to 133MHz. This will only change if the CPU is at the 133MHz FSB speed as shown in this table. The CPU, 3V66, PCI, and IOAPIC clocks will be glitch free during this transition, and only SDRAM will change.

Note 2: "ICS RESERVED BITS" must be writtarn as "0".

Note3: Undefined bits can be written either as "1 or 0"



Byte 0: Control Register (1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|--------------------------------|-----|-------------------|
| Bit 7 | - | Reserved ID | 0 | (Active/Inactive) |
| Bit 6 | - | Reserved ID | 0 | (Active/Inactive) |
| Bit 5 | - | Reserved ID | 0 | (Active/Inactive) |
| Bit 4 | - | Reserved ID | 1 | (Active/Inactive) |
| Bit 3 | - | SpreadSpectrum (1=On/0=Off) | 1 | (Active/Inactive) |
| Bit 2 | 27 | 48MHz 1 | 1 | (Active/Inactive) |
| Bit 1 | 26 | 48MHz 0 | 1 | (Active/Inactive) |
| Bit 0 | - | Reserved ID | 0 | (Active/Inactive) |

Note: Reserved ID bits must be written as "0"

Byte 1: Control Register (1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|--------|-----|-------------------|
| Bit 7 | 38 | SDRAM7 | 1 | (Active/Inactive) |
| Bit 6 | 41 | SDRAM6 | 1 | (Active/Inactive) |
| Bit 5 | 42 | SDRAM5 | 1 | (Active/Inactive) |
| Bit 4 | 45 | SDRAM4 | 1 | (Active/Inactive) |
| Bit 3 | 46 | SDRAM3 | 1 | (Active/Inactive) |
| Bit 2 | 47 | SDRAM2 | 1 | (Active/Inactive) |
| Bit 1 | 50 | SDRAM1 | 1 | (Active/Inactive) |
| Bit 0 | 51 | SDRAM0 | 1 | (Active/Inactive) |

Byte 2: Control Register (1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|--------------|-----|-------------------|
| Bit 7 | 12 | 3V66-2 (AGP) | 1 | (Active/Inactive) |
| Bit 6 | 29 | SDRAM12 | 1 | (Active/Inactive) |
| Bit 5 | 32 | SDRAM11 | 1 | (Active/Inactive) |
| Bit 4 | 33 | SDRAM10 | 1 | (Active/Inactive) |
| Bit 3 | 36 | SDRAM9 | 1 | (Active/Inactive) |
| Bit 2 | 37 | SDRAM8 | 1 | (Active/Inactive) |
| Bit 1 | 16 | PCICLK1 | 1 | (Active/Inactive) |
| Bit 0 | - | Reserved | 0 | (Active/Inactive) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default
3. Undefined bit can be written with either a "1" or "0".



Byte 4: Reserved Register
(1 = enable, 0 = disable)

| Bit | Pin# | Name | PWD | Description |
|-------|------|----------|-----|-------------------|
| Bit 7 | - | Reserved | 0 | (Active/Inactive) |
| Bit 6 | - | Reserved | 0 | (Active/Inactive) |
| Bit 5 | - | Reserved | 0 | (Active/Inactive) |
| Bit 4 | - | Reserved | 0 | (Active/Inactive) |
| Bit 3 | - | Reserved | 0 | (Active/Inactive) |
| Bit 2 | - | Reserved | 0 | (Active/Inactive) |
| Bit 1 | - | Reserved | 0 | (Active/Inactive) |
| Bit 0 | - | Reserved | 0 | (Active/Inactive) |

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Group Timing Relationship Table¹

| Group | CPU 66MHz SDRAM 100MHz | | CPU 100MHz SDRAM 100MHz | | CPU 133MHz SDRAM 100MHz | | CPU 133MHz SDRAM 133MHz | |
|---------------|---------------------------|-----------|----------------------------|-----------|----------------------------|-----------|----------------------------|-----------|
| | Offset | Tolerance | Offset | Tolerance | Offset | Tolerance | Offset | Tolerance |
| CPU to SDRAM | -2.5ns | 500ps | 5.0ns | 500ps | 0.0ns | 500ps | 3.75ns | 500ps |
| CPU to 3V66 | 7.5ns | 500ps | 5.0ns | 500ps | 0.0ns | 500ps | 0.0ns | 500ps |
| SDRAM to 3V66 | 0.0ns | 500ps | 0.0ns | 500ps | 0.0ns | 500ps | -3.75ns | 500ps |
| 3V66 to PCI | 1.5-3.5ns | 500ps | 1.5-3.5ns | 500ps | 1.5-3.5ns | 500ps | 1.5 -3.5ns | 500ps |
| PCI to PCI | 0.0ns | 500ps | 0.0ns | 500ps | 500ps | 1.0ns | 0.0ns | 500ps |
| USB & DOT | Asynch | N/A | Asynch | N/A | Asynch | N/A | Asynch | N/A |



Absolute Maximum Ratings

- Core Supply Voltage 4.6 V
- I/O Supply Voltage 3.6V
- Logic Inputs GND -0.5 V to V_{DD} +0.5 V
- Ambient Operating Temperature 0°C to +70°C
- Maximum Case Operating Temperature +135°C
- Storage Temperature -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|-------------------------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage | V _{IH} | | 2 | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | V _{SS} -0.3 | | 0.8 | V |
| Input High Current | I _{IH} | V _{IN} = V _{DD} | -5 | | 5 | μA |
| Input Low Current | I _{IL1} | V _{IN} = 0 V; Inputs with no pull-up resistors | -5 | | | μA |
| | I _{IL2} | V _{IN} = 0 V; Inputs with pull-up resistors | -200 | | | |
| Operating Supply Current | I _{DD3.3OP} | C _L = 0 pF; @ 66/100 MHz | | 138 | 200 | mA |
| | | C _L = 0 pF; @ 100/100 MHz | | 126 | 200 | |
| | | C _L = 0 pF; @ 133/133 MHz | | 172 | 200 | |
| | | C _L = 0 pF; @ 133/100 MHz | | 141 | 200 | |
| | | C _L = Max loads; @ 66/100 MHz | | 339 | 400 | mA |
| | | C _L = Max loads; @ 100/100 MHz | | 328 | 400 | |
| | | C _L = Max loads; @ 133/133 MHz | | 383 | 450 | |
| | | C _L = Max loads; @ 133/100 MHz | | 340 | 400 | |
| | I _{DD2.5OP} | C _L = 0 pF; @ 66/100 MHz | | 9 | 15 | mA |
| | | C _L = 0 pF; @ 100/100 MHz | | 11 | 18 | |
| | | C _L = 0 pF; @ 133/133 MHz | | 13 | 20 | |
| | | C _L = 0 pF; @ 133/100 MHz | | 13 | 20 | mA |
| | | C _L = Max loads; @ 66/100 MHz | | 13 | 35 | |
| | | C _L = Max loads; @ 100/100 MHz | | 23 | 60 | |
| Powerdown Current | I _{DD3.3PD} | C _L = Max loads | | 251 | 400 | μA |
| | I _{DD.25PD} | Input address VDD or GND | | <1 | 10 | |
| Input Frequency | F _i | V _{DD} = 3.3 V | 12 | 14.318 | 16 | MHz |
| Transition time ¹ | T _{trans} | To 1st crossing of target frequency | | | 3 | ms |
| Settling time ¹ | T _s | From 1st crossing to 1% target frequency | | | 3 | ms |
| Clk Stabilization ¹ | T _{STAB} | From V _{DD} = 3.3 V to 1% target frequency | | | 3 | ms |
| Delay ¹ | t _{PZH} , t _{PZL} | Output enable delay (all outputs) | 1 | | 10 | ns |
| | t _{PHZ} , t _{PLZ} | Output disable delay (all outputs) | 1 | | 10 | ns |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$; $V_{DDL} = 2.5 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|-------------------------|--|------|-----|-----|----------|
| Output Impedance | R_{DSP2B}^1 | $V_O = V_{DD} * (0.5)$ | 13.5 | 16 | 45 | Ω |
| Output Impedance | R_{DSN2B}^1 | $V_O = V_{DD} * (0.5)$ | 13.5 | 21 | 45 | Ω |
| Output High Voltage | V_{OH2B} | $I_{OH} = -1 \text{ mA}$ | 2 | | | V |
| Output Low Voltage | V_{OL2B} | $I_{OL} = 1 \text{ mA}$ | | | 0.4 | V |
| Output High Current | I_{OH2B} | $V_{OH @ MIN} = 1.0 \text{ V}$ | -27 | -68 | | mA |
| | | $V_{OH @ MAX} = 2.375 \text{ V}$ | | -9 | -27 | |
| Output Low Current | I_{OL2B} | $V_{OL @ MIN} = 1.2 \text{ V}$ | 27 | 54 | | mA |
| | | $V_{OL @ MAX} = 0.3 \text{ V}$ | | 11 | 30 | |
| Rise Time ¹ | t_{r2B} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.0 \text{ V}$ | 0.4 | 1.1 | 1.6 | ns |
| Fall Time ¹ | t_{f2B} | $V_{OH} = 2.0 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.1 | 1.6 | ns |
| Duty Cycle ¹ | d_{t2B} | $V_T = 1.25 \text{ V}$ | 45 | 49 | 55 | % |
| Skew window ¹ | t_{sk2B} | $V_T = 1.25 \text{ V}$ | | 45 | 175 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{j\text{cyc-cyc}2B}$ | $V_T = 1.25 \text{ V}$ | | 135 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|------------------------|--|-----|------|------|----------|
| Output Impedance | R_{DSP1B}^1 | $V_O = V_{DD} * (0.5)$ | 12 | 14 | 55 | Ω |
| Output Impedance | R_{DSN1B}^1 | $V_O = V_{DD} * (0.5)$ | 12 | 14.5 | 55 | Ω |
| Output High Voltage | V_{OH1} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 1 \text{ mA}$ | | | 0.55 | V |
| Output High Current | I_{OH1} | $V_{OH @ MIN} = 1.0 \text{ V}$ | -33 | -108 | | mA |
| | | $V_{OH @ MAX} = 3.135 \text{ V}$ | | -9 | -33 | |
| Output Low Current | I_{OL1} | $V_{OL @ MIN} = 1.95 \text{ V}$ | 30 | 95 | | mA |
| | | $V_{OL @ MAX} = 0.4 \text{ V}$ | | 29 | 38 | |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | 0.4 | 1.2 | 1.6 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.2 | 1.6 | ns |
| Duty Cycle ¹ | d_{t1} | $V_T = 1.5 \text{ V}$ | 45 | 49 | 55 | % |
| Skew window ¹ | t_{sk1} | $V_T = 1.5 \text{ V}$ | | 135 | 175 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{j\text{cyc-cyc}1}$ | $V_T = 1.5 \text{ V}$ | | 175 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - IOAPIC

T_A = 0 - 70C; V_{DDL} = 2.5 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------------------------|--|-----|-----|-----|-------|
| Output Impedance | R _{DSP4B} ¹ | V _O = V _{DD} *(0.5) | 9 | 16 | 30 | Ω |
| Output Impedance | R _{DSN4B} ¹ | V _O = V _{DD} *(0.5) | 9 | 20 | 30 | Ω |
| Output High Voltage | V _{OH4B} | I _{OH} = -1 mA | 2 | | | V |
| Output Low Voltage | V _{OL4B} | I _{OL} = 1 mA | | | 0.4 | V |
| Output High Current | I _{OH4B} | V _{OH @ MIN} = 1.0 V | -27 | -68 | | mA |
| | | V _{OH @ MAX} = 2.375 V | | -9 | -27 | |
| Output Low Current | I _{OL4B} | V _{OL @ MIN} = 1.2 V | 27 | 54 | | mA |
| | | V _{OL @ MAX} = 0.3 V | | 11 | 30 | |
| Rise Time ¹ | t _{r4B} | V _{OL} = 0.4 V, V _{OH} = 2.0 V | 0.4 | 1.1 | 1.6 | ns |
| Fall Time ¹ | t _{f4B} | V _{OH} = 2.0 V, V _{OL} = 0.4 V | 0.4 | 1.1 | 1.6 | ns |
| Duty Cycle ¹ | d _{t4B} | V _T = 1.25 V | 45 | 49 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | t _{jyc-cyc4B} | V _T = 1.25 V | | 180 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 20-30 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------------------------|--|-----|-----|-----|-------|
| Output Impedance | R _{DSP3B} ¹ | V _O = V _{DD} *(0.5) | 10 | 12 | 24 | Ω |
| Output Impedance | R _{DSN3B} ¹ | V _O = V _{DD} *(0.5) | 10 | 15 | 24 | Ω |
| Output High Voltage | V _{OH3} | I _{OH} = -1 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL3} | I _{OL} = 1 mA | | | 0.4 | V |
| Output High Current | I _{OH3} | V _{OH @ MIN} = 2.0 V | -54 | -92 | | mA |
| | | V _{OH @ MAX} = 3.135 V | | -16 | -46 | |
| Output Low Current | I _{OL3} | V _{OL @ MIN} = 1.0 V | 54 | 68 | | mA |
| | | V _{OL @ MAX} = 0.4 V | | 29 | 53 | |
| Rise Time ¹ | t _{r3} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.4 | 1 | 1.6 | ns |
| Fall Time ¹ | t _{f3} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.4 | 1.5 | 1.6 | ns |
| Duty Cycle ¹ | d _{t3} | V _T = 1.5 V | 45 | 52 | 55 | % |
| Skew window ¹ | t _{sk3} | V _T = 1.5 V | | 120 | 250 | ps |
| Jitter, Cycle-to-cycle ¹ | t _{jyc-cyc3} | V _T = 1.5 V | | 135 | 250 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 10\text{-}30 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|--|-----|------|------|----------|
| Output Impedance | R_{DSP1B}^1 | $V_O = V_{DD} \cdot (0.5)$ | 12 | 15 | 55 | Ω |
| Output Impedance | R_{DSN1B}^1 | $V_O = V_{DD} \cdot (0.5)$ | 12 | 15 | 55 | Ω |
| Output High Voltage | V_{OH1} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL1} | $I_{OL} = 1 \text{ mA}$ | | | 0.55 | V |
| Output High Current | I_{OH1} | $V_{OH @ MIN} = 1.0 \text{ V}$ | -33 | -106 | | mA |
| | | $V_{OH @ MAX} = 3.135 \text{ V}$ | | -14 | -33 | |
| Output Low Current | I_{OL1} | $V_{OL @ MIN} = 1.95 \text{ V}$ | 30 | 94 | | mA |
| | | $V_{OL @ MAX} = 0.4 \text{ V}$ | | 29 | 38 | |
| Rise Time ¹ | t_{r1} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | 0.4 | 1.3 | 2 | ns |
| Fall Time ¹ | t_{f1} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.4 | 2 | ns |
| Duty Cycle ¹ | d_{11} | $V_T = 1.5 \text{ V}$ | 45 | 51 | 55 | % |
| Skew window ¹ | t_{sk1} | $V_T = 1.5 \text{ V}$ | | 20 | 500 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jyc-cyc1}$ | $V_T = 1.5 \text{ V}$ | | 175 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz_0 (Pin 26)

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 10\text{-}20 \text{ pF}$ (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|----------------|--|-----|-----|------|----------|
| Output Impedance | R_{DSP5B}^1 | $V_O = V_{DD} \cdot (0.5)$ | 20 | 29 | 60 | Ω |
| Output Impedance | R_{DSN5B}^1 | $V_O = V_{DD} \cdot (0.5)$ | 20 | 27 | 60 | Ω |
| Output High Voltage | V_{OH15} | $I_{OH} = -1 \text{ mA}$ | 2.4 | | | V |
| Output Low Voltage | V_{OL5} | $I_{OL} = 1 \text{ mA}$ | | | 0.55 | V |
| Output High Current | I_{OH5} | $V_{OH @ MIN} = 1.0 \text{ V}$ | -29 | -54 | | mA |
| | | $V_{OH @ MAX} = 3.135 \text{ V}$ | | -11 | -23 | |
| Output Low Current | I_{OL5} | $V_{OL @ MIN} = 1.95 \text{ V}$ | 29 | 54 | | mA |
| | | $V_{OL @ MAX} = 0.4 \text{ V}$ | | 16 | 27 | |
| Rise Time ¹ | t_{r5} | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ | 0.4 | 1.3 | 4 | ns |
| Fall Time ¹ | t_{f5} | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ | 0.4 | 1.6 | 4 | ns |
| Duty Cycle ¹ | d_{15} | $V_T = 1.5 \text{ V}$ | 45 | 53 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | $t_{jyc-cyc5}$ | $V_T = 1.5 \text{ V}$, Fixed clocks | | 160 | 500 | ps |
| Jitter, Cycle-to-cycle ¹ | $t_{jyc-cyc5}$ | $V_T = 1.5 \text{ V}$, Ref clocks | | 420 | 1000 | ps |

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - 48MHz_1 (Pin 27)

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-15 pF (unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------------------------|--|-----|-----|------|-------|
| Output Impedance | R _{DSP3B} ¹ | V _O = V _{DD} *(0.5) | 10 | 15 | 24 | Ω |
| Output Impedance | R _{DSN3B} ¹ | V _O = V _{DD} *(0.5) | 10 | 15 | 24 | Ω |
| Output High Voltage | V _{OH3} | I _{OH} = -1 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL3} | I _{OL} = 1 mA | | | 0.55 | V |
| Output High Current | I _{OH3} | V _{OH @ MIN} = 2.0 V | -54 | -82 | | mA |
| | | V _{OH @ MAX} = 3.135 V | | -20 | -46 | |
| Output Low Current | I _{OL3} | V _{OL @ MIN} = 1.0 V | 54 | 95 | | mA |
| | | V _{OL @ MAX} = 0.4 V | | 28 | 53 | |
| Rise Time ¹ | t _{r3} | V _{OL} = 0.4 V, V _{OH} = 2.4 V | 0.4 | 1.1 | 1.6 | ns |
| Fall Time ¹ | t _{f3} | V _{OH} = 2.4 V, V _{OL} = 0.4 V | 0.4 | 1.3 | 1.6 | ns |
| Duty Cycle ¹ | d _{t3} | V _T = 1.5 V | 45 | 53 | 55 | % |
| Jitter, Cycle-to-cycle ¹ | t _{jyc-cyc3B} | V _T = 1.5 V | | 145 | 500 | ps |

¹Guaranteed by design, not 100% tested in production.



Group Skews (CPU 66 MHz, SDRAM 100MHz)

$T_A = 0 - 70^\circ C$; $V_{DD} = 3.3 V \pm 5\%$, $V_{DDL} = 2.5 V \pm 5\%$

CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF

Refer to Group Offset Waveforms diagram for definition of transition edges.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|----------------------|------------------------------|------|------|-----|-------|
| CPU to SDRAM Skew ¹ | T_{sk1} CPU-SDRAM | CPU @ 1.25 V, SDRAM @ 1.5 V | -3 | -2.7 | -2 | ns |
| Skew Window ¹ | T_{w1} CPU-SDRAM | | 0 | 165 | 500 | ps |
| CPU to 3V66 Skew ¹ | T_{sk1} CPU-3V66 | CPU @ 1.25 V, 3V66 @ 1.5 V | 7 | 7.6 | 8 | ns |
| Skew Window ¹ | T_{w1} CPU-3V66 | | 0 | 105 | 500 | ps |
| SDRAM to 3V66 Skew ¹ | T_{sk1} SDRAM-3V66 | SDRAM, 3V66 @ 1.5 V | -500 | 180 | 500 | ps |
| Skew Window ¹ | T_{w1} SDRAM-3V66 | | 0 | 210 | 500 | ps |
| 3V66 to PCI Skew ¹ | T_{sk1} 3V66-PCI | 3V66, PCI @ 1.5 V | 1.5 | 2.1 | 3.5 | ns |
| Skew Window ¹ | T_{w1} 3V66-PCI | | 0 | 90 | 500 | ps |
| IOAPIC to PCI Skew ¹ | T_{sk1} IOAPIC-PCI | IOAPIC @ 1.25 V, PCI @ 1.5 V | -1 | -0.1 | 1 | ns |
| Skew Window ¹ | T_{w1} IOAPIC-PCI | | 0 | 0 | 1 | ns |

¹Guaranteed by design, not 100% tested in production.

Group Skews (CPU 100 MHz, SDRAM 100MHz)

$T_A = 0 - 70^\circ C$; $V_{DD} = 3.3 V \pm 5\%$, $V_{DDL} = 2.5 V \pm 5\%$

CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF

Refer to Group Offset Waveforms diagram for definition of transition edges.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|----------------------|------------------------------|------|------|-----|-------|
| CPU to SDRAM Skew ¹ | T_{sk2} CPU-SDRAM | CPU @ 1.25 V, SDRAM @ 1.5 V | 4.5 | 4.9 | 5.5 | ns |
| Skew Window ¹ | T_{w2} CPU-SDRAM | | 0 | 180 | 500 | ps |
| CPU to 3V66 Skew ¹ | T_{sk2} CPU-3V66 | CPU @ 1.25 V, 3V66 @ 1.5 V | 4.5 | 5 | 5.5 | ns |
| Skew Window ¹ | T_{w2} CPU-3V66 | | 0 | 100 | 500 | ps |
| SDRAM to 3V66 Skew ¹ | T_{sk2} SDRAM-3V66 | SDRAM, 3V66 @ 1.5 V | -500 | 175 | 500 | ps |
| Skew Window ¹ | T_{w2} SDRAM-3V66 | | 0 | 200 | 500 | ps |
| 3V66 to PCI Skew ¹ | T_{sk2} 3V66-PCI | 3V66, PCI @ 1.5 V | 1.5 | 2.1 | 3.5 | ns |
| Skew Window ¹ | T_{w2} 3V66-PCI | | 0 | 90 | 500 | ps |
| IOAPIC to PCI Skew ¹ | T_{sk2} IOAPIC-PCI | IOAPIC @ 1.25 V, PCI @ 1.5 V | -1 | -0.1 | 1 | ns |
| Skew Window ¹ | T_{w2} IOAPIC-PCI | | 0 | 0 | 1 | ns |

¹Guaranteed by design, not 100% tested in production.



Group Skews (CPU 133 MHz, SDRAM 133MHz)

T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%

CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF

Refer to Group Offset Waveforms diagram for definition of transition edges.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|-----------------------------|------------------------------|-------|-------|-------|-------|
| CPU to SDRAM Skew ¹ | T _{sk3} CPU-SDRAM | CPU @ 1.25 V, SDRAM @ 1.5 V | 3.25 | 3.45 | 4.25 | ns |
| Skew Window ¹ | T _{w3} CPU-SDRAM | | 0 | 155 | 500 | ps |
| CPU to 3V66 Skew ¹ | T _{sk3} CPU-3V66 | CPU @ 1.25 V, 3V66 @ 1.5 V | -500 | 120 | 500 | ps |
| Skew Window ¹ | T _{w3} CPU-3V66 | | 0 | 120 | 500 | ps |
| SDRAM to 3V66 Skew ¹ | T _{sk3} SDRAM-3V66 | SDRAM, 3V66 @ 1.5 V | -3.25 | -3.08 | -4.25 | ps |
| Skew Window ¹ | T _{w3} SDRAM-3V66 | | 0 | 175 | 500 | ps |
| 3V66 to PCI Skew ¹ | T _{sk3} 3V66-PCI | 3V66, PCI @ 1.5 V | 1.5 | 2.2 | 3.5 | ns |
| Skew Window ¹ | T _{w3} 3V66-PCI | | 0 | 80 | 500 | ps |
| IOAPIC to PCI Skew ¹ | T _{sk3} IOAPIC-PCI | IOAPIC @ 1.25 V, PCI @ 1.5 V | -1 | -0.1 | 1 | ns |
| Skew Window ¹ | T _{w3} IOAPIC-PCI | | 0 | 0 | 1 | ns |

¹Guaranteed by design, not 100% tested in production.

Group Skews (CPU133 MHz, SDRAM 100MHz)

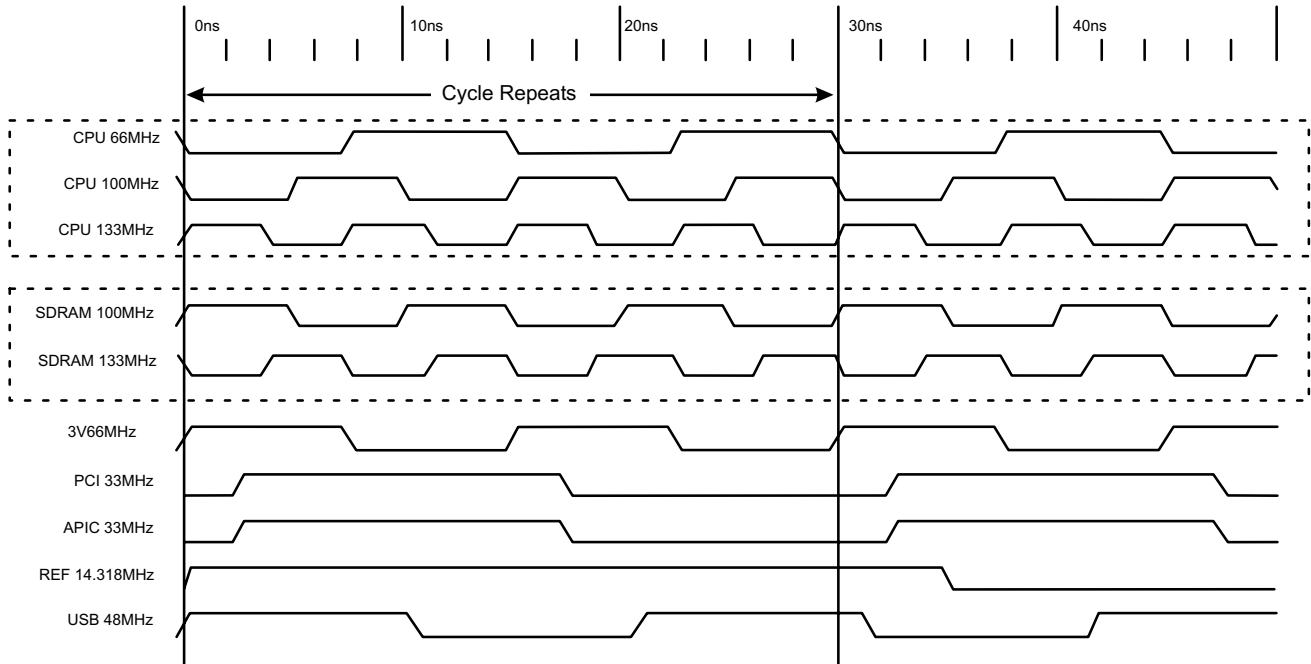
T_A = 0 - 70° C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%

CPU & IOAPIC load (lumped) = 20 pF; PCI, SDRAM, 3V66 load (lumped) = 30 pF

Refer to Group Offset Waveforms diagram for definition of transition edges.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|-----------------------------|------------------------------|------|------|-----|-------|
| CPU to SDRAM Skew ¹ | T _{sk3} CPU-SDRAM | CPU @ 1.25 V, SDRAM @ 1.5 V | -500 | -15 | 500 | ps |
| Skew Window ¹ | T _{w3} CPU-SDRAM | | 0 | 165 | 500 | ps |
| CPU to 3V66 Skew ¹ | T _{sk3} CPU-3V66 | CPU @ 1.25 V, 3V66 @ 1.5 V | -500 | 165 | 500 | ps |
| Skew Window ¹ | T _{w3} CPU-3V66 | | 0 | 105 | 500 | ps |
| SDRAM to 3V66 Skew ¹ | T _{sk3} SDRAM-3V66 | SDRAM, 3V66 @ 1.5 V | -500 | 185 | 500 | ps |
| Skew Window ¹ | T _{w3} SDRAM-3V66 | | 0 | 185 | 500 | ps |
| 3V66 to PCI Skew ¹ | T _{sk3} 3V66-PCI | 3V66, PCI @ 1.5 V | 1.5 | 2.2 | 3.5 | ns |
| Skew Window ¹ | T _{w3} 3V66-PCI | | 0 | 60 | 500 | ps |
| IOAPIC to PCI Skew ¹ | T _{sk3} IOAPIC-PCI | IOAPIC @ 1.25 V, PCI @ 1.5 V | -1 | -0.1 | 1 | ns |
| Skew Window ¹ | T _{w3} IOAPIC-PCI | | 0 | 0 | 1 | ns |

¹Guaranteed by design, not 100% tested in production.



Group Offset Waveforms



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte **one at a time**.
- Controller (host) sends a Stop bit

| How to Write: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D2 _(H) | |
| | ACK |
| Dummy Command Code | |
| | ACK |
| Dummy Byte Count | |
| | ACK |
| Byte 0 | |
| | ACK |
| Byte 1 | |
| | ACK |
| Byte 2 | |
| | ACK |
| Byte 3 | |
| | ACK |
| Byte 4 | |
| | ACK |
| Byte 5 | |
| | ACK |
| Stop Bit | |

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 5**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

| How to Read: | |
|---------------------------|----------------------|
| Controller (Host) | ICS (Slave/Receiver) |
| Start Bit | |
| Address D3 _(H) | |
| | ACK |
| | Byte Count |
| ACK | |
| | Byte 0 |
| ACK | |
| | Byte 1 |
| ACK | |
| | Byte 2 |
| ACK | |
| | Byte 3 |
| ACK | |
| | Byte 4 |
| ACK | |
| | Byte 5 |
| ACK | |
| Stop Bit | |

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

ICS9250-28



General Layout Precautions:

- 1) Use a ground plane on the top routing layer of the PCB in all areas not used by traces.
- 2) Make all power traces and ground traces as wide as the via pad for lower inductance.

Notes:

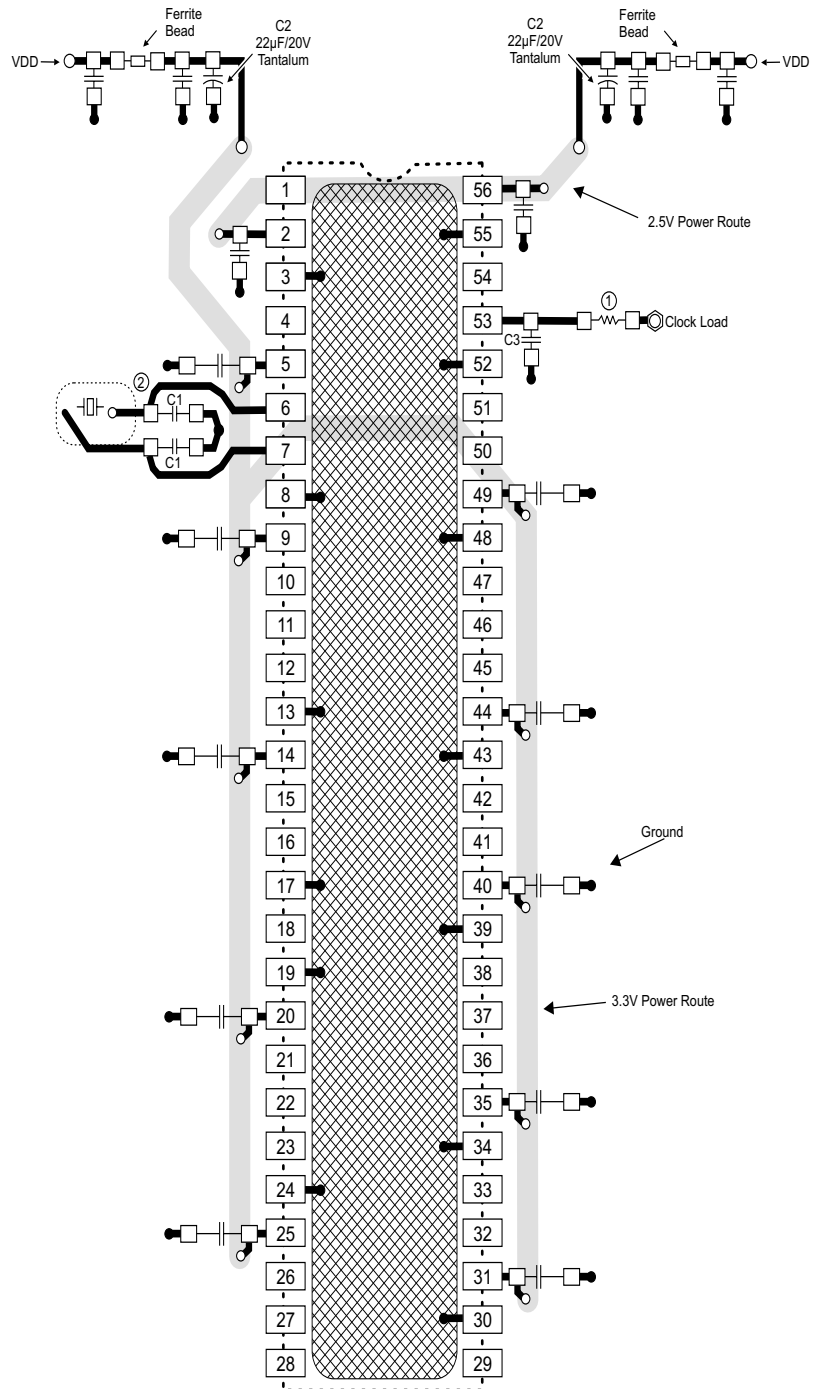
- ① All clock outputs should have provisions for a 15pF capacitor between the clock output and series terminating resistor. Not shown in all places to improve readability of diagram.
- ② Optional crystal load capacitors are recommended. They should be included in the layout but not inserted unless needed.

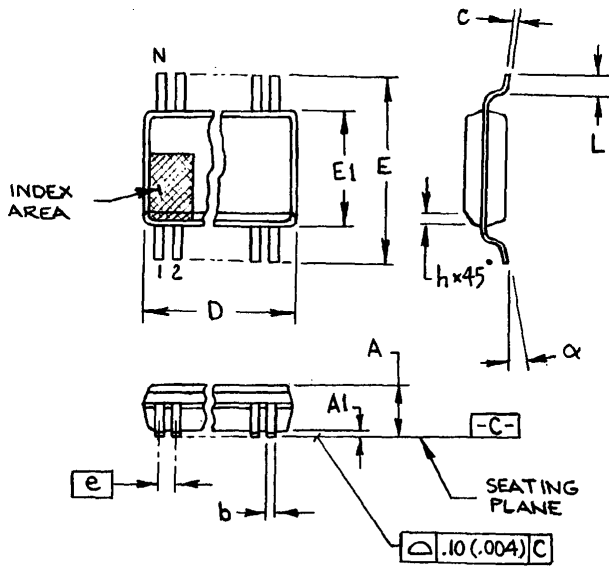
Component Values:

- C1 : Crystal load values determined by user
 C2 : 22 μ F/20V/D case/Tantalum
 AVX TAJD226M020R
 C3 : 15pF capacitor
 FB = Fair-Rite products 2512066017X1
 All unmarked capacitors are 0.01 μ F ceramic

Connections to VDD:

- Best
- Okay
- Avoid
- Avoid





300 mil SSOP

| SYMBOL | In Millimeters | | In Inches | |
|--------|-------------------|--------|-------------------|-------|
| | COMMON DIMENSIONS | | COMMON DIMENSIONS | |
| | MIN | MAX | MIN | MAX |
| A | 2.413 | 2.794 | .095 | .110 |
| A1 | 0.203 | 0.406 | .008 | .016 |
| b | 0.203 | 0.343 | .008 | .0135 |
| c | 0.127 | 0.254 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.033 | 10.668 | .395 | .420 |
| E1 | 7.391 | 7.595 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.381 | 0.635 | .015 | .025 |
| L | 0.508 | 1.016 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

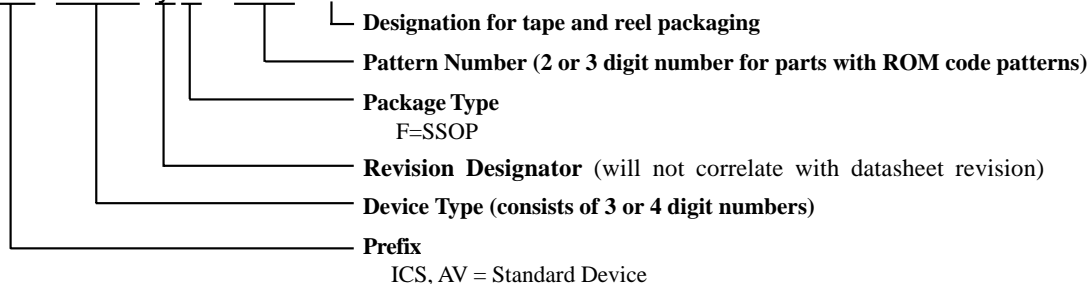
| N | D mm. | | D (inch) | |
|----|--------|--------|----------|------|
| | MIN | MAX | MIN | MAX |
| 28 | 9.398 | 9.652 | .370 | .380 |
| 34 | 11.303 | 11.557 | .445 | .455 |
| 48 | 15.748 | 16.002 | .620 | .630 |
| 56 | 18.288 | 18.542 | .720 | .730 |
| 64 | 20.828 | 21.082 | .820 | .830 |

Ordering Information

ICS9250yF-28-T

Example:

ICS XXXX y F - PPP - T



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.