ICS650-12
MPEG Clock Synthesizer

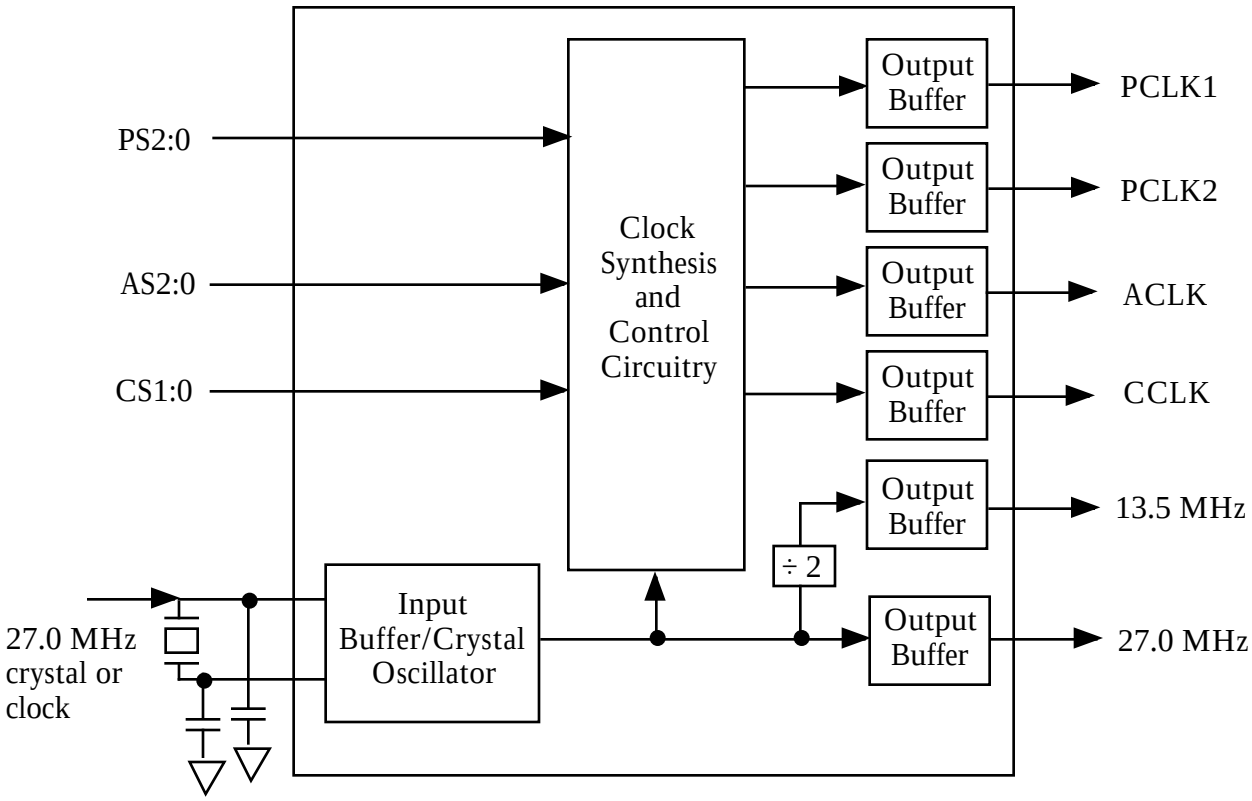
Description

The ICS650-12 is a low cost, low jitter, high performance clock synthesizer designed to produce fixed clock outputs of 13.5 MHz and 27.0 MHz and four selectable clock outputs of two Processor Clocks (PCLK1 and PCLK2), Audio Clock (ACLK), and Communications Clock (CCLK). Using our patented analog Phase-Locked Loop (PLL) techniques, the device uses a 27.0 MHz clock or fundamental crystal input to produce clocks ideal for Digital Video/MPEG-based applications.

Features

- Packaged in 20 pin tiny SSOP (QSOP)
- Input Frequency of 27.0 MHz
- Zero ppm synthesis error in output clocks
- Provides fixed 13.5 MHz and 27.0 MHz. Also provides two selectable Processor Clocks, one Audio Clock, and one Communications Clock
- Ideal for Digital Video/MPEG-based applications
- 3.3 V or 5.0 V operating voltage
- Entire chip powers down (when CS1=CS0=0)

Block Diagram



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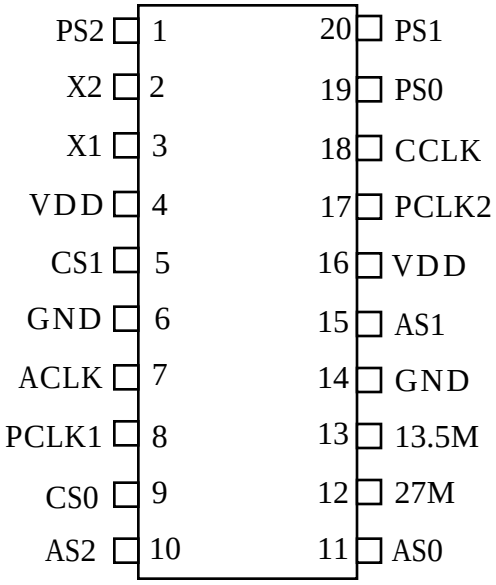
Pin Assignment



20 pin SSOP (QSOP)

PCLK1 and PCLK2 Select Table (in MHz)

PS2	PS1	PS0	PCLK1	PCLK2
0	0	0	108.00	54.00
0	0	1	55.00	27.5
0	1	0	66.67	33.33
0	1	1	80.00	40.00
1	0	0	54.00	27.00
1	0	1	81.00	40.5
1	1	0	50.00	25.00
1	1	1	60.00	30.00

ACLK Select Table (in MHz)

AS2	AS1	AS0	ACLK
0	0	0	12.288
0	0	1	11.2896
0	1	0	8.192
0	1	1	24.576
1	0	0	8.192
1	0	1	16.9344
1	1	0	18.432
1	1	1	11.2896

CCLK Select Table (in MHz)

CS1	CS0	CCLK
0	0	All off*
0	1	20.00
1	0	66.6666
1	1	24.576

*Note: Entire chip powers down (outputs stop low) when CS1 = CS0 = 0.

Pin Descriptions

Pin #	Name	Type	Description
1	PS2	I	Processor Clock Select Pin 2. See above table.
2	X2	XO	Crystal connection to a 27.0 MHz crystal or leave unconnected for clock input
3	X1	XI	Crystal connection. Connect to a 27.0 MHz fundamental mode crystal or clock input.
4, 16	VDD	P	Connect to +3.3 V or +5.0 V.
5	CS1	I	Communications Clock Select Pin 1. See above table.
6, 14	GND	P	Connect to ground.
7	ACLK	O	Audio Clock Output. See above table.
8	PCLK1	O	Processor Clock Output 1. See above table.
9	CS0	I	Communications Clock Select 0. See above table.
10	AS2	I	Audio Clock Select Pin 2. See above table.
11	AS0	I	Audio Clock Select Pin 0. See above table.
12	27M	O	27 MHz buffered clock output.
13	13.5M	O	13.5 MHz clock output.
15	AS1	I	Audio Clock Select Pin 1. See above table.
17	PCLK2	O	Processor Clock Output 2. See above table.
18	CCLK	O	Communications Clock Output. See above table.
19	PS0	I	Processor Clock Select Pin 0. See above table.
20	PS1	I	Prcoessor Clock Select Pin 1. See above table.

Key: I = Input with internal pull-up; O = output; P = power supply connection; XI, XO = crystal connections

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V or 5V unless noted)					
Operating Voltage, VDD		3.0		5.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	VDD=3.3V, IOH=-8mA	2.4			V
Output Low Voltage, VOL	VDD=3.3V, IOL=8mA			0.4	V
Output High Voltage, VOH, VDD = 3.3 or 5V	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD, at 5V	No Load		39		mA
Operating Supply Current, IDD, at 3.3V	No Load		22		mA
Short Circuit Current, VDD = 3.3 V	Each output		±50		mA
Input Capacitance	Except X1		7		pF
AC CHARACTERISTICS (VDD = 3.3V or 5V unless noted)					
Input Crystal or Clock Frequency			27		MHz
Output Clocks Accuracy (synthesis error)	All clocks		0	1	ppm
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40	50	60	%
One Sigma Jitter, ACLK	VDD=3.3 V		100		ps
	VDD=5.0 V		40		ps
Absolute Clock Period Jitter	VDD=3.3 V, Except CCLK=20 MHz		±300		ps
	VDD=5.0 V, Except CCLK=20 MHz		±200		ps

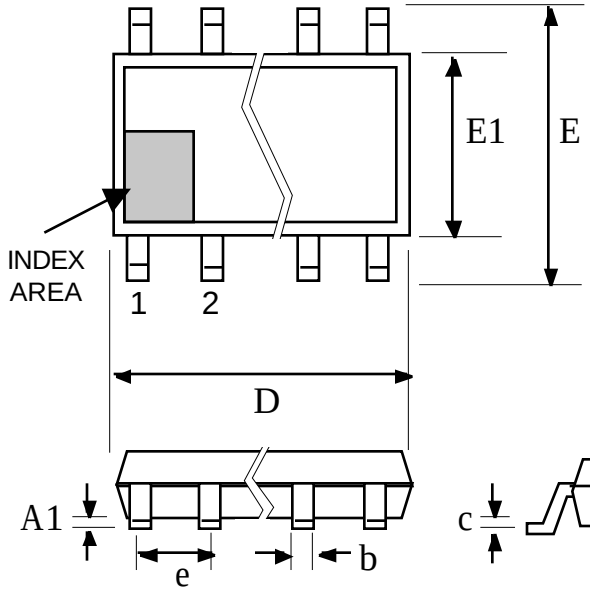
Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 µF should be connected between VDD and GND on pins 4 and 6, and 16 and 14, and a 33 Ω terminating resistor may be used on each clock output if the trace is longer than 1 inch.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



20 pin SSOP

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
D	0.337	0.344	8.55	8.75
e	.025 BSC		0.635 BSC	
E	0.228	0.244	5.80	6.20
E1	0.150	0.157	3.80	4.00
L	0.016	0.050	0.40	1.27

Ordering Information

Part/Order Number	Marking	Package	Shipping	Temperature
ICS650R-12	ICS650R-12	20 pin SSOP	Tubes	0 to 70 °C
ICS650R-12T	ICS650R-12	20 pin SSOP	Tape and Reel	0 to 70 °C

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