



### GENERAL DESCRIPTION



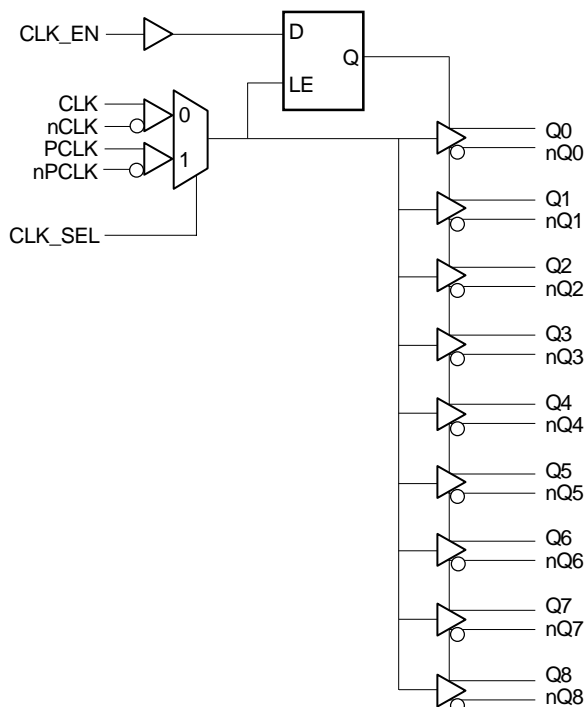
The ICS8531-01 is a low skew, high performance 1-to-9 Differential-to-3.3V LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8531-01 has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output skew and part-to-part skew characteristics make the ICS8531-01 ideal for high performance workstation and server applications.

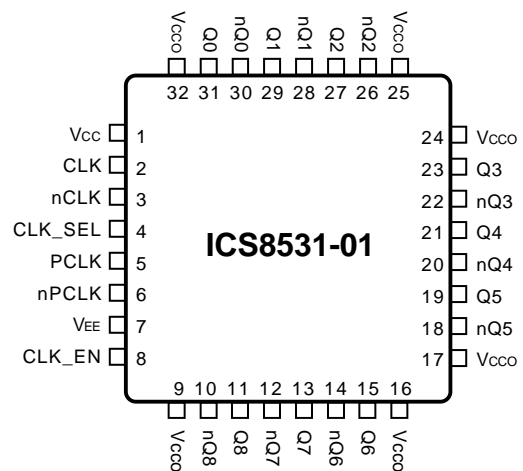
### FEATURES

- 9 differential 3.3V LVPECL outputs
- Selectable CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency up to 500MHz
- Translates any single ended input signal (LVCMOS, LVTTTL, GTL) to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 2ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**32-Lead LQFP**

7mm x 7mm x 1.4mm package body

**Y package**

Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	V <sub>CC</sub>	Power		Positive supply pin. Connect to 3.3V.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup	Inverting differential clock input.
4	CLK_SEL	Input	Pulldown	Clock Select input. When HIGH, selects PCLK, nPCLK inputs. When LOW, selects CLK, nCLK. LVTTTL / LVCMOS interface levels.
5	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
6	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
7	V <sub>EE</sub>	Power		Negative supply pin. Connect to ground.
8	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVTTTL / LVCMOS interface levels.
9, 16, 17, 24, 25, 32	V <sub>CCO</sub>	Power		Output supply pins. Connect to 3.3V.
10, 11	nQ8, Q8	Output		Differential output pair. LVPECL interface level.
12, 13	nQ7, Q7	Output		Differential output pair. LVPECL interface level.
14, 15	nQ6, Q6	Output		Differential output pair. LVPECL interface level.
18, 19	nQ5, Q5	Output		Differential output pair. LVPECL interface level.
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL interface level.
22, 23	nQ3, Q3	Output		Differential output pair. LVPECL interface level.
26, 27	nQ2, Q2	Output		Differential output pair. LVPECL interface level.
28, 29	nQ1, Q1	Output		Differential output pair. LVPECL interface level.
30, 31	nQ0, Q0	Output		Differential output pair. LVPECL interface level.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance	CLK, nCLK, PCLK, nPLCK			4	pF
		CLK_EN, CLK_SEL			4	pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ

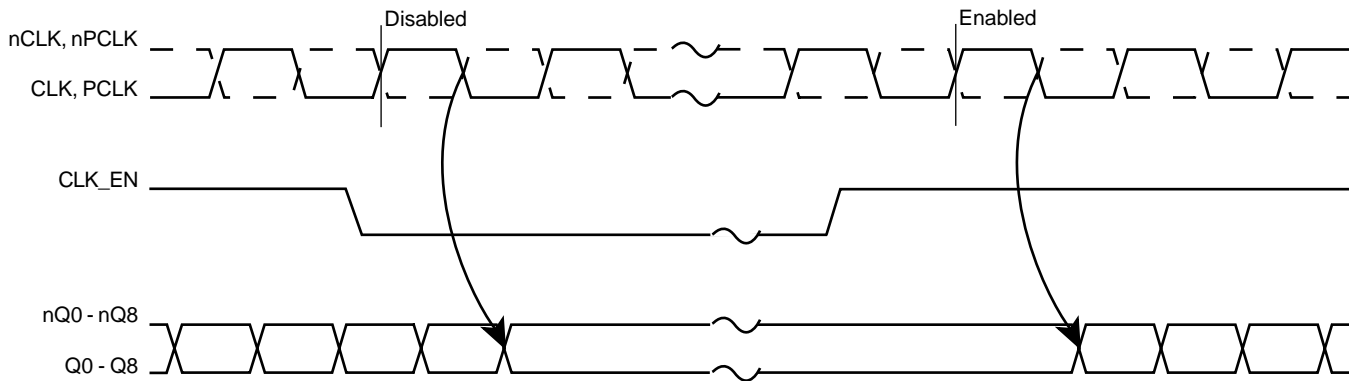


**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Sourced	Q0 thru Q8	nQ0 thru nQ8
0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH
0	1	PCLK, nPCLK	Disabled; LOW	Disabled; HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	PCLK, nPCLK	Enabled	Enabled

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.



**FIGURE 1: CLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUTS FUNCTION TABLE**

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	nCLK or nPCLK	Q0 thru Q8	nQ0 thru nQ8		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section on page 8, Figure 9, which discusses wiring the differential input to accept single ended levels.



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CCx}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{CCO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W
Storage Temperature, $T_{STG}$	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current			50	70	mA

**TABLE 4B. LVCMOS DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	CLK_EN, CLK_SEL		2		3.765	V
$V_{IL}$	CLK_EN, CLK_SEL		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK_EN	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
		CLK_SEL	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	CLK_EN	$V_{IN} = 0V, V_{CC} = 3.465V$	-150		$\mu A$
		CLK_SEL	$V_{IN} = 0V, V_{CC} = 3.465V$	-5		$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-5		$\mu A$
		nCLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for CLK and nCLK is  $V_{CC} + 0.3V$ .

NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PCLK	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		nPCLK	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	PCLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-5		$\mu A$
		nPCLK	$V_{IN} = 0V, V_{CC} = 3.465V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.3		1	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 1.5$		$V_{CC}$	V
$V_{OH}$	Output High Voltage; NOTE 3		$V_{CCO} - 1.4$		$V_{CCO} - 1.0$	V
$V_{OL}$	Output Low Voltage; NOTE 3		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Common mode input voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for PCLK and nPCLK is  $V_{CC} + 0.3V$ .

NOTE 3: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .

**TABLE 5. AC CHARACTERISTICS,  $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Maximum Output Frequency				500	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 250MHz$	1		2	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				50	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				250	ps
$t_R$	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
$t_F$	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		48	50	52	%

All parameters measured at 250MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

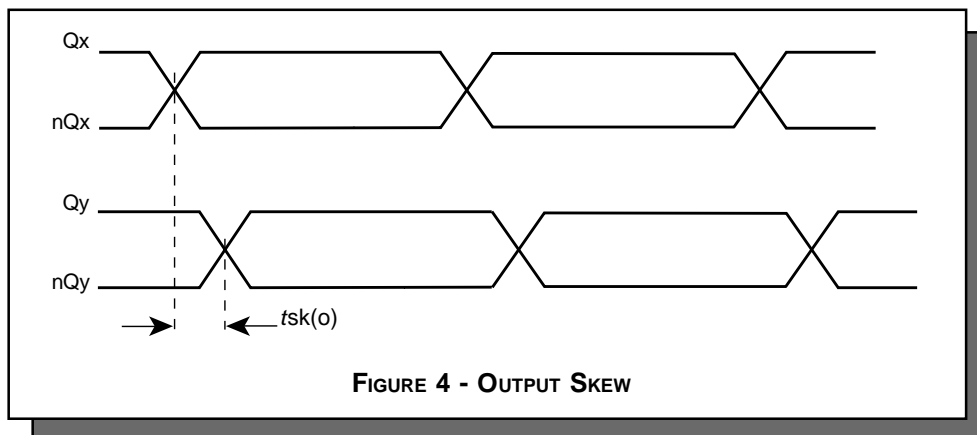
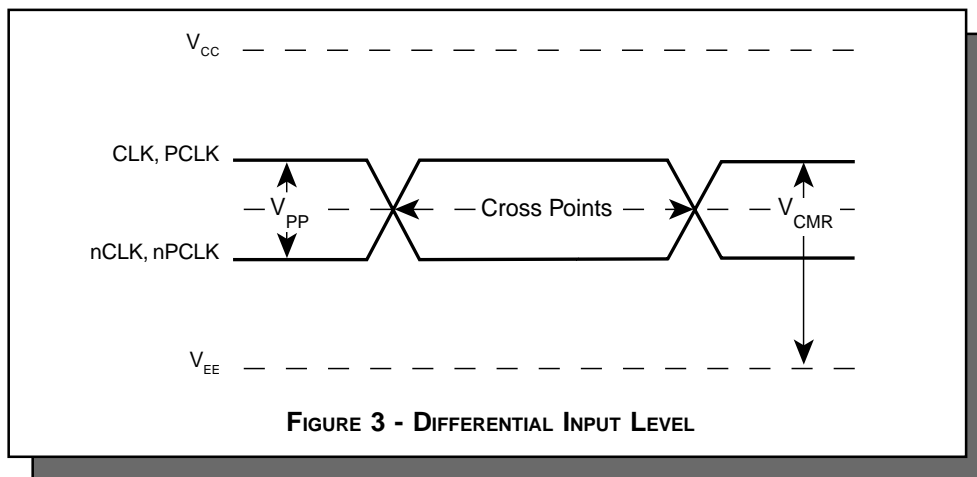
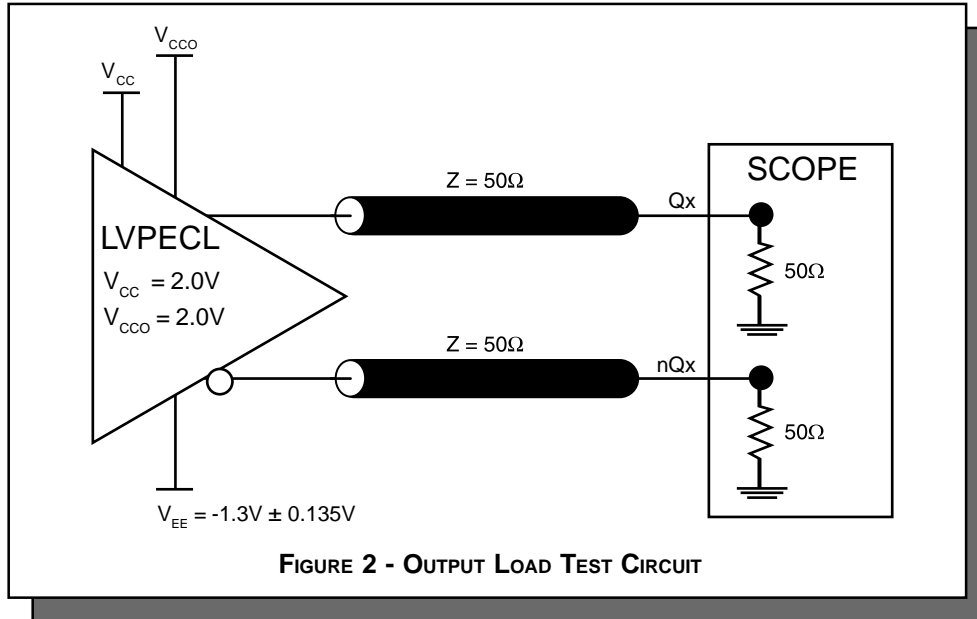
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

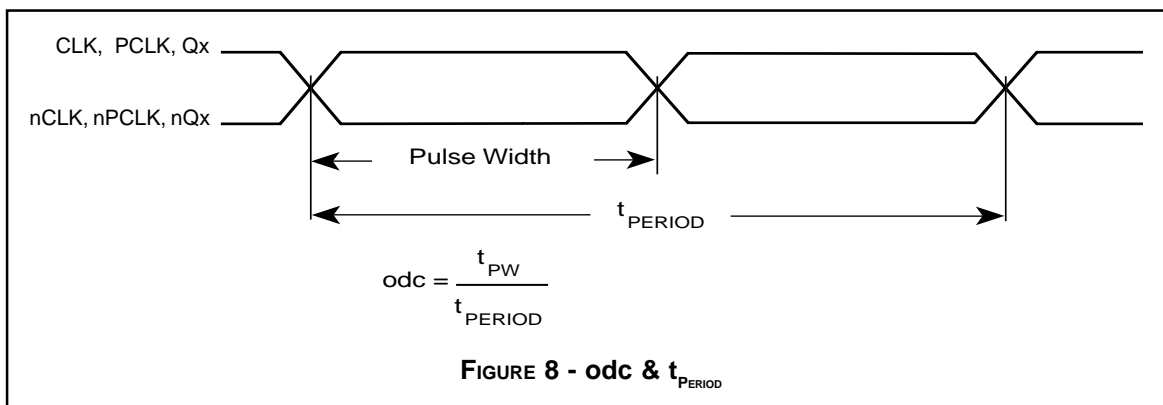
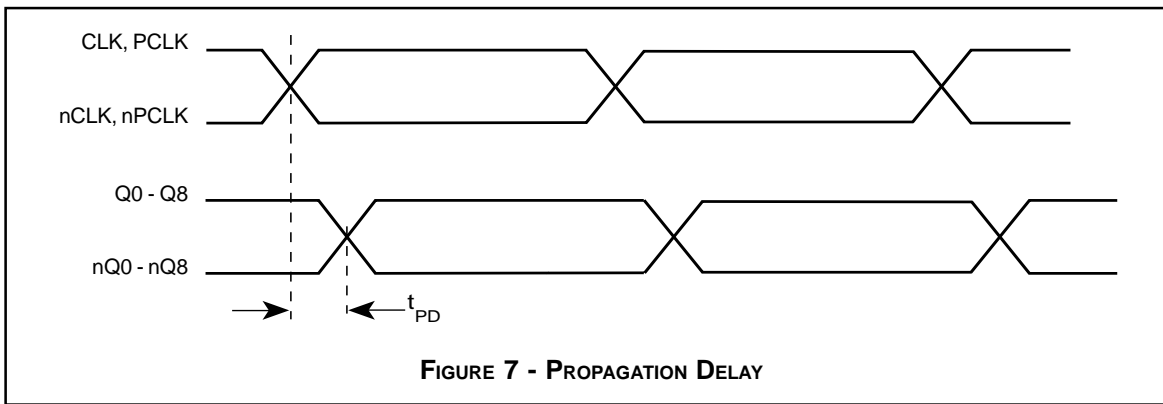
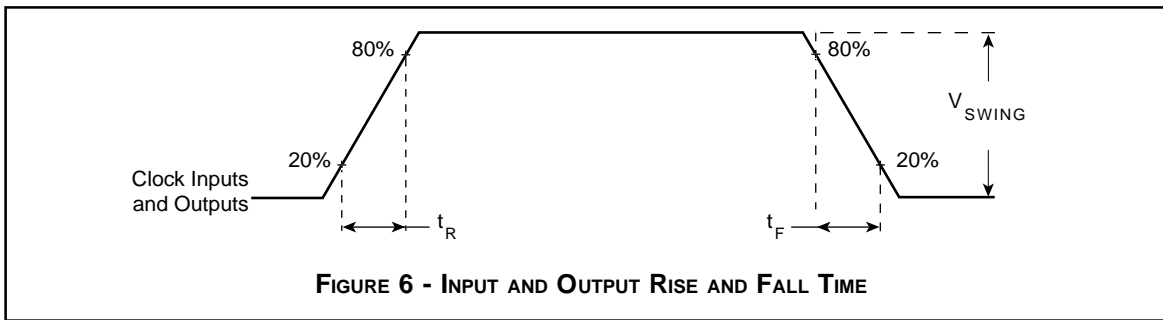
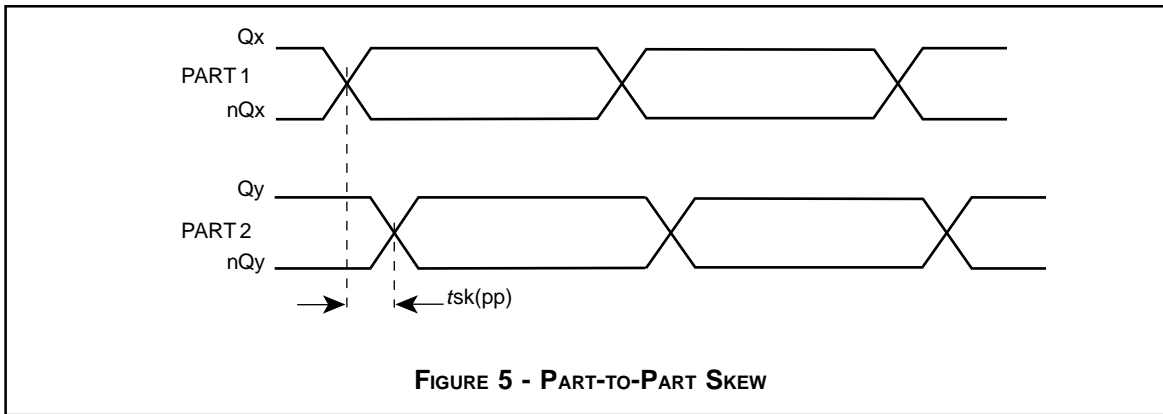
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



## PARAMETER MEASUREMENT INFORMATION



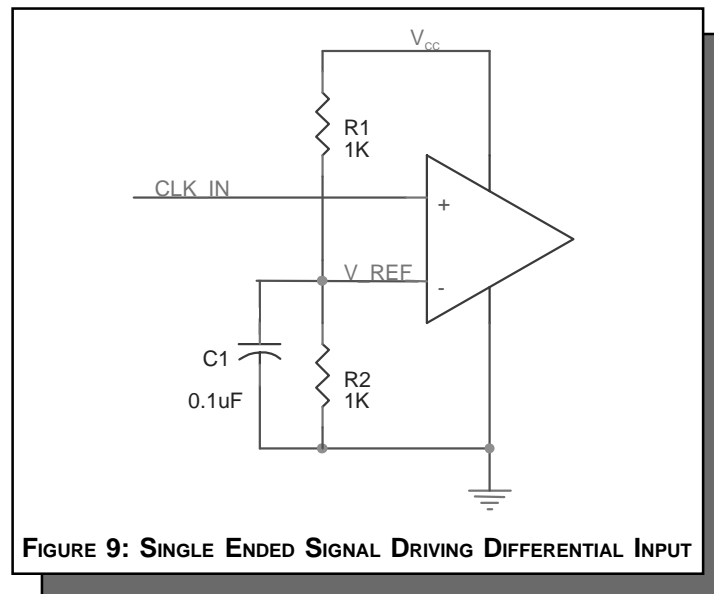




## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 9 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} \approx V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .







## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8531-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8531-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 70mA = \mathbf{242.6mW}$
- Power (outputs)<sub>MAX</sub> = **30.2mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $9 * 30.2mW = \mathbf{271.8mW}$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $242.6mW + 271.8mW = \mathbf{514.4mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-ambient thermal resistance

$Pd\_total$  = Total device power dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.514\text{W} * 42.1^\circ\text{C/W} = 91.6^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 32-pin LQFP Forced Convection**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

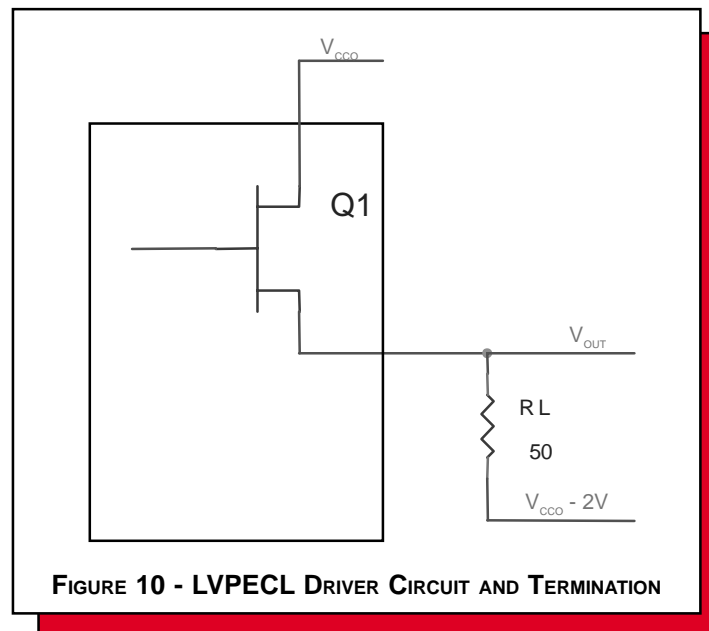
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 10*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

$Pd_H$  is power dissipation when the output drives high.  
 $Pd_L$  is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V)) / R_L] * (V_{CC\_MAX} - V_{OH\_MAX})$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V)) / R_L] * (V_{CC\_MAX} - V_{OL\_MAX})$$

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 1.0V$   
Using  $V_{CC\_MAX} = 3.465$ , this results in  $V_{OH\_MAX} = 2.465V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V$   
Using  $V_{CC\_MAX} = 3.465$ , this results in  $V_{OL\_MAX} = 1.765V$

$$Pd_H = [(2.465V - (3.465V - 2V)) / 50\Omega] * (3.465V - 2.465V) = 20mW$$

$$Pd_L = [(1.765V - (3.465V - 2V)) / 50\Omega] * (3.465V - 1.765V) = 10.2mW$$

Total Power Dissipation per output pair =  $Pd_H + Pd_L = 30.2mW$



## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE

	$\theta_{JA}$ by Velocity (Linear Feet per Minute)		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most all modern PCB designs use multi-layered boards, so the data in the second row will pertain to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8531-01 is: 632



PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX

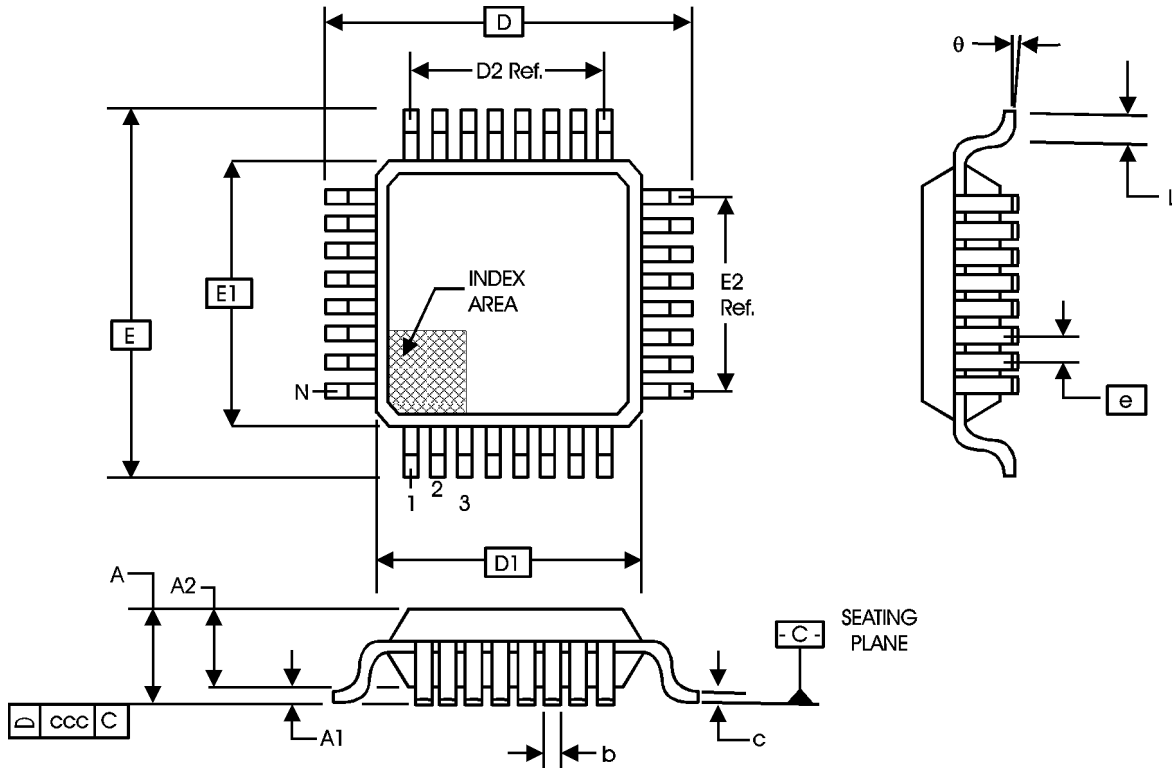


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026



Integrated  
Circuit  
Systems, Inc.

# ICS8531-01

## LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-3.3V LVPECL FANOUT BUFFER

**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS8531AY-01	ICS8531AY-01	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8531AY-01T	ICS8531AY-01	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C

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