



MK3720

27 MHz and 54 MHz 3.3 Volt VCXO

Description

The MK3720 is a low cost, low jitter, high performance 3.3 Volt VCXO and PLL clock synthesizer designed to replace expensive 13.5, 27, or 54MHz VCXOs. The patented on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by ± 100 ppm. Using our patented VCXO and analog/digital Phase-Locked Loop (PLL) techniques, the device uses an inexpensive external 13.5 MHz pullable crystal input to produce output clocks of 13.5 MHz, 27 MHz, and 54 MHz .

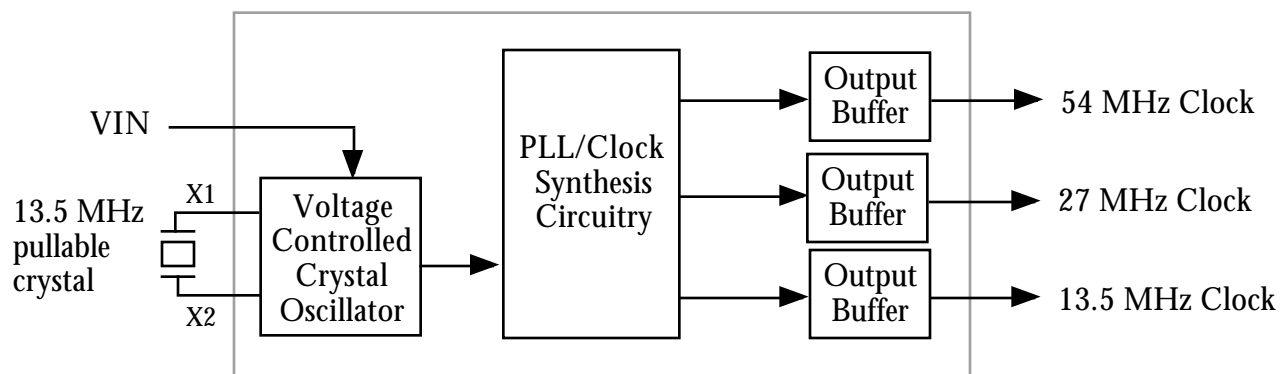
The MK3720A is a drop-in replacement to the earlier MK3720S.

Features



- Packaged in 8 pin SOIC
- 3.3 V only operating voltage
- Output clocks of 54, 27, and 13.5MHz
- Uses an inexpensive 13.500 MHz external crystal
- On-chip patented VCXO with pull range of 200ppm (minimum)
- VCXO tuning voltage of 0 to 3.3 V
- 12 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- The A version is the latest, manufactured in a smaller geometry process. The MK3720A gives a wider pull range than the MK3720S, and so is recommended for all new designs, and cost reductions of existing designs.

Block Diagram

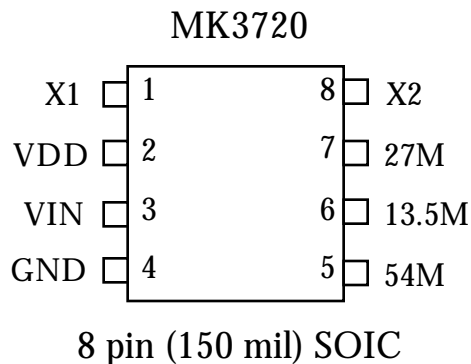




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Pin Assignment



Pin Descriptions

| Number | Name | Description |
|--------|-------|---|
| 1 | X1 | Crystal connection. Connect to a pullable 13.5 MHz crystal. |
| 2 | VDD | VDD. Connect to +3.3 V. |
| 3 | VIN | Voltage input to VCXO. Zero to 3.3 V analog input which controls the frequency of the VCXO. |
| 4 | GND | Connect to ground. |
| 5 | 54M | 54 MHz VCXO clock output. |
| 6 | 13.5M | 13.5 MHz VCXO clock output. |
| 7 | 27M | 27 MHz VCXO clock output. |
| 8 | X2 | Crystal connection. Connect to a pullable 13.5 MHz crystal. |

Pullable Crystal Specifications:

| | |
|----------------------------------|------------|
| Correlation (load) Capacitance | 14 pF |
| C0/C1 | 240 max |
| ESR | 35 max |
| Operating Temperature | 0 to 70 °C |
| Initial Accuracy | ±20 ppm |
| Temperature plus Aging Stability | ±50 ppm |



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Electrical Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|--|-------------------|---------|----------|---------|-------|
| ABSOLUTE MAXIMUM RATINGS (note 1) | | | | | |
| Supply voltage, VDD | Referenced to GND | | | 7 | V |
| Inputs and Clock Outputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Ambient Operating Temperature | | 0 | | 70 | °C |
| Soldering Temperature | Max of 10 seconds | | | 260 | °C |
| Storage temperature | | -65 | | 150 | °C |
| DC CHARACTERISTICS (VDD = 3.3 V unless noted) | | | | | |
| Operating Voltage, VDD | | 3.15 | | 3.45 | V |
| Output High Voltage, VOH | IOH=-12mA | 2.4 | | | V |
| Output Low Voltage, VOL | IOL=12mA | | | 0.4 | V |
| Output High Voltage, VOH, CMOS level | IOH=-4mA | VDD-0.4 | | | V |
| Operating Supply Current, IDD | No Load | | 11 | | mA |
| Short Circuit Current | | | ±50 | | mA |
| VIN, VCXO control voltage | | 0 | | 3.3 | V |
| AC CHARACTERISTICS (VDD = 3.3 V unless noted) | | | | | |
| Input Crystal Frequency | | | 13.50000 | | MHz |
| Output Clock Rise Time | 0.8 to 2.0V | | | 1.5 | ns |
| Output Clock Fall Time | 2.0 to 0.8V | | | 1.5 | ns |
| Output Clock Duty Cycle | At 1.4V | 45 | 50 | 55 | % |
| Maximum Absolute Jitter, short term | | | 100 | | ps |
| Output pullability, note 2 | 0V VIN 3.3 V | ±100 | | | ppm |

- Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
 2. With an ICS approved pullable crystal. The MK3720A has a typical pull range of ±180 ppm.

External Components

The MK3720 requires a minimum number of external components for proper operation. A decoupling capacitor of 0.01µF should be connected between VDD and GND on pins 2 and 4, as close to the MK3720 as possible. A series termination resistor of 33 Ω may be used for the clock output. The input crystal must be connected as close to the chip as possible. The input crystal should be a parallel mode, pullable, AT cut, 13.5 MHz, with 14 pF load capacitance. Consult ICS for recommended suppliers. **IMPORTANT** - read application note MAN05 before laying out the PCB.



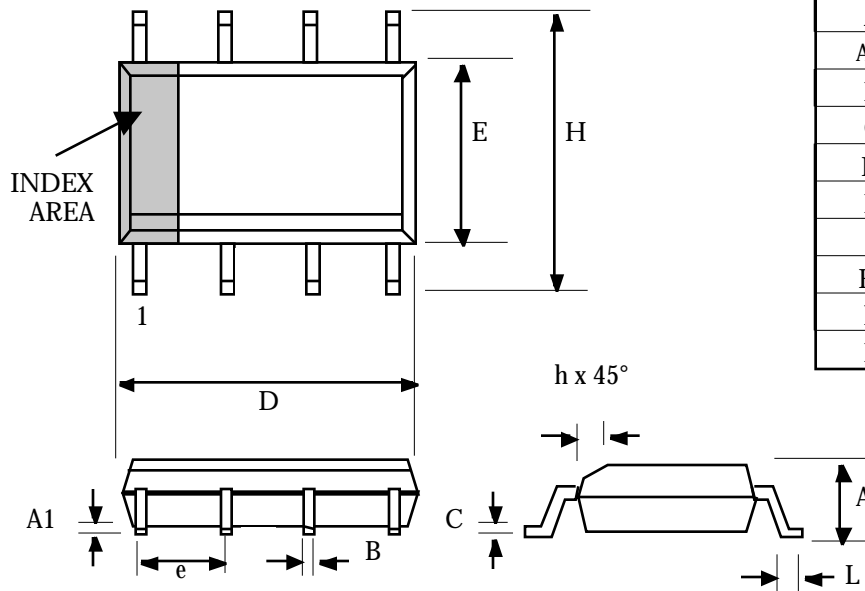
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Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

8 pin SOIC



| Symbol | Inches | | Millimeters | |
|--------|----------|--------|-------------|------|
| | Min | Max | Min | Max |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.24 |
| B | 0.0130 | 0.0200 | 0.33 | 0.51 |
| C | 0.0075 | 0.0098 | 0.19 | 0.24 |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 |
| e | .050 BSC | | 1.27 BSC | |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 |
| h | 0.0099 | 0.0195 | 0.25 | 0.50 |
| L | 0.0160 | 0.0500 | 0.41 | 1.27 |

Ordering Information

| Part/Order Number | Marking | Shipping packaging | Package | Temperature |
|-------------------|---------|--------------------|------------|-------------|
| MK3720A | MK3720A | tubes | 8 pin SOIC | 0-70 °C |
| MK3720ATR | MK3720A | Tape and reel | 8 pin SOIC | 0-70 °C |
| MK3720S | MK3720S | tubes | 8 pin SOIC | 0-70 °C |
| MK3720STR | MK3720S | Tape and reel | 8 pin SOIC | 0-70 °C |

CHANGE HISTORY

| Version | Date first published | Status | Comments |
|---------|----------------------|-------------|---|
| D | 5/31/00 | | Added A version |
| C | 12/29/99 | Released | Changed to JEDEC dimensions. Changed VDD to ±5%. Added Crystal specs. |
| B | 5/25/99 | Preliminary | Updated specs for crystal capacitance, IDD, jitter. |
| A | 4/19/99 | Preliminary | Original |

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