PA7024 PEEL™ Array

Programmable Electrically Erasable Logic Array

Features

- **CMOS Electrically Erasable Technology**
  - Reprogrammable in 24-pin DIP, SOIC and 28-pin PLCC packages
  - -Optional JN package for 22V10 power/ground compatibility
- **Most Powerful 24-pin PLD Available**
  - 20 I/Os, 2 inputs/clocks, 40 registers/latches
  - 40 logic cell output functions
  - PLA structure with true product-term sharing
  - Logic functions and registers can be I/O-buried
- **Flexible Logic Cell**
  - Multiple output functions per cell
  - D,T and JK registers with special features
  - Independent or global clocks, resets, presets, clock polarity and output enables
  - -Sum of products logic for output enable
- **High-Speed Commercial and Industrial Versions**
  - As fast as 10ns/15ns (tpdi/tpdx), 71.4MHz (fMAX)
  - Industrial grade available for 4.5 to 5.5V Vcc and -40 to +85°C temperatures
- **Ideal for Combinatorial, Synchronous and Asynchronous Logic Applications**
  - Integration of multiple PLDs and random logic
  - Buried counters, complex state-machines
  - Comparators, decoders, multiplexers and other wide-gate functions
- **Development and Programmer Support**
  - ICT PLACE Development Software
  - Fitters for ABEL, CUPL and other software
  - -Programming support by ICT PDS-3 and popular third-party programmers

General Description

The PA7024 is a member of the Programmable Electrically Erasable Logic (PEEL™) Array family based on ICT's CMOS EEPROM technology. PEEL™ Arrays free designers from the limitations of ordinary PLDs by providing the architectural flexibility and speed needed for today's programmable logic designs. The PA7024 is by far the most powerful 24-pin PLD available today with 20 I/O pins, 2 input/global-clocks and 40 registers/latches (20 buried logic cells and 20 I/O registers/latches). Its logic array implements 84 sum-of-product logic functions that share 80 product terms. The PA7024's logic and I/O cells (LCCs, IOCs) are extremely flexible, offering two output functions per logic cell (a total of 40 for all 20 logic cells). Logic cells are configurable as D, T, and JK registers with independent or global clocks, resets, presets, clock polarity, and other special features. This makes them suitable for a wide variety of combinatorial, synchronous and asynchronous logic applications. With pin compatibility and super-set functionality to most 24-pin PLDs, (22V10, EP610/630, GAL6002), the PA7024 can implement designs that exceed the architectures of such devices. The PA7024 supports speeds as fast as 10ns/15ns (tpdi/tpdx) and 71.4MHz (fMAX) at moderate power consumption 120mA (85mA typical). Packaging includes 24-pin DIP, SOIC and 28-pin PLCC (see Figure 1). Development and programming support for the PA7024 is provided by ICT and popular third-party development tool manufacturers.

Figure 1: Pin Configuration

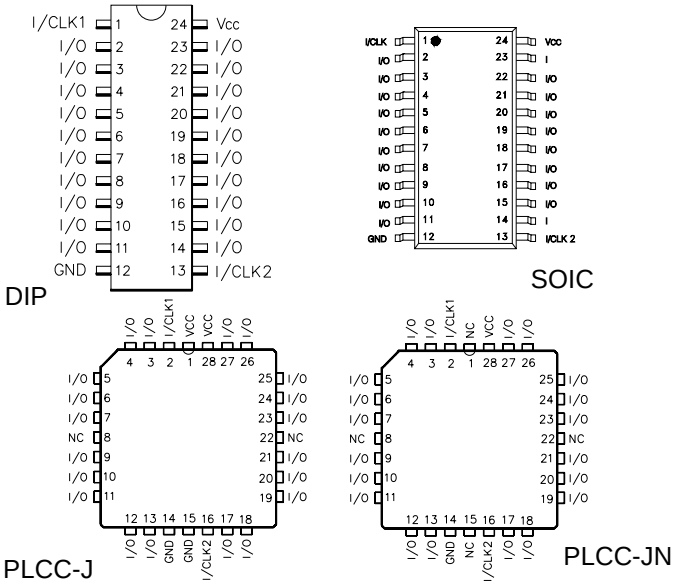
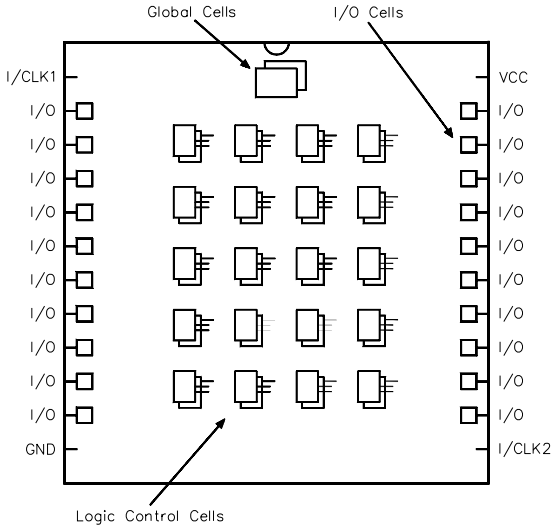


Figure 2. Block Diagram



This device has been designed and tested for the recommended operating conditions. Proper operation outside these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 7.0	V
V_I, V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to V_{CC} + 0.6	V
I_O	Output Current	Per pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Table 2. Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	
T_A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T_R	Clock Rise Time	See Note 2		20	ns
T_F	Clock Fall Time	See Note 2		20	ns
T_{RVCC}	V_{CC} Rise Time	See Note 2		250	ms

Table 3. D.C. Electrical Characteristics over the recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = -4.0mA		2.4		V
V_{OHC}	Output HIGH Voltage - CMOS	V_{CC} = Min, I_{OH} = -10µA		V_{CC} - 0.3		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 16mA			0.5	V
V_{OLC}	Output LOW Voltage - CMOS	V_{CC} = Min, I_{OL} = 10µA			0.15	V
V_{IH}	Input HIGH Level			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level			-0.3	0.8	V
I_{IL}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ V_{CC}			±10	µA
I_{OZ}	Output Leakage Current	I/O = High-Z, GND ≤ V_O ≤ V_{CC}			±10	µA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = 5V, V_O = 0.5V, T_A= 25°C		-30	-120	mA
I_{CC}[11]	V_{CC} Current	V_{IN} = 0V or V_{CC}[3,11] f = 25MHz All outputs disabled[4]	-15	85 (typ.)[17]	120	mA
			-20		120	
			-25		120	
			I-25		130	
C_{IN}[7]	Input Capacitance[5]	T_A = 25°C, VCC = 5.0V @ f = 1 MHz			6	pF
C_{OUT}[7]	Output Capacitance[5]				12	pF

Table 1. A.C Electrical Characteristics Combinatorial

Over the operating range

Symbol	Parameter[6,12]	-15		-20		I -25		Unit
		Min	Max	Min	Max	Min	Max	
tPDI	Propagation delay Internal (tAL + tLC)		10		13		17	ns
tPDX	Propagation delay External (tIA + tAL +tLC + tLO)		15		20		25	ns
tIA	Input or I/O pin to array input		2		2		2	ns
tAL	Array input to LCC		9		12		16	ns
tLC	LCC input to LCC output[10]		1		1		1	ns
tLO	LCC output to output pin		3		5		6	ns
tOD, tOE	Output Disable, Enable from LCC output[7]		3		5		6	ns
tOX	Output Disable, Enable from input pin[7]		15		20		25	ns

Combinatorial Timing - Waveforms and Block Diagram

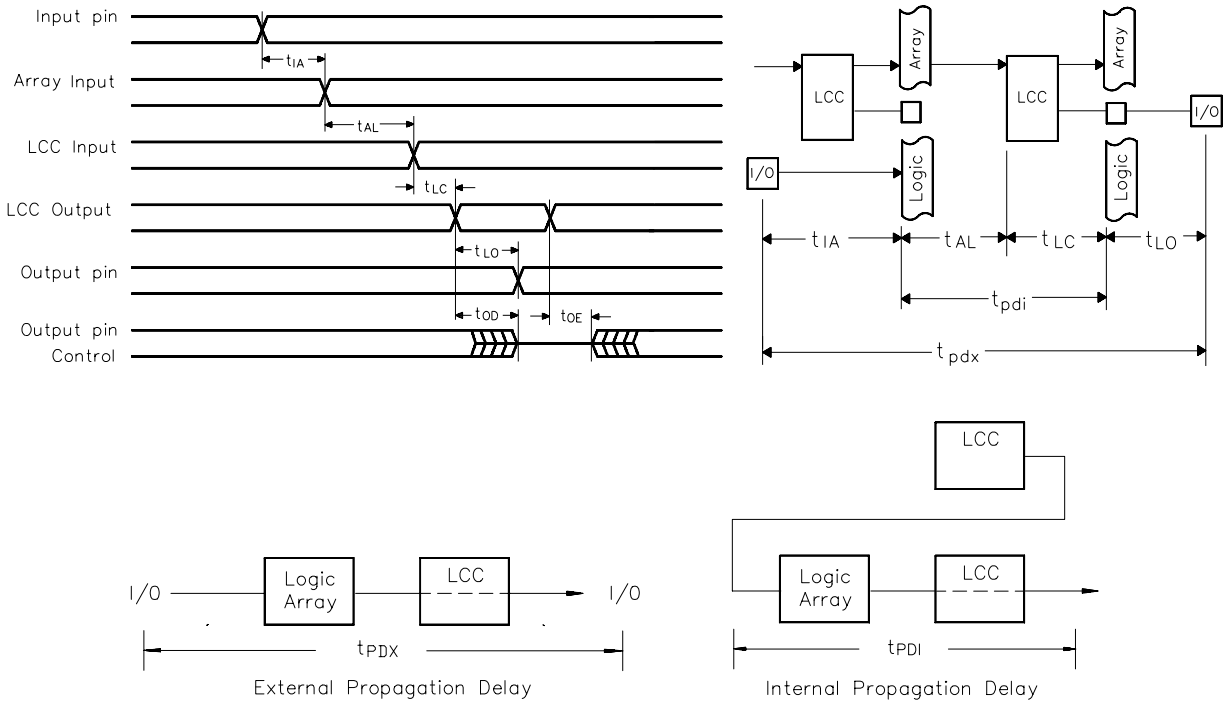
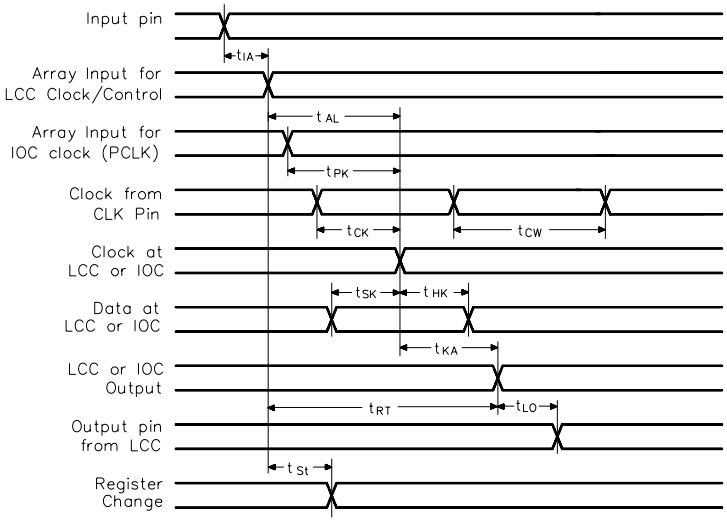
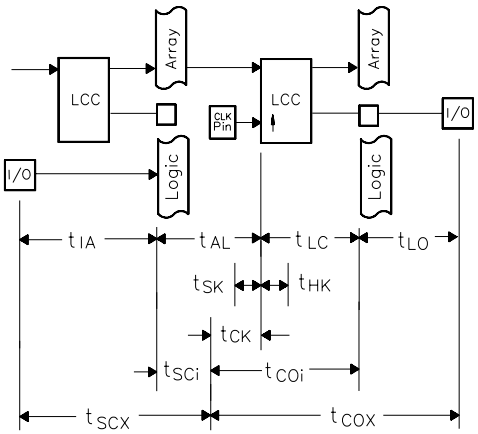


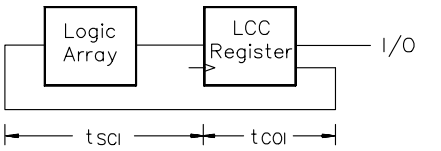
Table 1. A.C. Electrical Characteristics Sequential over the operating range

Symbol	Parameter[6,12]	-15		-20		I-25		Unit
		Min	Max	Min	Max	Min	Max	
tSCI	Internal set-up to system clock[8] - LCC[14] (tAL + tSK + tLC - tCK)	6		9		15		ns
tSCX	Input[16] (EXT.) set-up to system clock, - LCC (tIA + tSCI)	8		11		17		ns
tCOI	System-clock to Array Int. - LCC/IOC/INC[14] (tCK +tLC)		8		8		8	ns
tCOX	System-clock to Output Ext. - LCC (tCOI + tLO)		12		13		13	ns
tHX	Input hold time from system clock - LCC	0		0		0		ns
tSK	LCC Input set-up to async. clock[13] - LCC	3		3		4		ns
tAK	Clock at LCC or IOC - LCC output	1		1		1		ns
tHK	LCC input hold time from system clock - LCC	4		4		4		ns
tSI	Input set-up to system clock - IOC/INC[14] (tSK - tCK)	0		0		0		ns
tHI	Input hold time from system clock - IOC/INC[14] (tSK - tCK)	4		4		4/3		ns
tPK	Array input to IOC PCLK clock		6		7		9	ns
tSPI	Input set-up to PCLK clock[18] - IOC/INC (tSK-tPK-tIA)[16]	0		0		0		ns
tHPI	Input hold from PCLK clock[18] - IOC/INC (tPK+tIA-tSK)[16]	5		6		7		ns
tCK	System-clock delay to LCC/IOCINC		7		7		7	ns
tCW	System-clock low or high pulse width	7		7		8		ns
fMAX1	Max. system-clock frequency Int/Int 1/(tSCI + tCOI)		71.4		58.8		43.5	MHz
fMAX2	Max. system-clock frequency Ext/Int 1/(tSCX + tCOI)		62.5		52.6		40.0	MHz
fMAX3	Max. system-clock frequency Int/Ext 1/(tSCI + tCOX)		55.5		45.5		35.7	MHz
fMAX4	Max. system-clock frequency Ext/Ext 1/(tSCX + tCOX)		50.0		41.6		33.3	MHz
fTGL	Max. system-clock toggle frequency 1/(tCW + tCW)[9]		71.4		71.4		62.5	MHz
tPR	LCC presents/reset to LCC output		1		1		2	ns
tST	Input to Global Cell present/reset (tIA + tAL + tPR)		12		15		20	ns
tAW	Asynch. preset/reset pulse width	8		8		8		ns
tRT	Input to LCC Reg-Type (RT)		6		8		10	ns
tRTV	LCC Reg-Type to LCC output register change		1		1		2	ns
tRTC	Input to Global Cell register-type change (tRT + tRTV)		7		9		12	ns
tRW	Asynch. Reg-Type pulse width	10		10		10		ns
tRESET	Power-on reset time for registers in clear state[2]		5		5		5	µs

Sequential Timing - Waveforms and Block Diagram

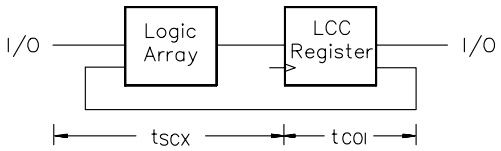






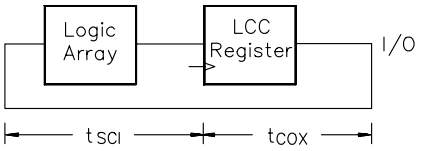
Internal Set–up, Internal Feedback (Int/Int)

$f_{MAX1} = 1/t_{SCI} + t_{COI}$



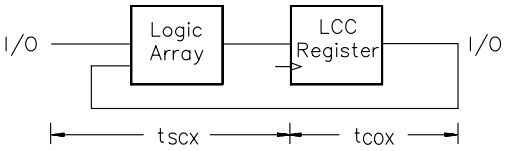
External Set–up, Internal Feedback (Ext/Int)

$f_{MAX2} = 1/t_{SCX} + t_{COI}$



Internal Set–up, External Feedback (Int/Ext)

$f_{MAX3} = 1/t_{SCI} + t_{COX}$



External Set–up, External Feedback (Ext/Ext)

$f_{MAX4} = 1/t_{SCX} + t_{COX}$

Notes

1. Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns.
2. Test points for Clock and V_{CC} in t_R,t_F,t_{CL},t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
3. I/O pins are 0V or V_{CC}.
4. Test one output at a time for a duration of less than 1 sec.
5. Capacitances are tested on a sample basis.
6. Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
7. t_{OE} is measured from input transition to V_{REF} ±0.1V (See test loads for V_{REF} value). t_{OD} is measured from input transition to V_{OH} -0.1Vor V_{OL} +0.1V.
8. “System-clock” refers to pin 1 or 13 (2 or 16 PLCC) high speed clocks.
9. For T or JK registers in toggle (divide by 2) operation only.
10. For combinatorial and async-clock to LCC output delay.
11. I_{CC} for a typical application: This parameter is tested with the device programmed as a 10-bit D-type counter.
12. Test loads are specified in Section 5 of this Data Book.
13. “Async. clock” refers to the clock from the Sum term (OR gate).
14. The “LCC” term indicates that the timing parameter is applied to the LCC register. The “IOC” term indicates that the timing parameter is applied to the IOC register. The “LCC/IOC/INC” term indicates that the timing parameter is applied to both the LCC, IOC and INC registers.
15. The term “Input” without any reference to another term refers to an (external) input pin.
16. The parameter t_{SPI} indicates that the PCLK signal to the IOC register is always slower than the data from the pin or input by the absolute value of (t_{SK} -t_{PK} -t_{IA}). This means that no set-up time for the data from the pin or input is required, i.e. the external data and clock can be sent to the device simultaneously. Additionally, the data from the pin must remain stable for t_{HPI} time, i.e. to wait for the PCLK signal to arrive at the IOC register.
17. Typical (typ) I_{CC} is measured at T_A =25°C, Freq = 25MHz, V_{CC} =5V.

Ordering Information

Part Number	Speed	Temperature	Package
PA7024P-15	10/15ns	C	P24
PA7024J-15			J28
PA7024JN-15			JN28
PA7024S-15			S24
PA7024P-20	13/20ns	C	P24
PA7024J-20			J28
PA7024JN-20			JN28
PA7024S-20			S24
PA7024PI-25	17/25ns	I	P24
PA7024JI-25	17/25ns	I	J28
PA7024JNI-25	17/25ns	I	JN28
PA7024SI-25	17/25ns	I	S24

Part Number