PEEL™ 22LV10AZ-25 / I-35
CMOS Programmable Electrically Erasable Logic Device

Features

- **Low Voltage, Ultra Low Power Operation**
  - Vcc = 2.7 to 3.6 V
  - Icc = 5 µA (typical) at standby
  - Icc = 1.5 mA (typical) at 1 MHz
  - Meets JEDEC LV Interface Spec (JESD8-B)
  - 5 Volt tolerant inputs and I/O's
- **CMOS Electrically Erasable Technology**
  - Superior factory testing
  - Reprogrammable in plastic package
  - Reduces retrofit and development costs
- **Application Versatility**
  - Replaces random logic
  - Super set of standard PLDs
  - Pin and JEDEC compatible with 22V10
  - Ideal for battery powered systems
  - Replaces expensive oscillators
- **Architectural Flexibility**
  - Enhanced architecture fits in more logic
  - 133 product terms x 44 input AND array
  - 12 inputs and 10 I/O pins
  - 12 possible macrocell configurations
  - Asynchronous clear, synchronous preset
  - Independent output enables
  - Programmable clock; pin 1 or p-term
  - Programmable clock polarity
  - 24-Pin DIP/SOIC/TSSOP and 28 Pin PLCC
  - Schmitt triggers on clock and data inputs
- **Schmitt Trigger Inputs**
  - Eliminates external Schmitt trigger devices
  - Ideal for encoder designs

General Description

The PEEL22LV10AZ is a Programmable Electrically Erasable Logic (PEEL) SPLD (Simple Programmable Logic Device) that operates over the supply voltage range of 2.7V-3.6V and features ultra-low, automatic "zero" power-down operation. The PEEL22LV10AZ is logically and functionally similar to ICT's 5V PEEL22CV10A and PEEL22CV10AZ. The "zero power" (25 µA max. I_{CC}) power-down mode makes the PEEL22LV10AZ ideal for a broad range of battery-powered portable equipment applications, from hand-held meters to PCMCIA modems. EE-reprogrammability provides both the convenience of product fast reprogramming for product development and quick personalization in manufacturing, including Engineering Change Orders.

The differences between the PEEL22LV10AZ and PEEL22CV10A include the addition of programmable clock polarity, p-term clock, and Schmitt trigger input buffers on all inputs, including the clock. Schmitt trigger inputs allow direct input of slow signals such as biomedical and sine waves or clocks. Like the PEEL22CV10A, the PEEL22LV10AZ is a pin and JEDEC compatible, logical superset of the industry standard PAL22V10 SPLD Figure 1. The PEEL22LV10AZ provides additional architectural features that allow more logic to be incorporated into the design. The PEEL22LV10AZ architecture allows it to replace over twenty standard 24-pin DIP, SOIC, TSSOP and PLCC packages.

Figure 1 - Pin Configuration

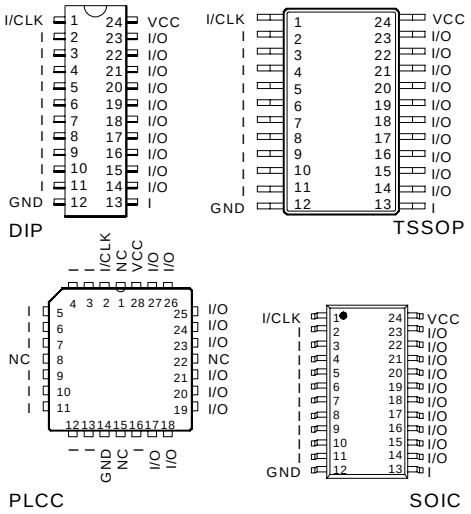
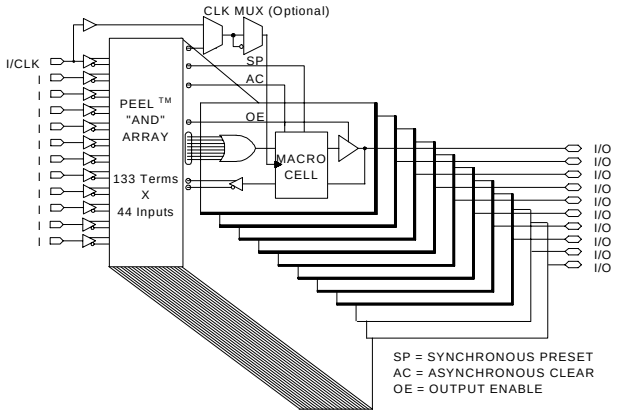


Figure 2 - Block Diagram



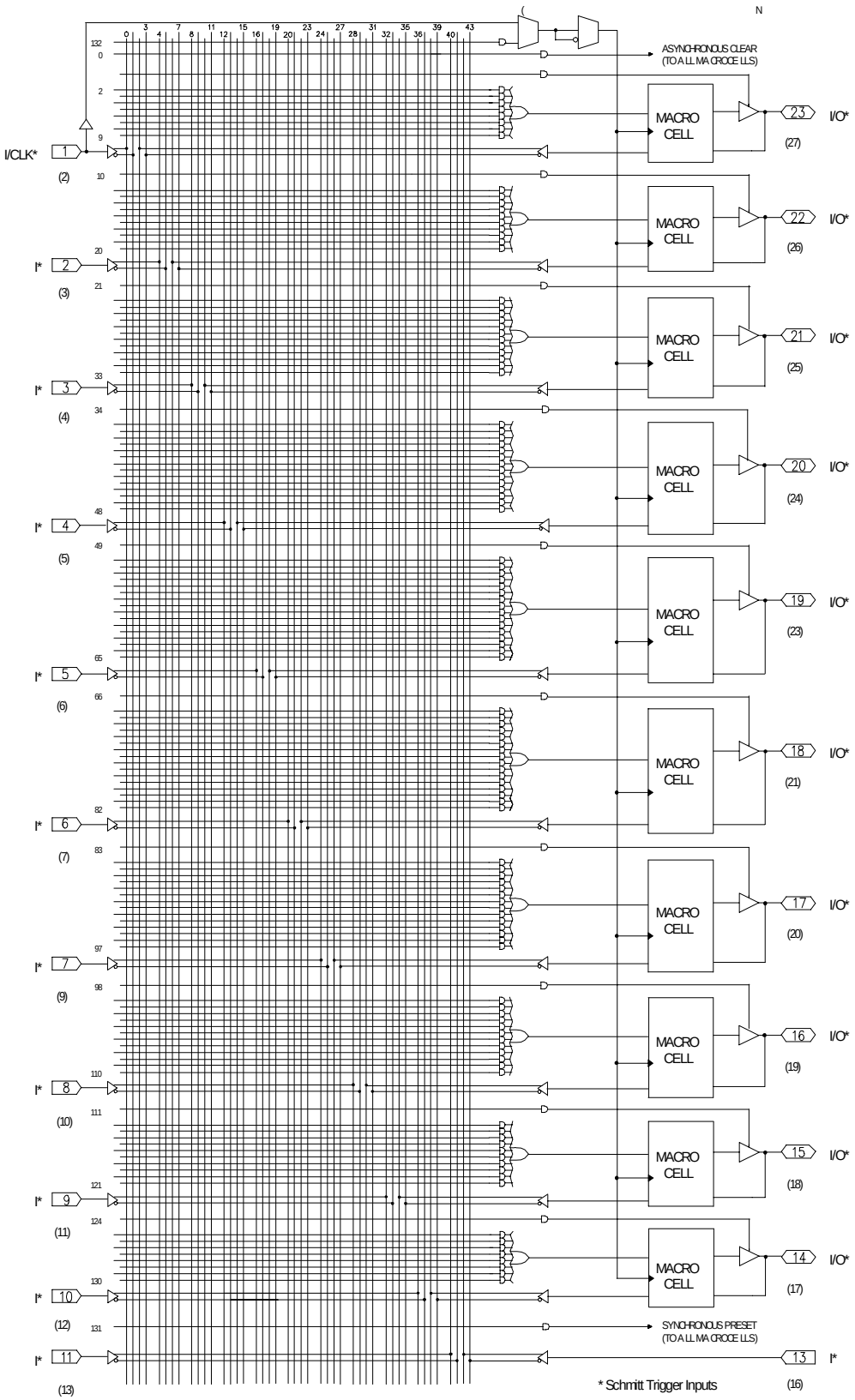


Figure 3 - PEEL22LV10AZ Logic Array Diagram

Function Description

The PEEL22LV10AZ implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

ICT has added optional enhanced capabilities to the PEEL22CV10A family of products with additional features and added fuses to support them. Please view the comparison chart found below for the best algorithm

Algorithms	PEEL V10A Algorithm	PEEL V10A+ Algorithm	PEEL V10A++ Algorithm
Number of Fuses	5828	5873	5958
Supported Features	Standard 22V10 JEDEC Compatible 4 macrocell options	Superset of standard 22V10 12 macrocell options 3 byte signature word Security bit	Superset of standard 22V10 (recommended for new designs) 12 macrocell options 8 byte signature word Security bit Clock source selection Clock polarity selection

Table 1 - Programming Algorithm Comparison

Architecture Overview

The PEEL22LV10AZ architecture is illustrated in the block diagram of Figure 2. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically erasable AND array that drives a fixed OR array. With this structure, the PEEL22LV10AZ can implement up to 10 sum-of-products logic expressions.

Associated with each of the ten OR functions is an I/O macrocell that can be independently programmed to one of 12 different configurations, including the four standard 22V10 modes. The programmable macrocells allow each I/O to be used to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL22LV10AZ (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

- **44 Input Lines:**
  - 24 input lines carry the true and complement of the signals applied to the 12 input pins
  - 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os
- **133 Product Terms:**
  - 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) are used to form sum of product functions
  - 10 outputs enable terms (one for each I/O)
  - 1 global synchronous preset term
  - 1 global asynchronous clear term
  - 1 programmable clock term

At each input-line/product-term intersection, there is an EEPROM memory cell that determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term that is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE.

When programming the PEEL22LV10AZ, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function).

Programmable I/O Macrocell
The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently lets you to tailor the configuration of the PEEL22LV10AZ to the precise requirements of your design.

Macrocell Architecture
Each I/O macrocell, as shown in Figure 4, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine output polarity, output type (registered or non-registered) and input-feedback path (bidirectional I/O, combinatorial feedback). Refer to Table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 6. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10), the macrocell provides eight additional configurations. When creating a PEEL device design, the desired macrocell configuration is generally specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type
The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register is set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear sets Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity
Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable
The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is switched into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select
The PEEL22LV10AZ macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell can be obtained from three different locations; from the I/O input pin, from the Q output of the flip-flop (registered feedback), or directly from the OR gate (combinatorial feedback).

Bi-directional I/O
The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with a bi-directional I/O, refer to Figure 4.

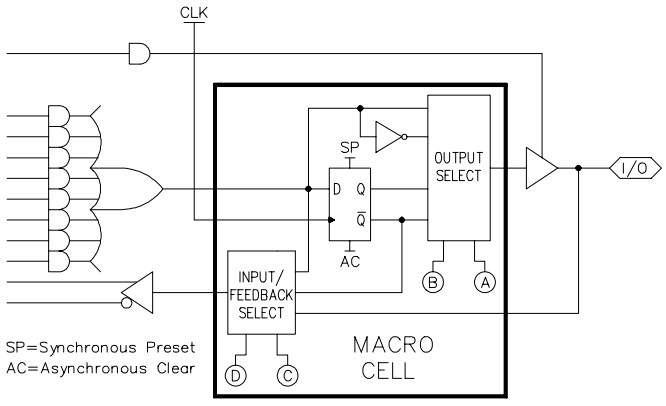


Figure 4 - Block Diagram of the PEEL22LV10AZ I/O Macrocell

Combinatorial Feedback
The signal-select multiplexer gives the macrocell the ability to feedback the output of the OR gate, bypassing the output buffer, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in Figure 6.)

Registered Feedback
Feedback also can be taken from the register, regardless of whether the output function is programmed to be combinatorial or registered. When implementing a combinatorial output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Programmable Clock Options (see Table 1)
A unique feature of the PEEL22LV10AZ is a programmable clock multiplexer that allows the user to select true or complement forms of either input pin or product-term clock sources.

Operates in both 3 Volt and 3.3 Volt Systems
The PEEL22LV10AZ is designed to operate with a V_{CC} range of 2.7 to 3.6 Volts D.C. This allows operation in both 3 Volt 10% (battery operated) and 3.3 Volt 10% (power supply operated) systems. The propagation delay t_{PD} is 5 ns slower at the lower voltage, but this is typically not an issue in battery-operated systems (see Table 6 - A.C. Electrical Characteristics).

Zero Power Feature
The CMOS PEEL22LV10AZ features "Zero-Power" standby operation for ultra-low power consumption. With the "Zero-Power" feature, transition-detection circuitry monitors the inputs, I/Os (including CLK) and feedbacks. If these signals do not change for a period of time greater than approximately two t_{PD}'s, the outputs are latched in their current state and the device automatically powers down. When the next signal transition is detected, the device will "wake up" for active operation until the signals stop switching long enough to trigger the next power-down. (Note that the t_{PD} is approximately 5 ns. slower on the first transition from sleep mode.)

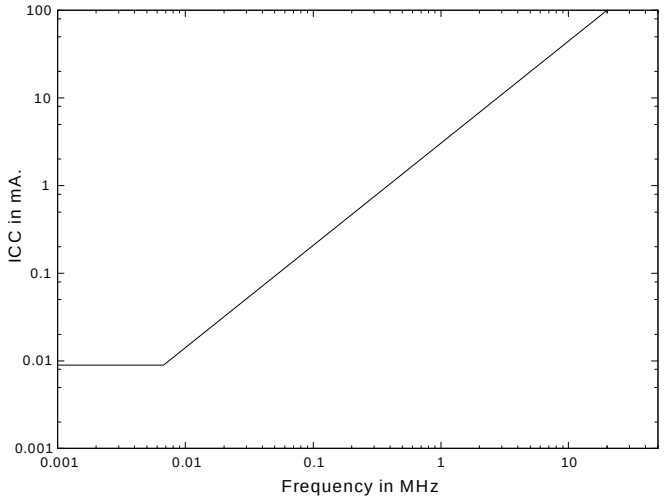


Figure 5 - Typical ICC vs. Input Clock Frequency for the 22LV10AZ

As a result of the "Zero-Power" feature, significant power savings can be realized for combinatorial or sequential operations when the inputs or clock change at a modest rate. See Figure 5.

When the PEEL22LV10AZ is powered up, a built-in feature holds the outputs in tri-state until V_{CC} reaches 2.2V. This prevents output transitions during power-up.

Schmitt Trigger Inputs
The PEEL22LV10AZ has Schmitt trigger input buffers on all inputs, including the clock. Schmitt trigger inputs allow direct input of slow signals such as biomedical and sine waves or clocks. They are also useful in cleaning up noisy signals. This makes the PEEL22LV10AZ especially desirable in portable applications where the environment is less predictable.

Design Security
The PEEL22LV10AZ provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word
The signature word feature allows a 64-bit code to be programmed into the PEEL22LV10AZ if the PEEL V10A+ software option (see Table 1) is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

Programming Support
ICT's JEDEC file translator allows easy conversion of existing 24 pin PLD designs to the PEEL22LV10AZ, without the need for redesign. ICT supports a broad range of popular third party design entry systems, including Data I/O Synario and Abel, Logical Devices CUPL and others. ICT also offers its proprietary WinPLACE software, an easy-to-use entry level PC-based software development system.

Programming support includes all the popular third party programmers; Data I/O, Logical Devices, and numerous others.

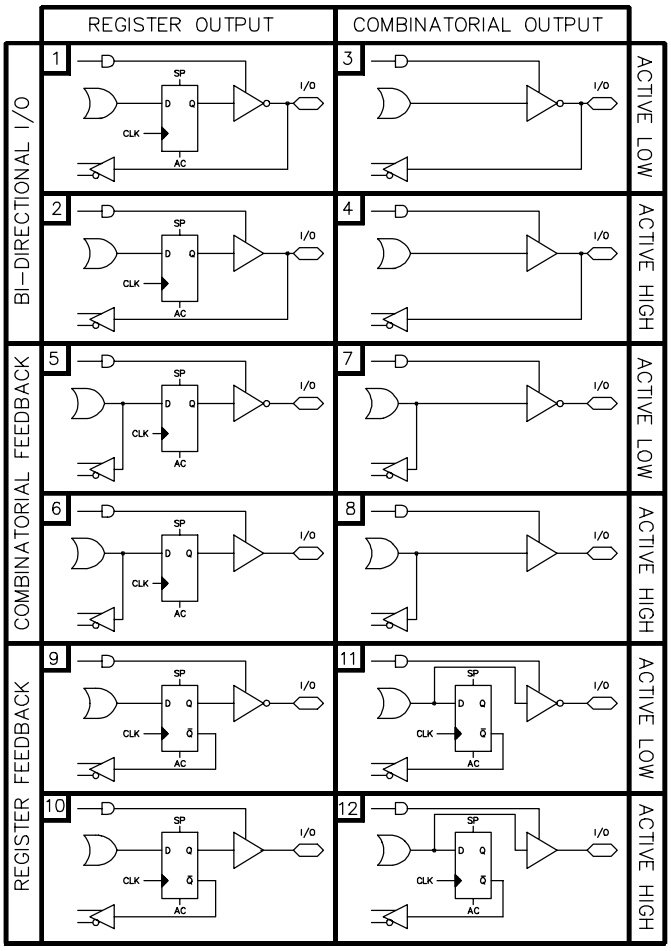


Figure 6 - Twelve Extended I/O Macrocell Configurations (see Table 1)

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	0	0	1	0	Bi-directional I/O	Register	Active Low
2	1	0	1	0			Active High
3	0	1	0	0		Combinatorial	Active Low
4	1	1	0	0			Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1			Active High
7	0	1	1	1		Combinatorial	Active Low
8	1	1	1	1			Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0			Active High
11	0	1	1	0		Combinatorial	Active Low
12	1	1	1	0			Active High

Table 2 – Extended Macrocell Configuration Bits (see Table 1)

This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Table 3 - Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to Ground	-0.5 to + 6.0	V
V_I, V_O	Voltage Applied to Any Pin[2]	Relative to Ground[1]	-0.5 to 5.5	V
I_O	Output Current	Per Pin (I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		-65 to +150	°C
T_{LT}	Lead Temperature	Soldering 10 Seconds	+300	°C

Table 4 - Operating Range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage[3]	Commercial/Industrial	2.7	3.6	V
T_A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	
T_{RVCC}	V_{CC} Rise Time	See Note 4.		250	ms

Table 5 - D.C. Electrical Characteristics Over the operating range (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage - TTL	V_{CC} = Min, I_{OH} = -2.0 mA	V_{CC} - 0.5		V
V_{OHC}	Output HIGH Voltage - CMOS	V_{CC} = Min, I_{OH} = -10 µA	V_{CC} - 0.3		V
V_{OL}	Output LOW Voltage - TTL	V_{CC} = Min, I_{OL} = 8.0 mA		0.4	V
V_{OLC}	Output LOW Voltage - CMOS	V_{CC} = Min, I_{OL} = 10 µA		0.15	V
V_{IH}	Input HIGH Voltage	V_{CC} = 3.3 V	2.0	5.5	V
V_{IL}	Input LOW Voltage	V_{CC} = 3.3 V	-0.3	0.8	V
V_H	Input Voltage Hysteresis		0.2		V
I_{IN}	Input Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ VCC, I/O = High Z		+/- 1	µA
		V_{CC} = Min, GND ≤ V_{IN} ≤ 5.5V, I/O = High Z		25	µA
	I/O Leakage Current	V_{CC} = Max, GND ≤ V_{IN} ≤ VCC, I/O = High Z		+/- 1	µA
		V_{CC} = Min, GND ≤ V_{IN} ≤ 5.5V, I/O = High Z		500	µA
I_{CCS}	VCC Current, Standby	V_{IN} = 0V or V_{CC}, All Outputs disabled[5]	5 (typ)	25	µA
I_{CC}[11]	VCC Current, f=1MHz	V_{IN} = 0V or V_{CC}, All Outputs disabled[5]	1.5 (typ)	3	mA
C_{IN}[8]	Input Capacitance	T_A = 25°C, V_{CC} = Max @ f = 1 MHz		6	pF
C_{OUT}[8]	Output Capacitance			12	pF

Table 6 - A.C. Electrical Characteristics
(Over the operating range[9])

Symbol	Parameter	-25				I-35				Units
		3V±10%		3.3V±10%		3V±10%		3.3V±10%		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input[6] to non-registered output in continuous mode[13]		30		25		40		35	ns
t_{OE}	Input[6] to output enable[7]		30		25		40		35	ns
t_{OD}	Input[6] to output disable[7]		30		25		40		35	ns
t_{CO1}	Clock to output		20		15		28		25	ns
t_{CO2}	Clock to comb. Output delay via internal registered feedback		40		35		56		49	ns
t_{CF}	Clock to Feedback		14		9		20		13	ns
t_{SC}	Input[6] or feedback setup to clock	20		15		28		21		ns
t_{HC}	Input[6] hold after clock	0		0		0		0		ns
t_{CL}, t_{CH}	Clock low time, clock high time[9]	20		13		28		18		ns
t_{CP}	Min clock period Ext (t_{SC} + t_{CO1})	40		30		56		39		ns
f_{MAX1}	Internal feedback 1/ (t_{SC} + t_{CF})[12]	29.4		41.6		20.8		29.4		MHz
f_{MAX2}	External Feedback (1/ t_{CP})[12]	25		33.3		17.9		25.6		MHz
f_{MAX3}	No Feedback 1/ (t_{CL} + t_{CH})[12]	25		38.4		17.9		27.7		MHz
t_{AW}	Asynchronous Reset Pulse Width	30		25		40		35		ns
t_{AP}	Input to Asynchronous Reset		30		25		40		35	ns
t_{AR}	Asynchronous Reset recovery time		30		25		40		35	ns
t_{RESET}	Power-on reset time for registers in clear state[14]		5		5		5		5	µs

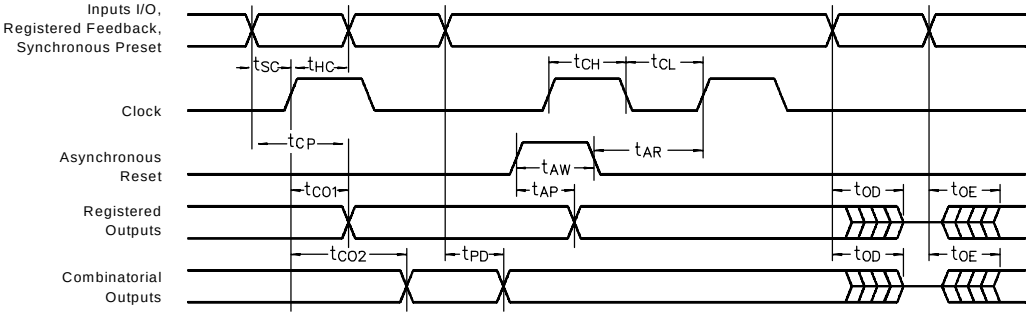


Figure 7 - Switching Waveforms

Notes:

1. Minimum DC input is -0.5V, however, inputs may undershoot to -2.0V for periods less than 20 ns.
2. V_I and V_O are not specified for program/verify operation.
3. The Supply Voltage range of 2.7 to 3.6V was chosen to allow this part to be used in both 3V 10% and 3.3V 10% applications.
4. Test Points for Clock and V_{CC} in t_R and t_F are referenced at the 10% and 90% levels.
5. I/O pins are 0V and V_{CC}.
6. "Input" refers to an input pin signal.
7. t_{OE} is measured from input transition to V_{REF} 0.1V, TOD is measured from input transition to V_{OH} -0.1V or V_{OL} +0.1V; V_{REF} =V_L
8. Capacitances are tested on a sample basis.
9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (Unless otherwise specified).
10. Test one output at a time for duration of less than 1 second.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design process modification that might affect operational frequency.
13. t_{PD}, t_{OE}, t_{OD}, t_{CO}, t_{SC}, and t_{AP} are approximately 5 ns, slower on the first transaction from sleep mode.
14. All inputs at GND.

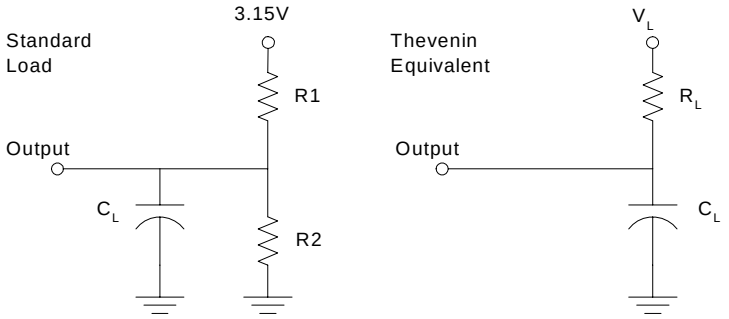


Figure 8 - PEEL™ Device and Array Test Loads

Technology	R1	R2	RL	VL	CL
CMOS	274kΩ	257kΩ	110kΩ	1.30V	33 pF
TTL	315Ω	548Ω	200Ω	2.00V	33 pF

Table 7 - Ordering Information

Part Number	Speed	Temperature	Package
PEEL22LV10AZP-25	25ns	Commercial	24-pin Plastic DIP
PEEL22LV10AZPI-35	35ns	Industrial	24-pin Plastic DIP
PEEL22LV10AZJ-25	25ns	Commercial	28-pin PLCC
PEEL22LV10AZJI-35	35ns	Industrial	28-pin PLCC
PEEL22LV10AZS-25	25ns	Commercial	24-pin SOIC
PEEL22LV10AZSI-35	35ns	Industrial	24-pin SOIC
PEEL22LV10AZT-25	25ns	Commercial	24-pin TSSOP
PEEL22LV10AZTI-35	35ns	Industrial	24-pin TSSOP

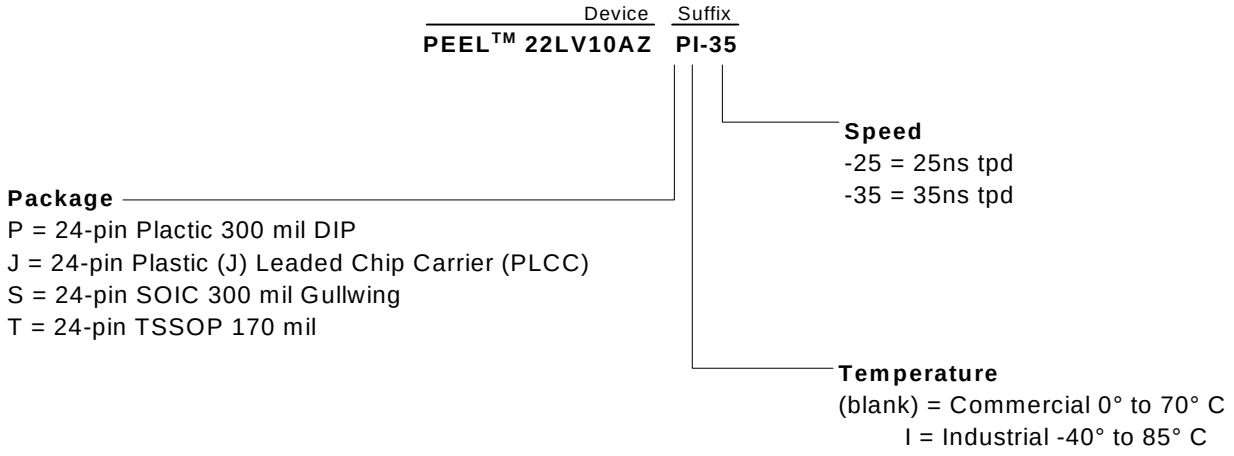


Figure 9 - Part Number

Corporate Office

2123 Ringwood Avenue
San Jose, CA 95131
TEL (408) 434-0678
FAX (408) 432-0815

Email:
sales&marketing@ictpld.com

Website:
http://www.ictpld.com