



Integrated Device Technology, Inc.

# FAST CMOS 1-OF-8 DECODER WITH ENABLE

IDT54/74FCT138T/AT/CT

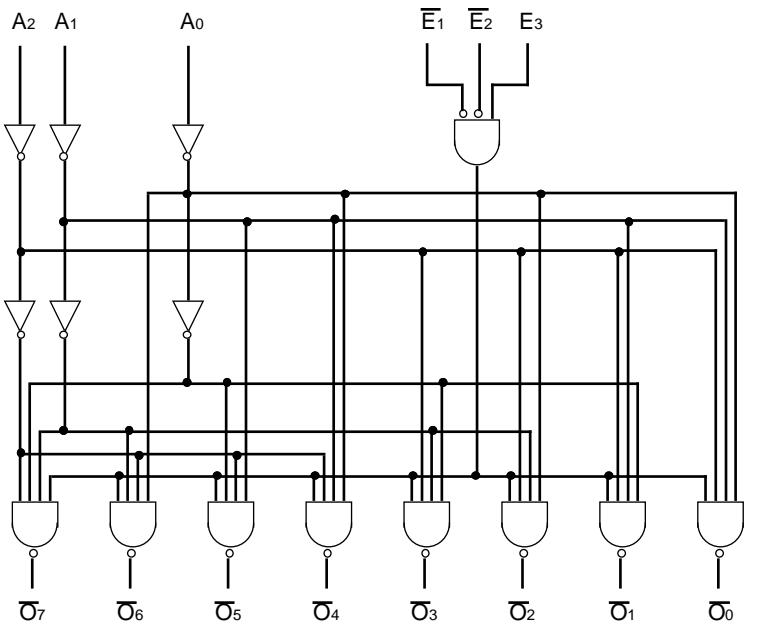
## FEATURES:

- Std., A and C speed grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH} = 3.3\text{V}$  (typ.)
  - $V_{OL} = 0.3\text{V}$  (typ.)
- High drive outputs (-15mA  $I_{OH}$ , 48mA  $I_{OL}$ )
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

## DESCRIPTION:

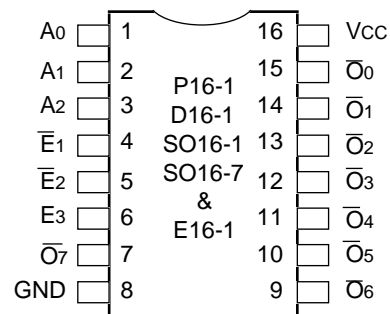
The IDT54/74FCT138T/AT/CT are 1-of-8 decoders built using an advanced dual metal CMOS technology. The IDT54/74FCT138T/AT/CT accepts three binary weighted inputs ( $A_0$ ,  $A_1$ ,  $A_2$ ) and, when enabled, provides eight mutually exclusive active LOW outputs ( $\bar{O}_0$ – $\bar{O}_7$ ). The IDT54/74FCT138T/AT/CT features three enable inputs, two active LOW ( $\bar{E}_1$ ,  $\bar{E}_2$ ) and one active HIGH ( $E_3$ ). All outputs will be HIGH unless  $\bar{E}_1$  and  $\bar{E}_2$  are LOW and  $E_3$  is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138T/AT/CT devices and one inverter.

## FUNCTIONAL BLOCK DIAGRAM



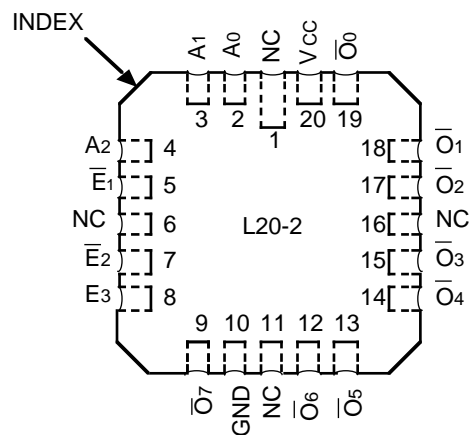
2570 drw 01

## PIN CONFIGURATIONS



2570 drw 02

DIP/SOIC/QSOP/CERPACK  
TOP VIEW



2570 drw 03

LCC  
TOP VIEW

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**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**APRIL 1995**

## PIN DESCRIPTION

Pin Names	Description
A0–A2	Address Inputs
$\bar{E}_1, \bar{E}_2$	Enable Inputs (Active LOW)
E3	Enable Input (Active HIGH)
$\bar{O}_0\text{--}\bar{O}_7$	Outputs (Active LOW)

2570 tbl 01

## FUNCTION TABLE

Inputs						Outputs							
$\bar{E}_1$	$\bar{E}_2$	E3	A0	A1	A2	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

2570 tbl 02

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	–0.5 to V <sub>CC</sub> +0.5	–0.5 to V <sub>CC</sub> +0.5	V
T <sub>A</sub>	Operating Temperature	0 to +70	–55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	–55 to +125	–65 to +135	°C
T <sub>STG</sub>	Storage Temperature	–55 to +125	–65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	–60 to +120	–60 to +120	mA

2570 lmk 03

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Input and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

2570 lmk 04

### NOTE:

- This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$		-60	-120	-225	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 32\text{mA MIL.}$ $I_{OL} = 48\text{mA COM'L.}$	—	0.3	0.5	V
$V_H$	Input Hysteresis	—		—	200	—	mV
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	0.01	1	mA

**NOTES:**

2570 tbl 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .

### POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.3	mA/ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open Toggle $\bar{E}_1$ , $\bar{E}_2$ or $E_3$ 50% Duty Cycle $f_o = 10\text{MHz}$ One Input and One Output Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.8	5.0	

**NOTES:**

2570 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_o$  = Output Frequency  
 $N_o$  = Number of Outputs at  $f_o$   
 All currents are in milliamps and all frequencies are in megahertz.

### SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT138T				FCT138AT				FCT138CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to $\bar{O}_n$	$CL = 50\text{pF}$ $RL = 500\Omega$	1.5	9.0	1.5	12.0	1.5	5.8	1.5	7.8	1.5	5.1	1.5	6.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}_1$ or $\bar{E}_2$ to $\bar{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_3$ to $\bar{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	

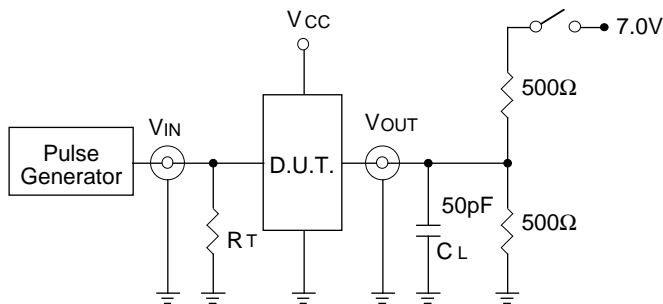
**NOTES:**

2570 tbl 07

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



2570 drw 04

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

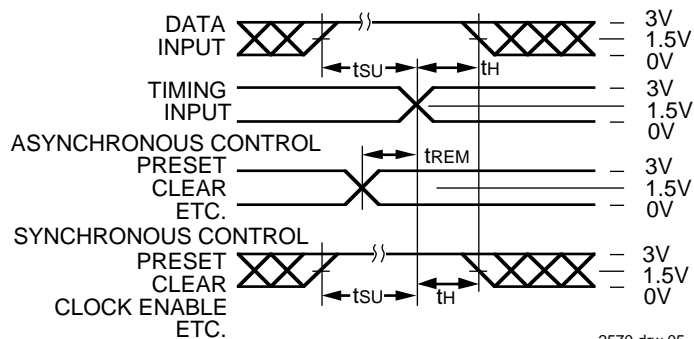
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#### DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.

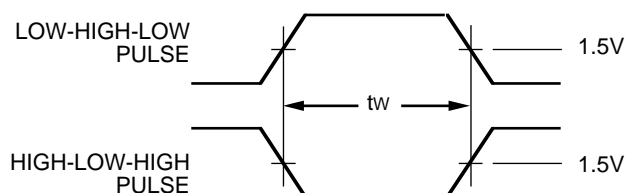
RT= Termination resistance: should be equal to ZOUT of the Pulse Generator.

### SET-UP, HOLD AND RELEASE TIMES



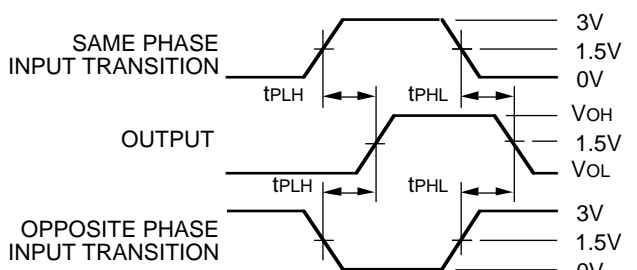
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### PULSE WIDTH



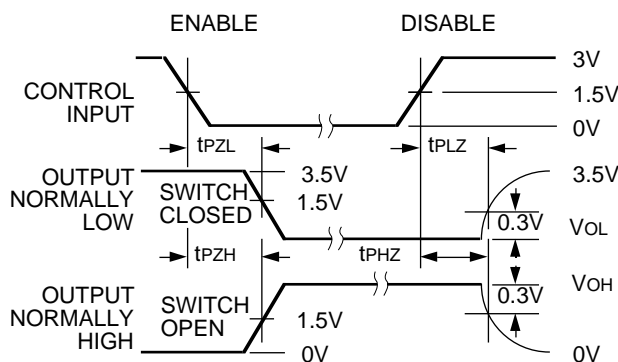
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### PROPAGATION DELAY



2570 drw 07

### ENABLE AND DISABLE TIMES

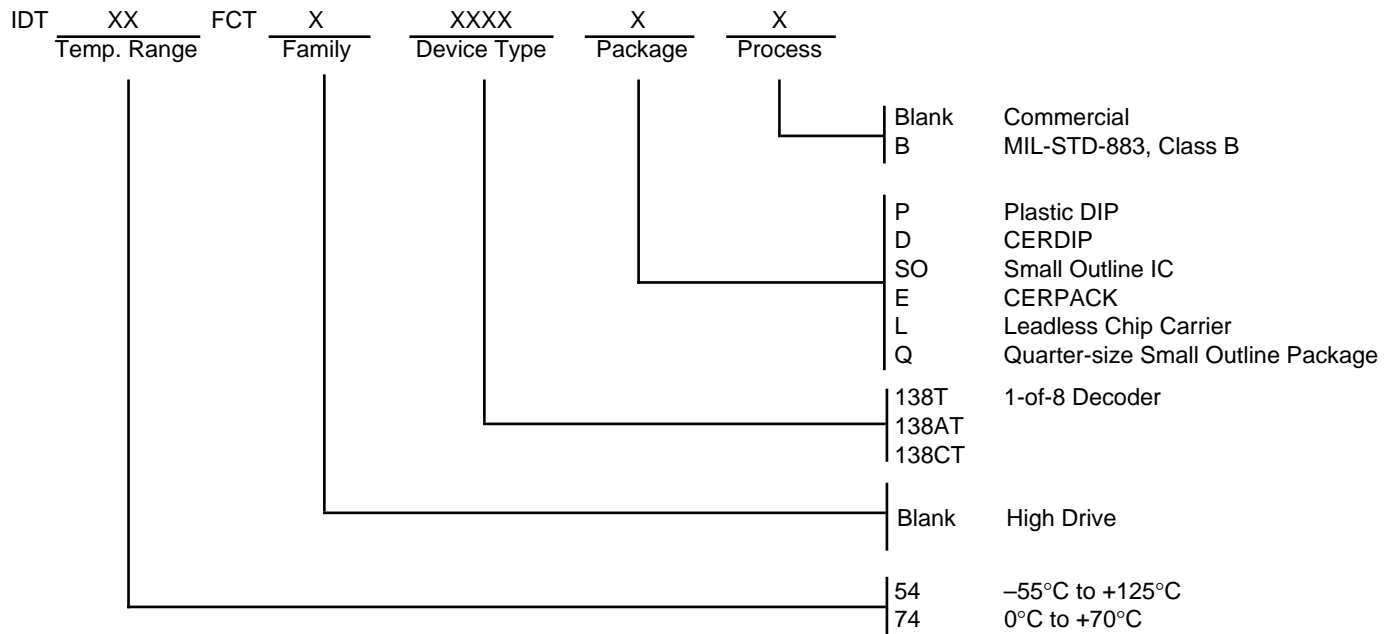


2570 drw 08

#### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $t_f \leq$  2.5ns;  $t_r \leq$  2.5ns

**ORDERING INFORMATION**



2570 drw 09