Integrated Device Technology, Inc.

CMOS SyncFIFO™ 256 x 18, 512 x 18, 1024 x 18, 2048 x 18 and 4096 x 18

IDT72205LB
IDT72215LB
IDT72225LB
IDT72235LB
IDT72245LB

FEATURES:

- 256 x 18-bit organization array (72205LB)
- 512 x 18-bit organization array (72215LB)
- 1024 x 18-bit organization array (72225LB)
- 2048 x 18-bit organization array (72235LB)
- 4096 x 18-bit organization array (72245LB)
- 15 ns read/write cycle time
- Easily expandable in depth and width
- Read and write clocks can be asynchronous or coincident
- Dual-Port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high-impedance state
- High-performance submicron CMOS technology
- Available in a 64-lead thin quad flatpack (TQFP/STQFP), pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40^{O}C to +85^{O}C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT72205LB/72215LB/72225LB/72235LB/72245LB are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, Local Area Networks (LANs), and interprocessor communication.

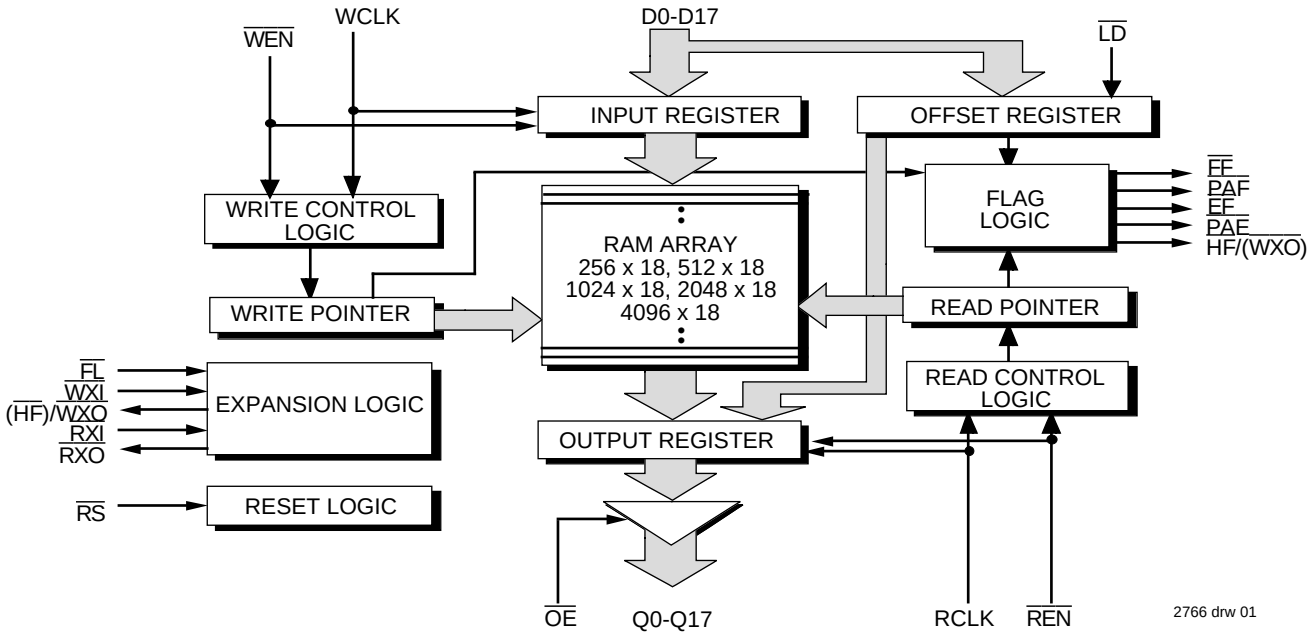
Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a data input enable pin ($\overline{WEN}$). Data is read into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An Output Enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the Load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available when the FIFO is used in a single device configuration.

The IDT72205LB/72215LB/72225LB/72235LB/72245LB are depth expandable using a daisy-chain technique. The XI and $\overline{XO}$ pins are used to expand the FIFOs. In depth expansion configuration, FL is grounded on the first device and set to HIGH for all other devices in the daisy chain.

The IDT72205LB/72215LB/72225LB/72235LB/72245LB is fabricated using IDT's high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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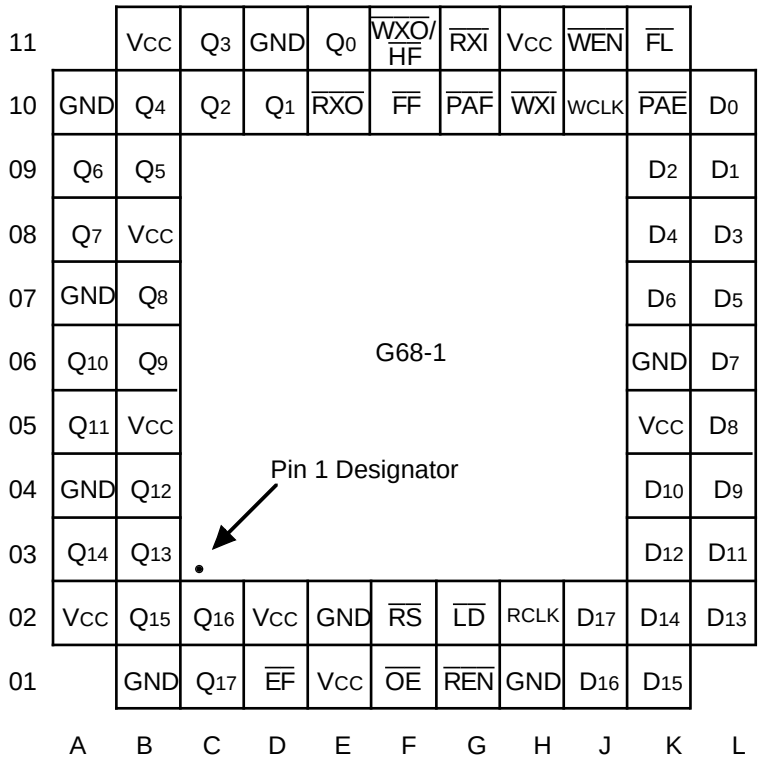
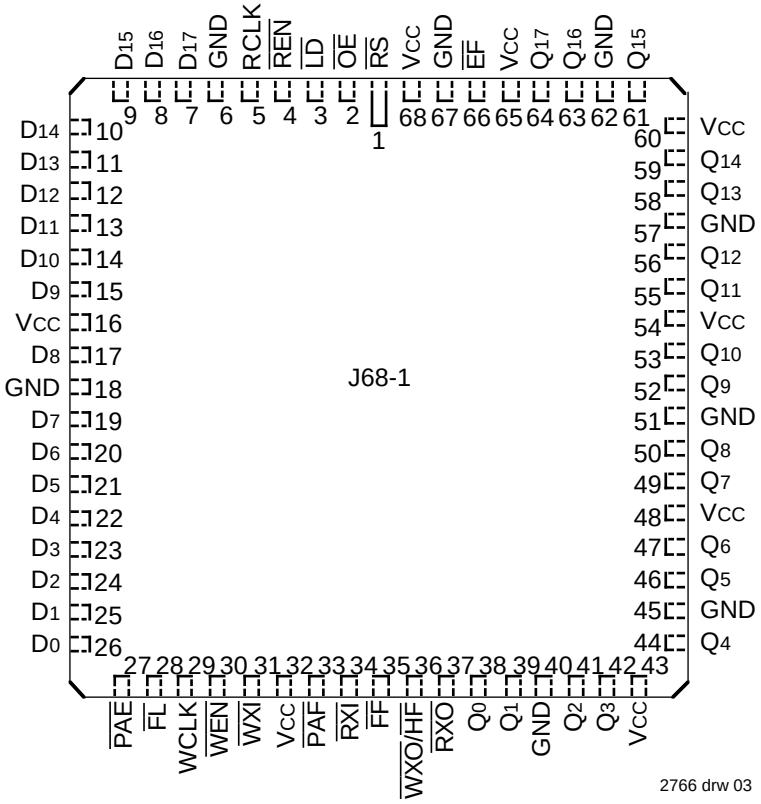
PIN CONFIGURATIONS

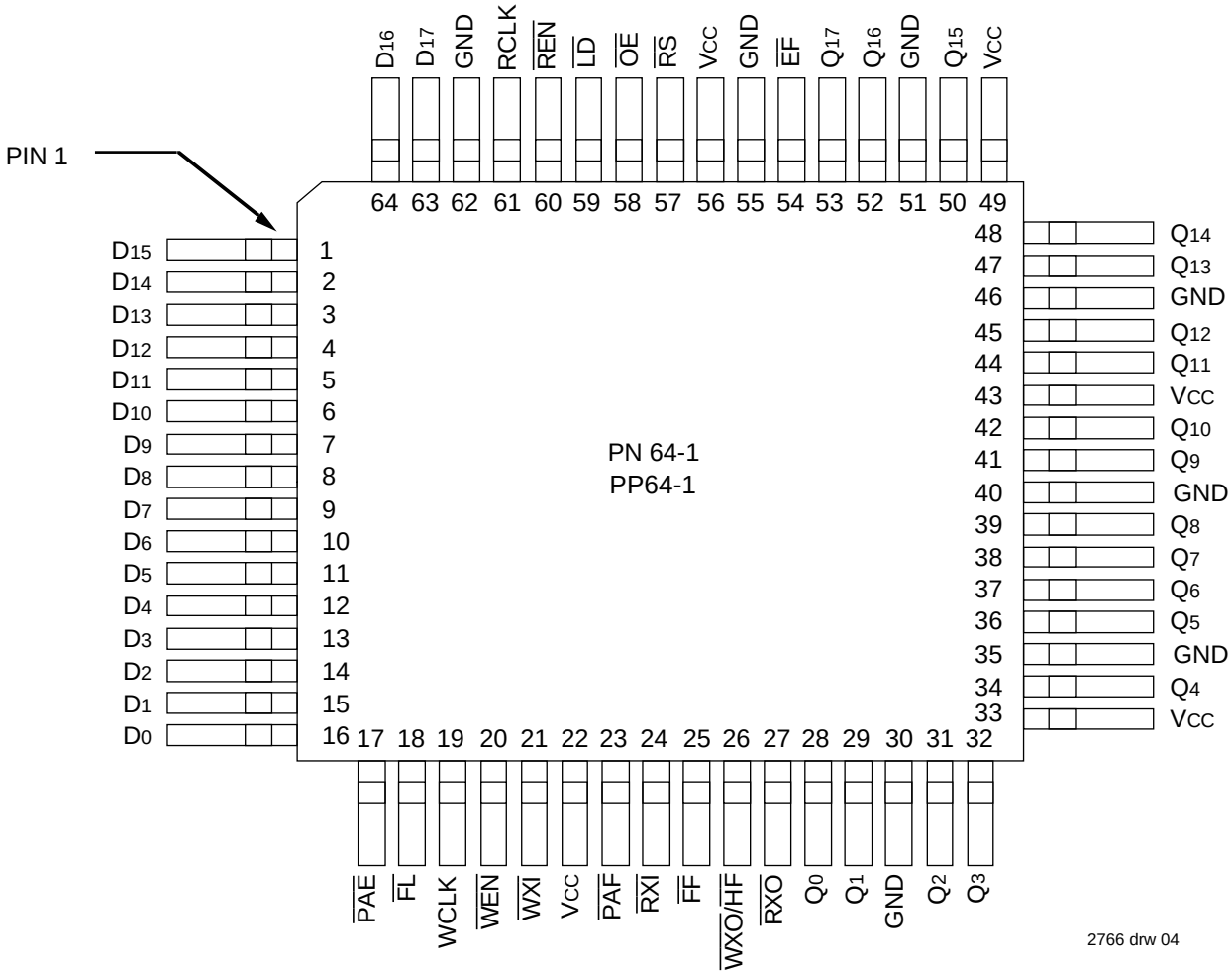


PGA
TOP VIEW



PLCC
TOP VIEW

PIN CONFIGURATIONS



TQFP/STQFP
TOP VIEW

NOTE:
1. For information on the flatpack (F68-1), contact factory.

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0–D17	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on a LOW-to-HIGH transition of WCLK, if the FIFO is not full.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	When $\overline{REN}$ is LOW, data is read from the FIFO on a LOW-to-HIGH transition of RCLK, if the FIFO is not empty.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D0–D11 is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q0–Q11 is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FL}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to HIGH for all other devices in the daisy chain.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, RXI is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 31 from empty for 72205LB, 63 from empty for 72215LB, and 127 from empty for 72225LB/72235LB/72245LB.
$\overline{PAF}$	Programmable	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 31 from full for 72205LB, 63 from full for 72215LB, and 127 from full for 72225LB/72235LB/72245LB.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q0–Q17	Data Outputs	O	Data outputs for a 18-bit bus.
VCC	Power		Eight +5V power supply pins for the PLCC and PGA, five pins for the TQFP.
GND	Ground		Eight ground pins for the PLCC and PGA, seven pins for the TQFP.

2766 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	MIlitary	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

2766 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

2766 tbl 03

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72205LB IDT72215LB IDT72225LB Commercial t_{CLK} = 15, 20, 25, 35, 50ns			IDT72205LB IDT72215LB IDT72225LB Military t_{CLK} = 25, 35, 50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic “1” Voltage, IOH = –2 mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic “0” Voltage, IOL = 8 mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	200	—	—	250	mA
ICC2(3)	Average Standby Current (All Input = VCC – 0.2V, except RCLK and WCLK which are free-running)	—	—	70	—	—	85	mA

Symbol	Parameter	IDT72235LB IDT72245LB Commercial t_{CLK} = 15, 20, 25, 35, 50ns			IDT72235LB IDT72245LB Military t_{CLK} = 25, 35, 50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic “1” Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic “0” Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(4)	Active Power Supply Current	—	—	200	—	—	250	mA
I_{CC2}(4)	Average Standby Current (All Input = VCC – 0.2V, except RCLK and WCLK which are free-running)	—	—	70	—	—	85	mA

2766 tbl 04

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3 & 4. Tested at f = 20MHz with outputs unloaded.
(3) Typical I_{CC1} = 60 + (f_{CLK}*0.57/MHz) + (f_{CLK}*C_L*0.02/MHz-pF) mA
(4) Typical I_{CC1} = 80 + (f_{CLK} + 0.73/MHz) + (f_{CLK}*C_L*0.02/MHz-pF) mA
f_{CLK} = 1/t_{CLK}, C_L = external capacitive load (30 pF typical)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	VIN = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	VOUT = 0V	10	pF

NOTES: 2766 tbl 05
1. With output deselected, ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commercial				Commercial and Military						
		72205LB15 72215LB15 72225LB15 72235LB15 72245LB15		72205LB20 72215LB20 72225LB20 72235LB20 72245LB20		72205LB25 72215LB25 72225LB25 72235LB25 72245LB25		72205LB35 72215LB35 72225LB35 72235LB35 72245LB35		72205LB50 72215LB50 72225LB50 72235LB50 72245LB50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	10	2	12	3	15	3	20	3	25	ns
tCLK	Clock Cycle Time	15	—	20	—	25	—	35	—	50	—	ns
tCLKH	Clock HIGH Time	6.5	—	8	—	10	—	14	—	20	—	ns
tCLKL	Clock LOW Time	6.5	—	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	7	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	7	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[1]	15	—	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	10	—	12	—	15	—	20	—	30	—	ns
tRSR	Reset Recovery Time	10	—	12	—	15	—	20	—	30	—	ns
tRSF	Reset to Flag and Output Time	—	35	—	35	—	40	—	45	—	50	ns
tOLZ	Output Enable to Output in Low-Z[2]	0	—	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	12	—	15	—	20	ns
tOHZ	Output Enable to Output in High-Z[2]	1	8	1	9	1	12	1	15	1	20	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
tPAF	Clock to Programmable Almost-Full Flag	—	28	—	30	—	35	—	40	—	40	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	28	—	30	—	35	—	40	—	40	ns
tHF	Clock to Half-Full Flag	—	28	—	30	—	35	—	40	—	40	ns
tXO	Clock to Expansion Out	—	10	—	12	—	15	—	20	—	30	ns
tXI	Expansion In Pulse Width	6.5	—	8	—	10	—	14	—	20	—	ns
tXIS	Expansion In Set-Up Time	5	—	8	—	10	—	15	—	20	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	10	—	14	—	16	—	18	—	20	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	10	—	14	—	16	—	18	—	20	—	ns

NOTES: 2766 tbl 06
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2766 tbl 07

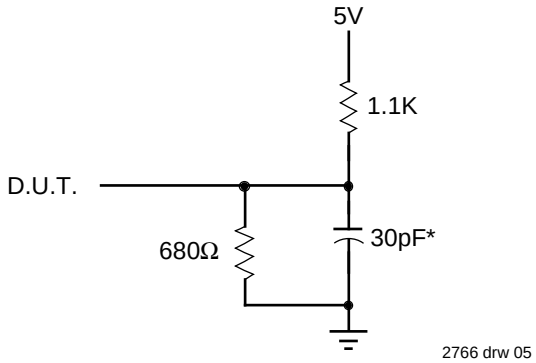


Figure 1. Output Load
* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{17})

Data inputs for 18-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$), Half-Full Flag ($\overline{HF}$), and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to LOW after tRSF. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

WRITE CLOCK (WCLK)

A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)

When Write Enable ($\overline{WEN}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When $\overline{WEN}$ is HIGH, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the $\overline{FF}$ will go HIGH after t_{WFF} allowing a write to begin. $\overline{WEN}$ is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK), when Output Enable ($\overline{OE}$) is set LOW.

The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)

When Read Enable ($\overline{REN}$) is LOW, data is loaded from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When $\overline{REN}$ is HIGH, the output register holds the previous data and no new data is loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a write is performed, the $\overline{EF}$ will go HIGH after t_{REF} and a read can begin. $\overline{REN}$ is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (HIGH), the Q output data bus is in a high-impedance state.

LOAD ($\overline{LD}$)

The IDT72205LB/72215LB/72225LB/72235LB/72245LB devices contain two 12-bit offset registers with data on the inputs, or read on the outputs. When the Load ($\overline{LD}$) pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D0-D11 is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the $\overline{LD}$ pin and

LD	WEN	WCLK(1)	Selection
0	0		Writing to offset registers: Empty Offset Full Offset
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

NOTE: 2766 tbl 08
1. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register

($\overline{WEN}$) are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the $\overline{LD}$ pin HIGH, the FIFO is returned to normal read/write operation. When the LD pin is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

When the $\overline{LD}$ pin is LOW and $\overline{WEN}$ is HIGH, the WCLK input is disabled; then a signal at this input can neither increment the write offset register pointer, nor execute a write.

The contents of the offset registers can be read on the output lines when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK). The act of reading the control registers employs a dedicated read offset register pointer. (The read and write pointers operate independently).

A read and a write should not be performed simultaneously to the offset registers.First Load (FL)

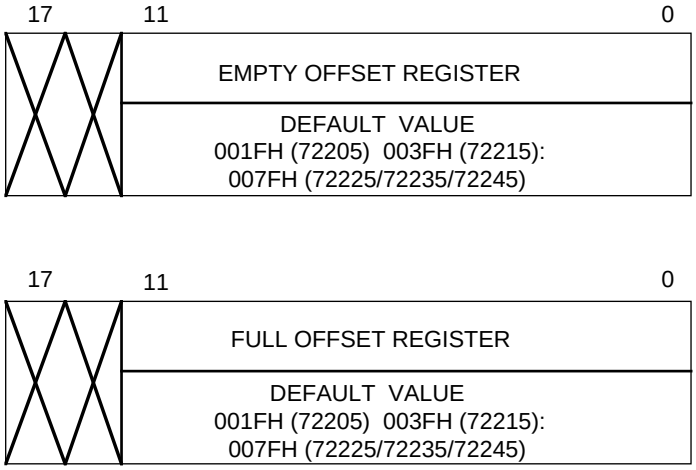
First Load ($\overline{FL}$) is grounded to indicate operation in the Single Device or Width Expansion mode. In the Depth Expansion configuration, $\overline{FL}$ is grounded to indicate it is the first device loaded and is set to HIGH for all other devices in the daisy chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT ($\overline{WXI}$)

This is a dual purpose pin. Write Expansion In ($\overline{WXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. $\overline{WXI}$ is connected to Write Expansion Out ($\overline{WXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

READ EXPANSION INPUT (RXI)

This is a dual purpose pin. Read Expansion In ($\overline{RXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. $\overline{RXI}$ is connected to Read Expansion Out ($\overline{RXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.



NOTE: 2766 drw 06
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

TABLE I — STATUS FLAGS

Number of Words in FIFO									
72205	72215	72225	72235	72245	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	0	0	H	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
(n + 1) to 128	(n + 1) to 256	(n + 1) to 512	(n + 1) to 1024	(n + 1) to 2048	H	H	H	H	H
129 to (256-(m+1))	257 to (512-(m+1))	513 to (1024-(m+1))	1025 to (2048-(m+1))	2049 to (4096-(m+1))	H	H	L	H	H
(256-m)[2] to 255	(512-m)[2] to 511	(1024-m)[2] to 1023	(2048-m)[2] to 2047	(4096-m)[2] to 4095	H	L	L	H	H
256	512	1024	2048	4096	L	L	L	H	H

NOTES: 2766 tbl 09
1. n = Empty Offset (Default Values : 72205 n=31, 72215 n = 63, 72225/72235/72245 n = 127)
2. m = Full Offset (Default Values : 72205 n=31, 72215 n = 63, 72225/72235/72245 n = 127)

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, indicating that the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 256 writes for the IDT72205LB, 512 writes for the IDT72215LB, 1024 writes for the IDT72225LB, 2048 writes for the IDT72235LB and 4096 writes for the IDT72245LB.

The Full Flag ($\overline{FF}$) is updated on the LOW-to-HIGH transition of the write clock (WCLK).

EMPTY FLAG (EF)

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The $\overline{EF}$ is updated on the LOW-to-HIGH transition the read clock (RCLK).

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the $\overline{PAF}$ will go LOW after (256-

m) writes for the IDT72205LB, (512-m) writes for the IDT72215LB, (1024-m) writes for the IDT72225LB, (2048–m) writes for the IDT72235LB and (4096–m) writes for the IDT72245LB. The offset "m" is defined in the FULL offset register.

If there is no Full offset specified, the $\overline{PAF}$ will be LOW when the device is 31 away from completely full for 72205LB, 63 away from completely full for 72215LB, and 127 away from completely full for 72225LB/72235LB/72245LB.

The $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of the write clock (WCLK). $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of the read clock (RCLK). Thus $\overline{PAF}$ is asychronous.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the EMPTY offset register.

If there is no Empty offset specified, the Programmable Almost Empty Flag ($\overline{PAE}$) will be LOW when the device is 31 away from completely empty for 72205LB, 63 away from completely empty for 72215LB, and 127 away from completely empty for 72225LB/72235LB/72245LB.

The $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of the read clock (RCLK). $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of the write clock (WCLK). Thus $\overline{PAF}$ is asychronous.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when Write Expansion In ($\overline{WXI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the LOW-to-HIGH transition of the next write cycle, the Half-Full Flag goes LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to HIGH by the LOW-to-HIGH transition of the read clock (RCLK). The $\overline{HF}$ is asychronous.

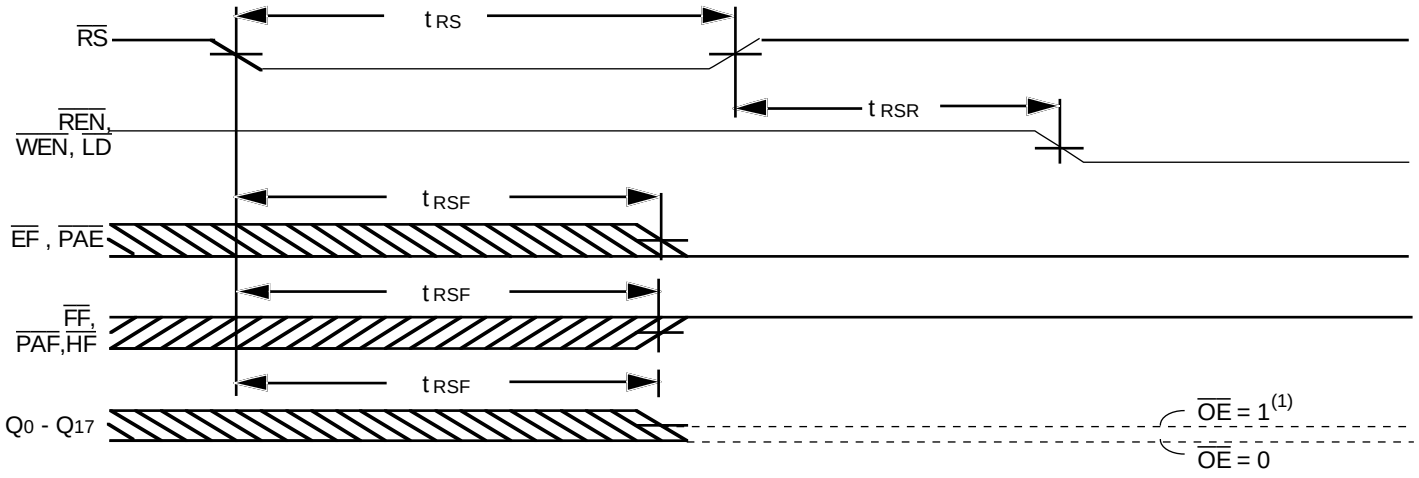
In the Depth Expansion or Daisy Chain mode, $\overline{WXI}$ is connected to $\overline{WXO}$ of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device writes to the last location of memory.

READ EXPANSION OUT ($\overline{RXO}$)

In the Depth Expansion or Daisy Chain configuration, Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

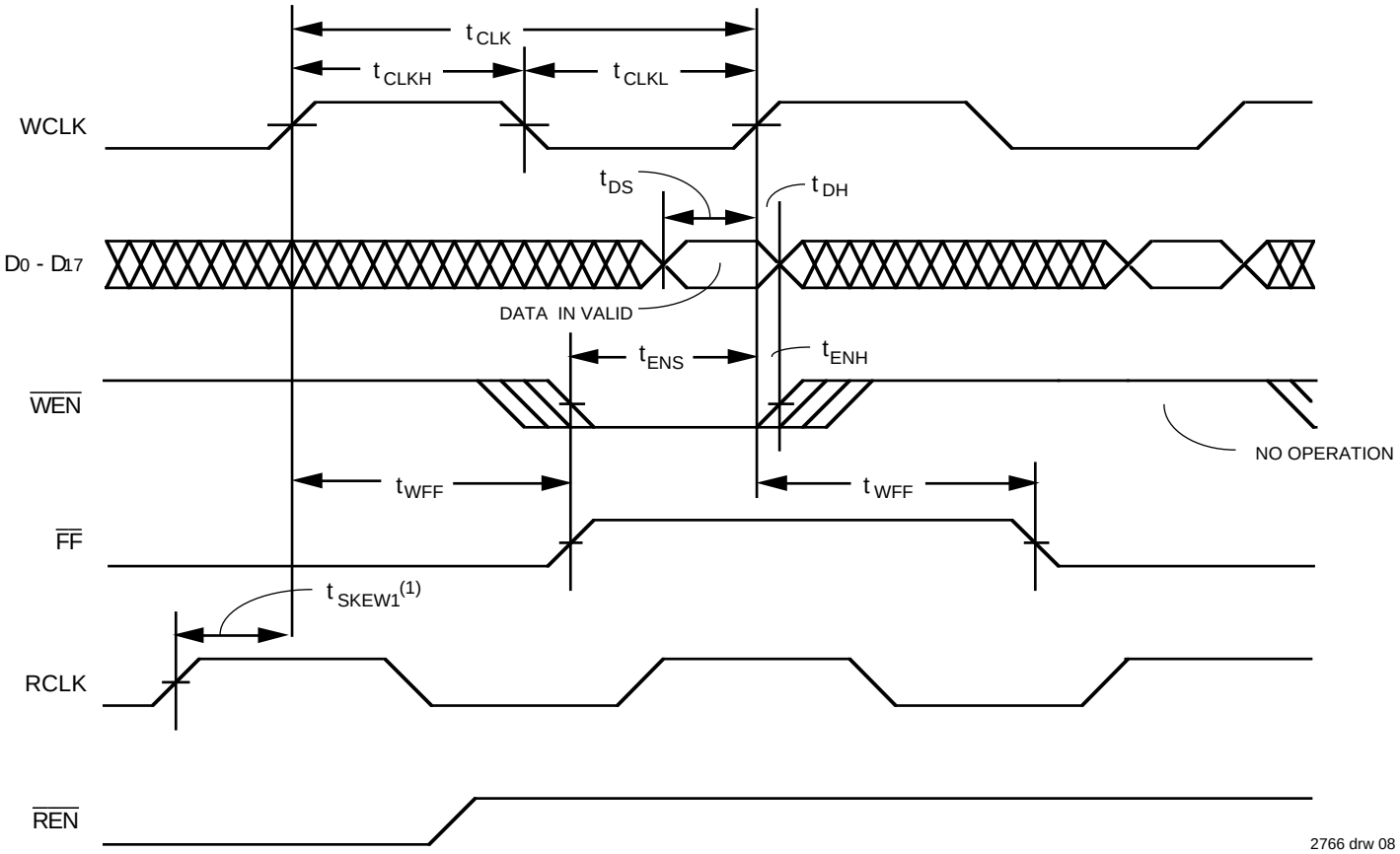
DATA OUTPUTS (Q0-Q17)

Q0-Q17 are data outputs for 18-bit wide data.



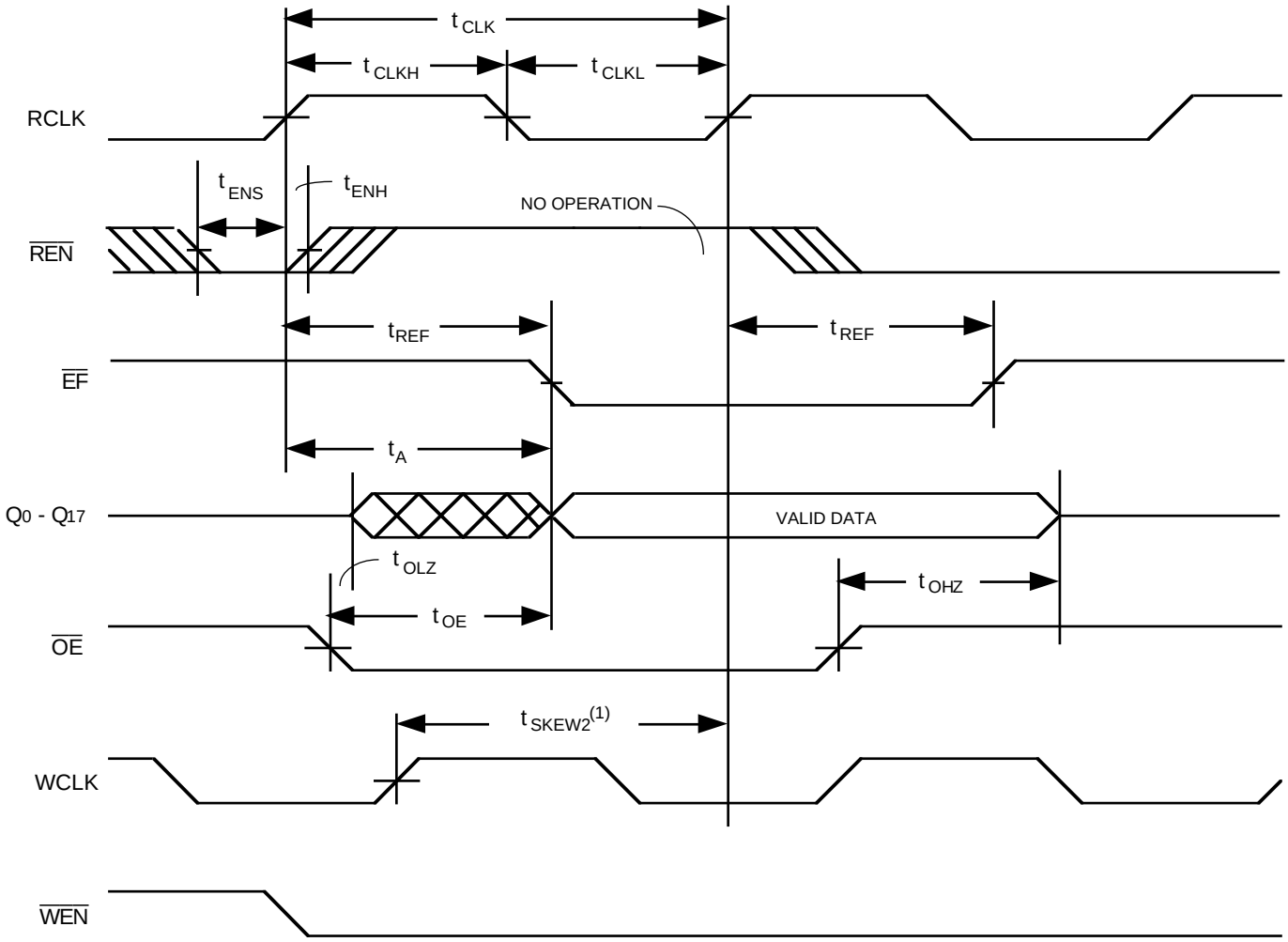
NOTES:
1. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 5. Reset Timing(2)



NOTE:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 6. Write Cycle Timing



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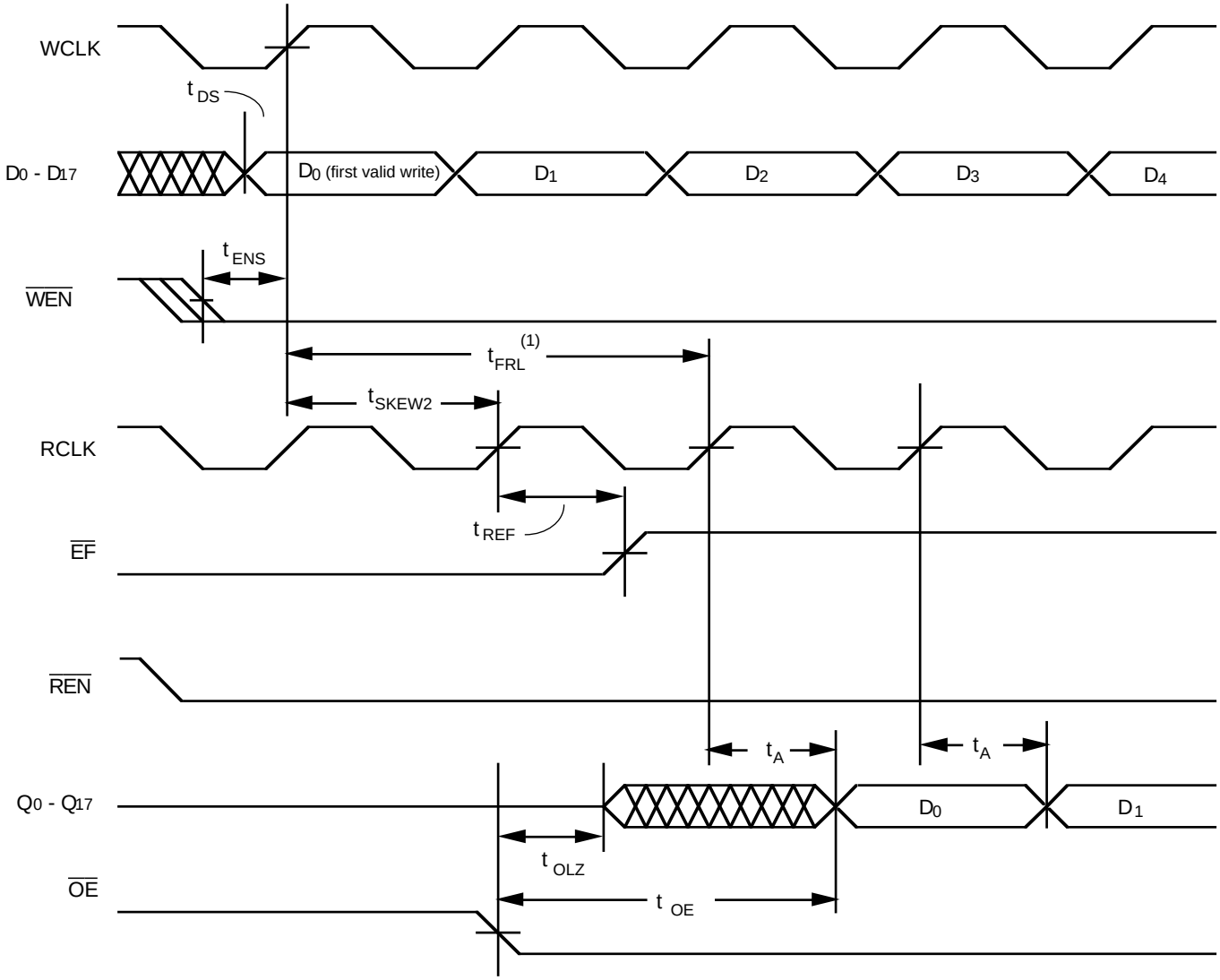
NOTE:
1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 7. Read Cycle Timing



NOTES:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
2. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

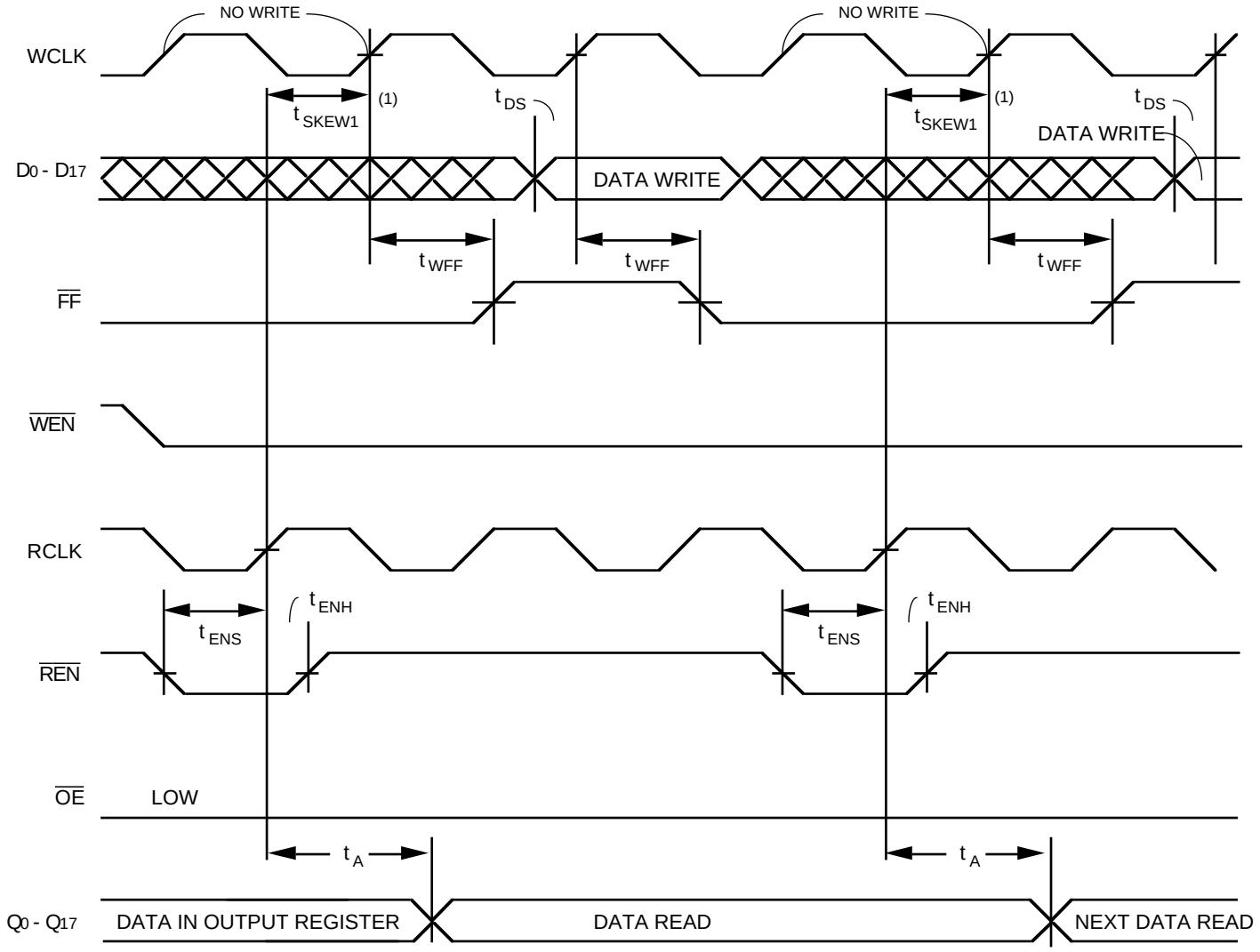


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Figure 9. Full Flag Timing

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

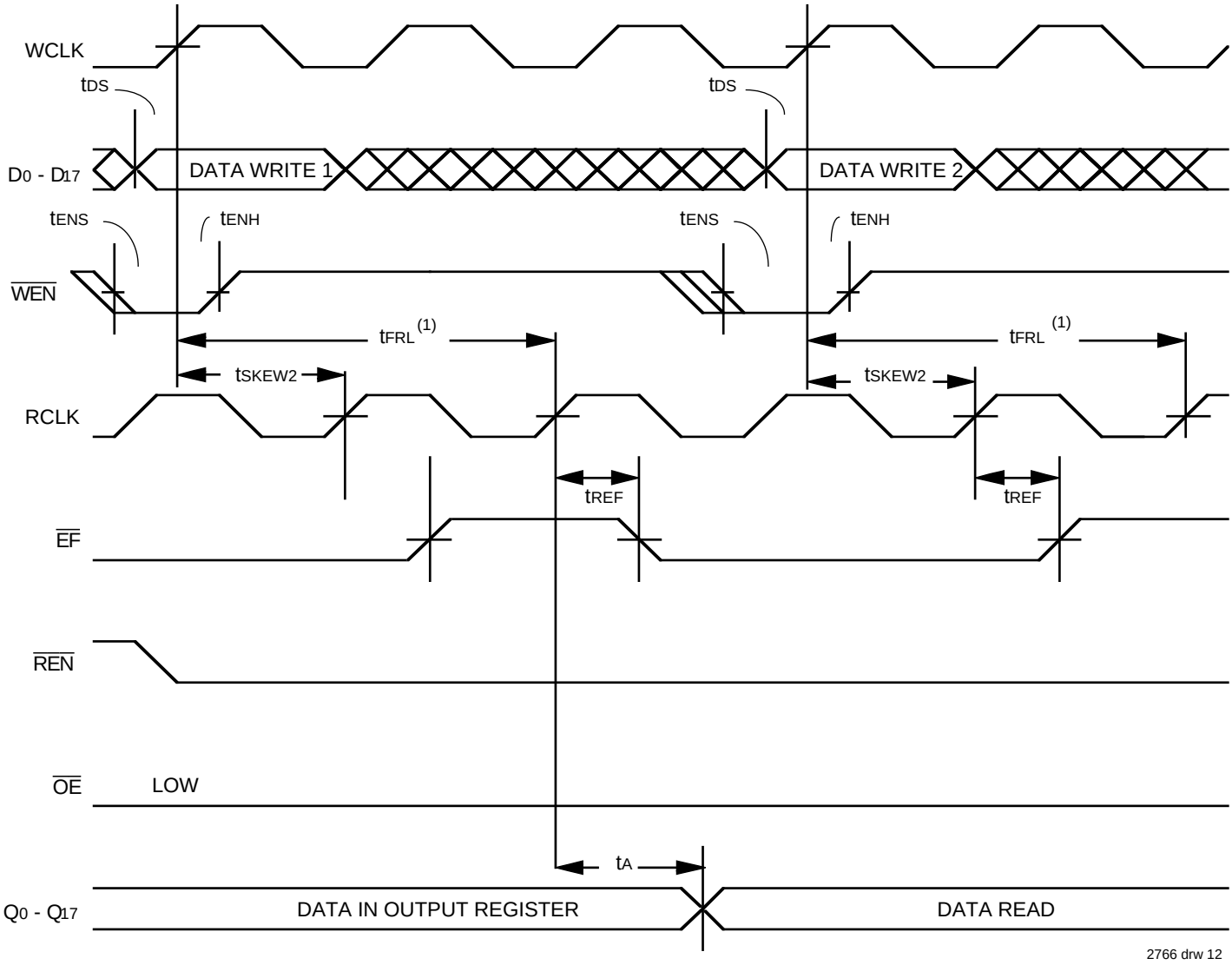


Figure 10. Empty Flag Timing

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2}. or t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

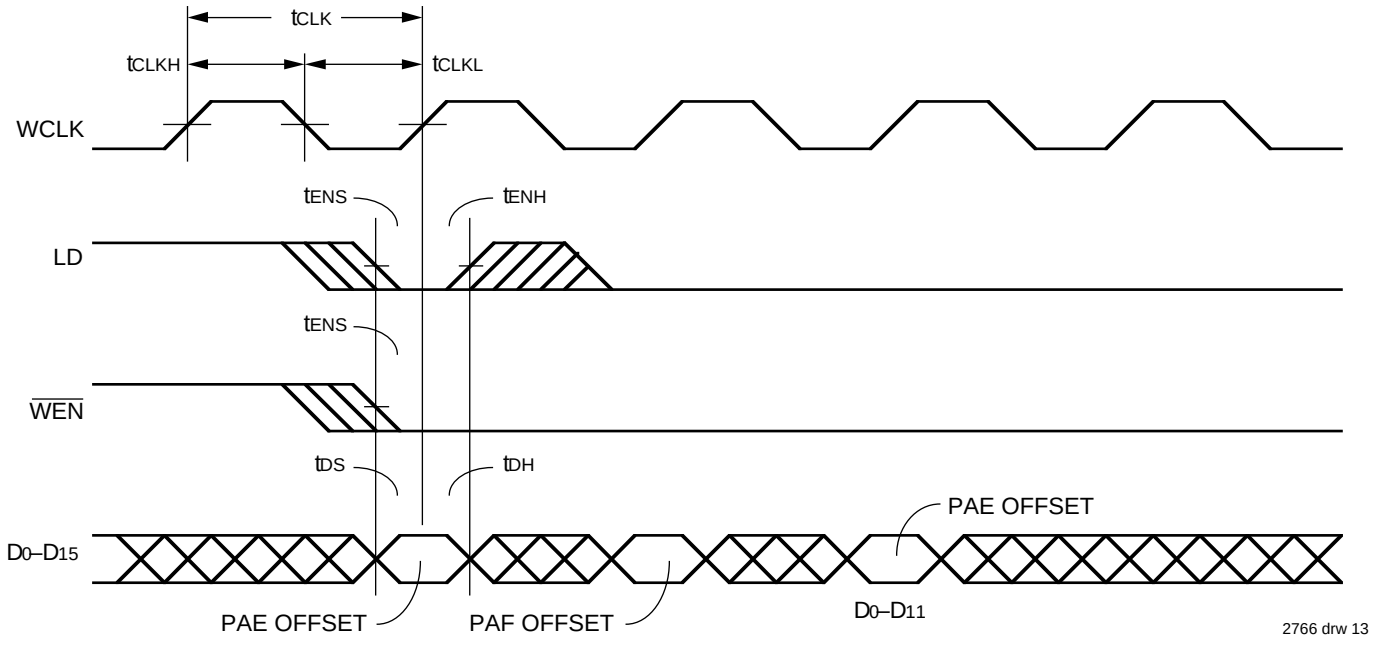


Figure 11. Write Programmable Registers

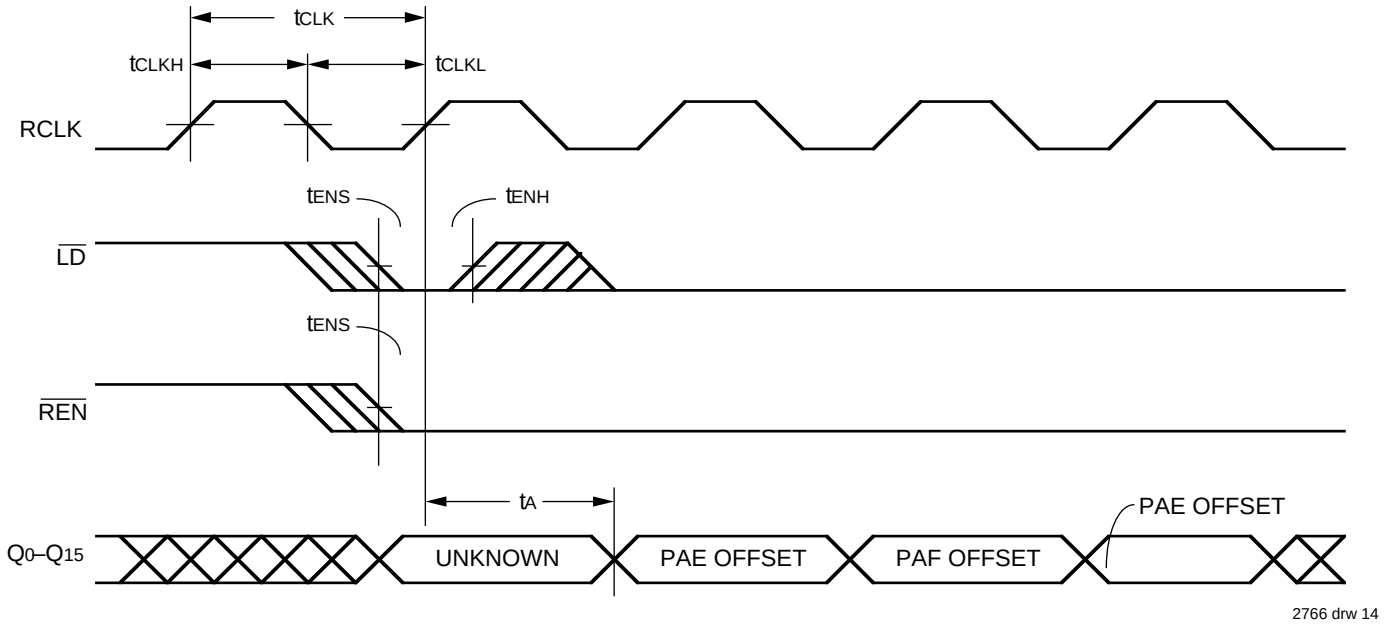
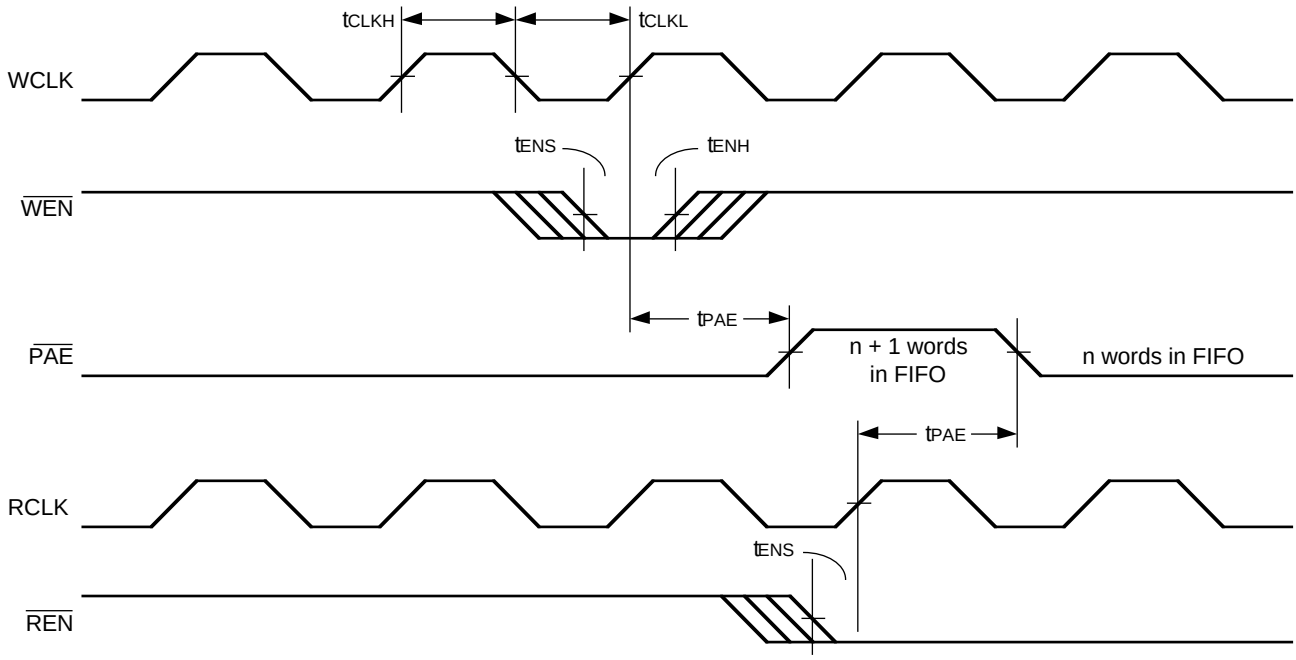
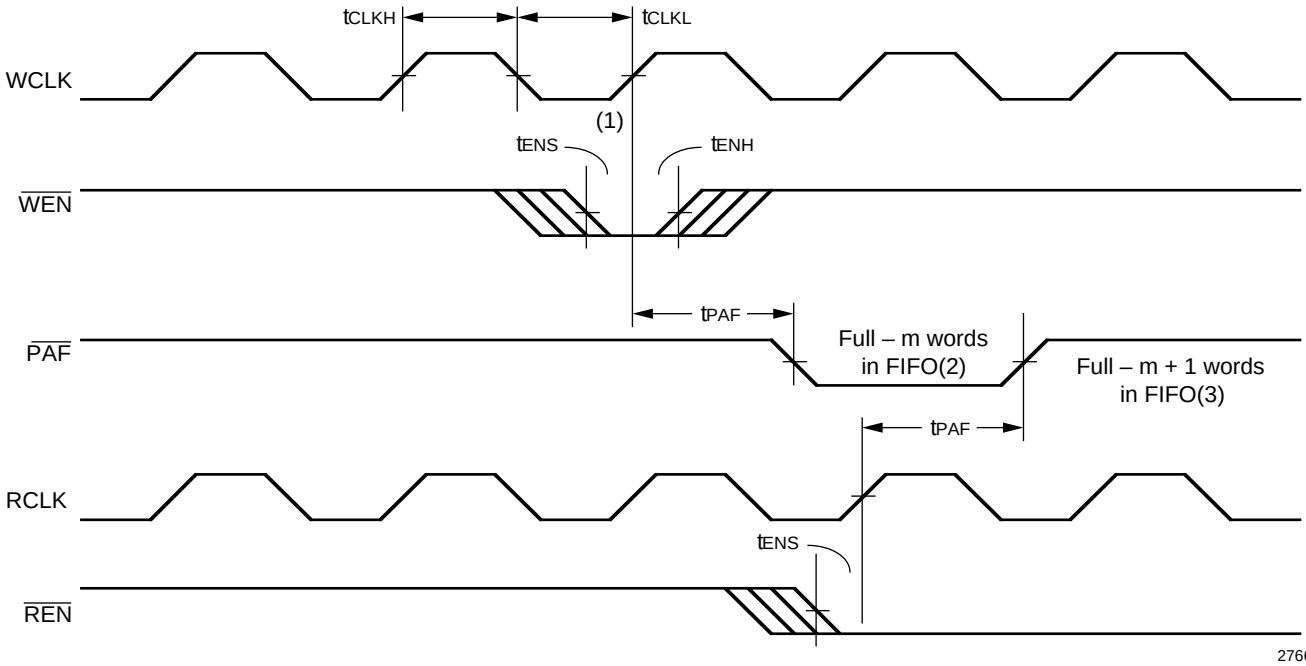


Figure 12. Read Programmable Registers



NOTE:
1. PAE is offset = n. Number of data words written into FIFO already = n.

Figure 13. Programmable Almost Empty Flag Timing



NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 256 - m + 1 for the IDT72205B, 512 - m + 1 for the IDT72215B, 1024 - m + 1 for the IDT72225B, 2048 – m + 1 for the IDT72235B and 4096 – m +1 for the IDT72245B.
2. 256 - m words in IDT72205B, 512 - m words in IDT72215B, 1024 - m words in IDT72225B, 2048 – m words in IDT72235B and 4096 – m words in IDT72245B.
3. 256 - m + 1 words in IDT72205B, 512 - m + 1 words in IDT72215B, 1024 - m + 1 words in IDT72225B, 2048 – m + 1 words in IDT72235B and 4096 – m + 1 words in IDT72245B.

Figure 14. Programmable Almost-Full Flag Timing

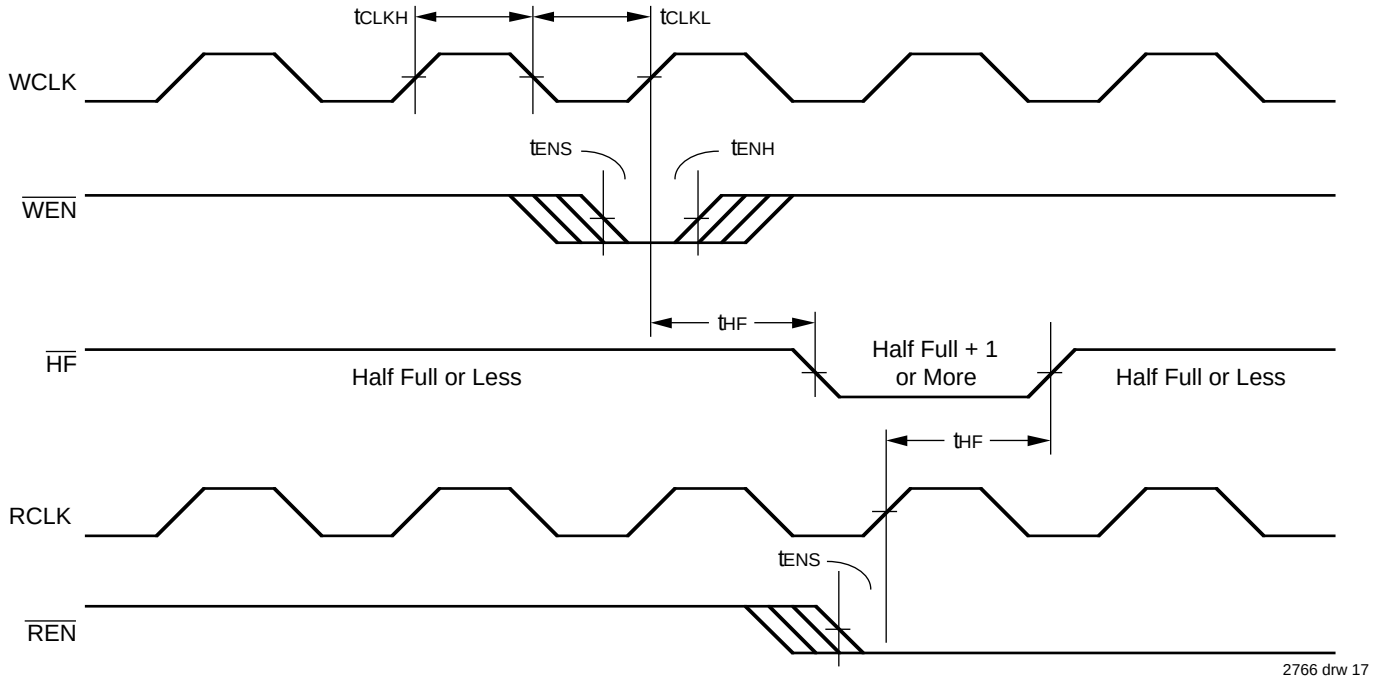
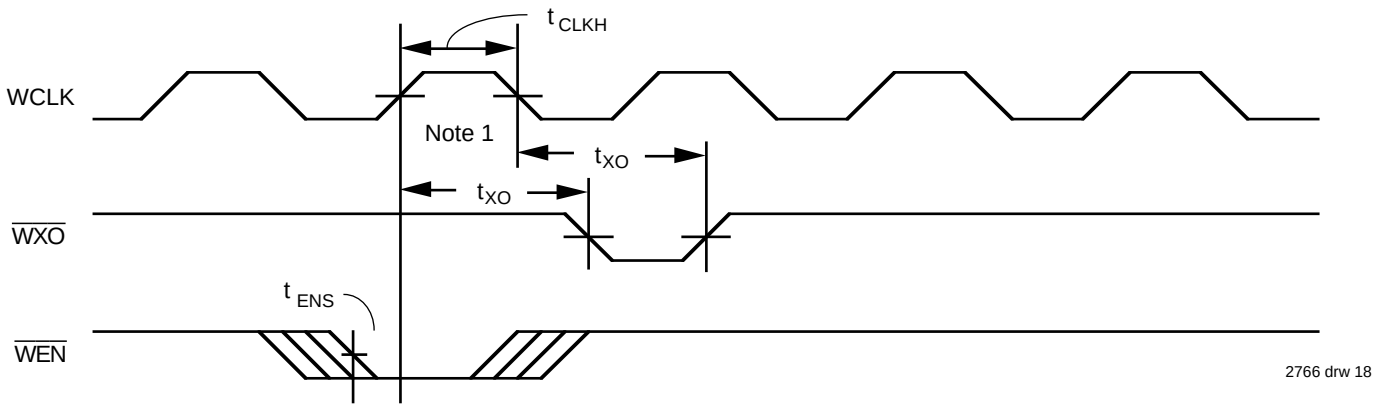
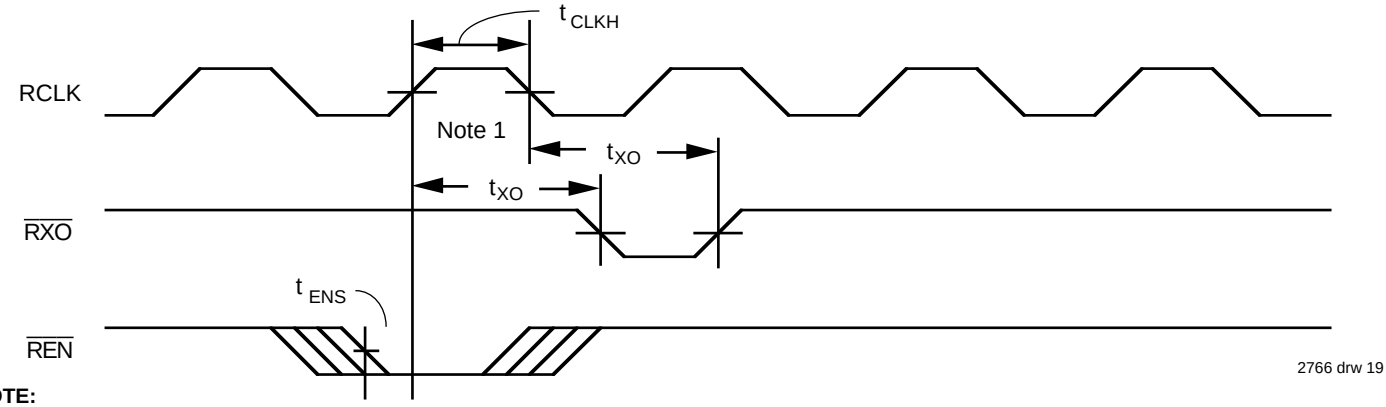


Figure 15. Half-Full Flag Timing



NOTE:
1. Write to Last Physical Location.

Figure 16. Write Expansion Out Timing



NOTE:
1. Read from Last Physical Location.

Figure 17. Read Expansion Out Timing

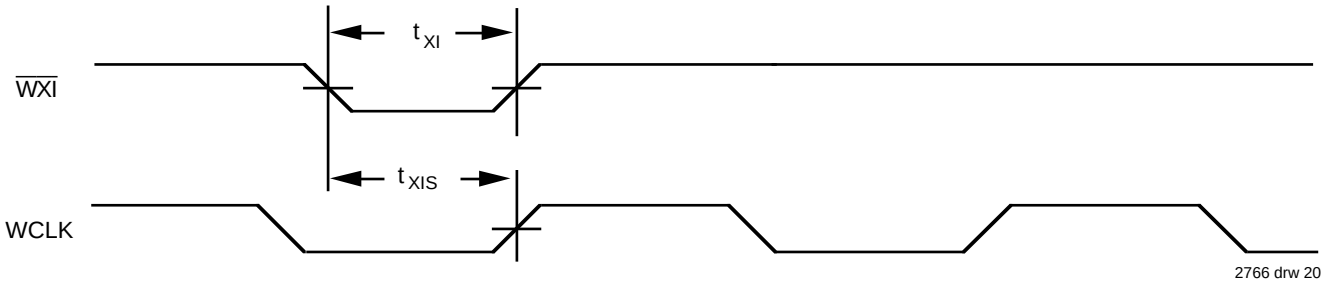


Figure 18. Write Expansion In Timing

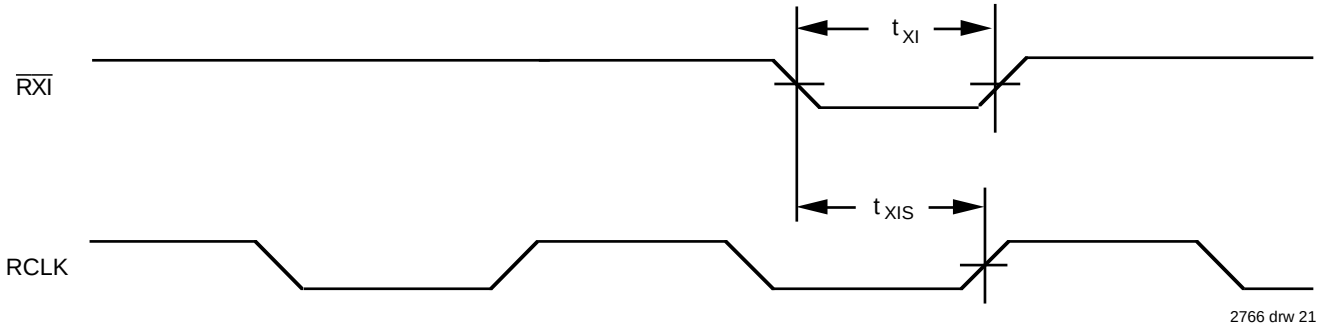


Figure 19. Read Expansion In Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72205LB/72215LB/72225LB/72235LB/72245LB may be used when the application requirements are for 256/512/1024/2048/4096 words or less. The IDT72205LB/72215LB/72225LB/72235LB/72245LB are in a single Device Configuration when the Write Exansion In ($\overline{WXI}$), Read Expansion In ($\overline{RXI}$), and First Load ($\overline{FL}$) control inputs are grounded (Figure 20).

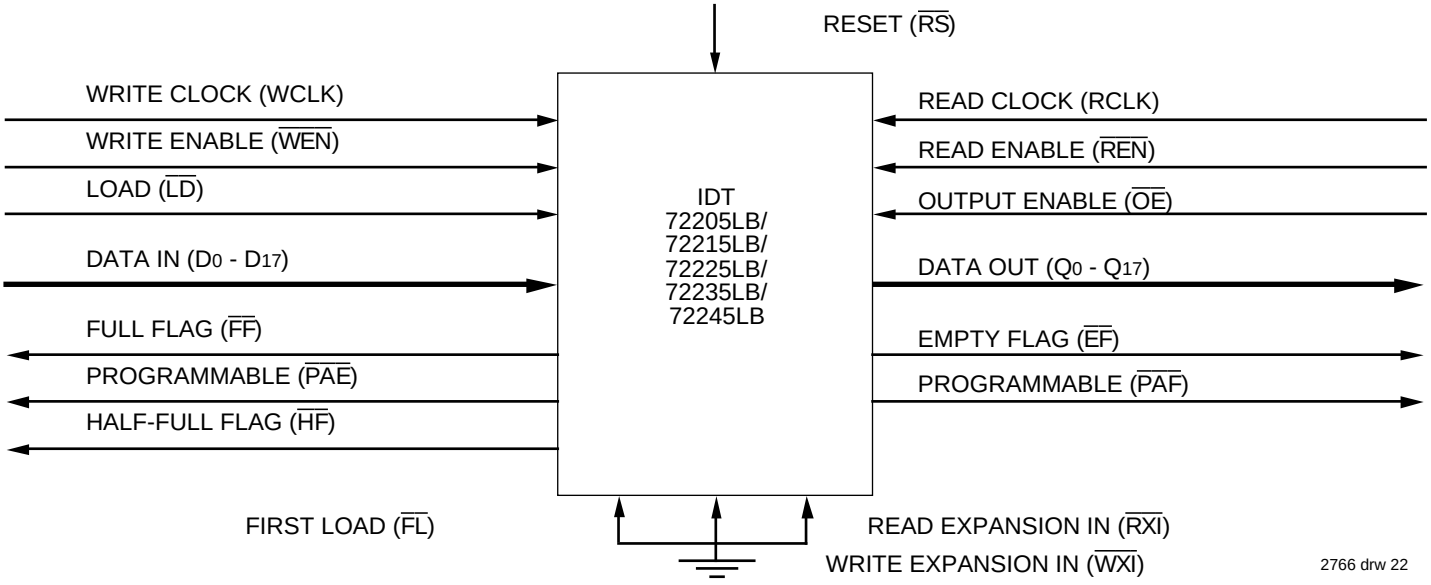
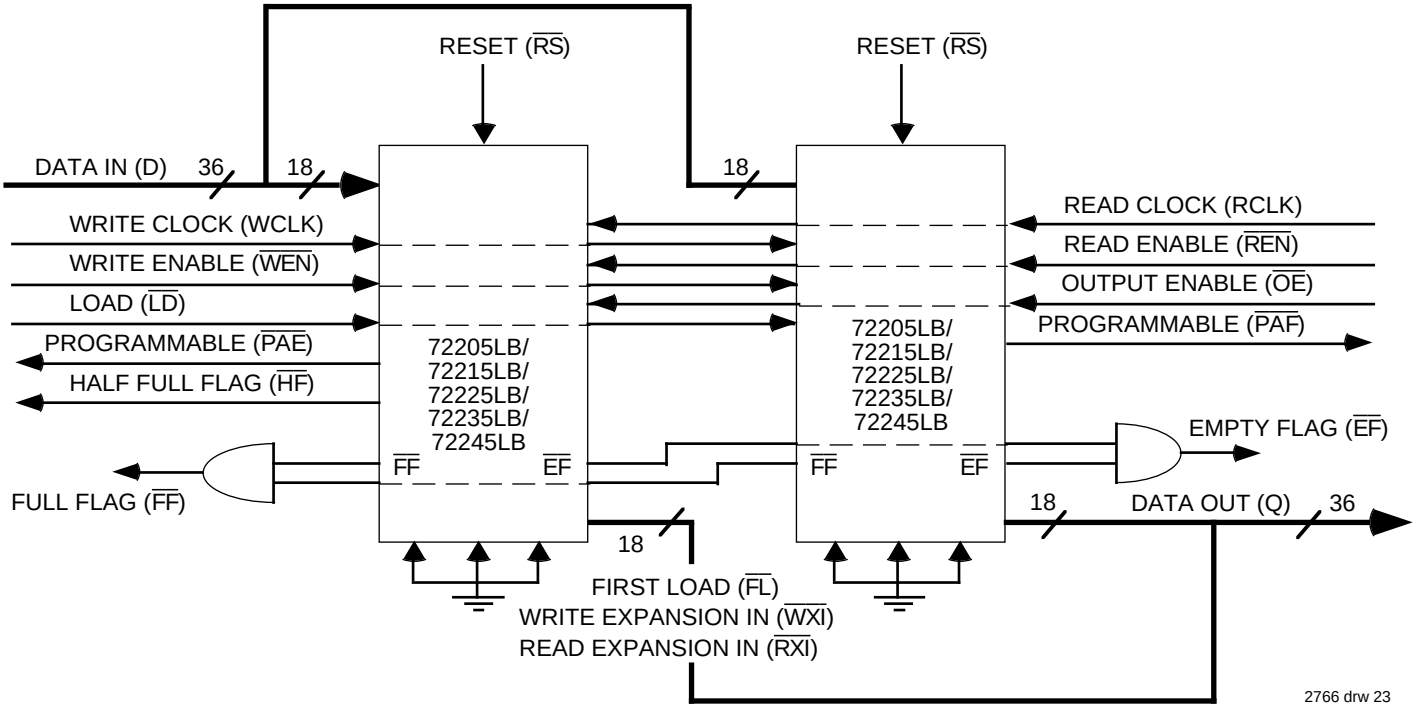


Figure 20. Block Diagram of Single 256 x 18/512 x 18/1024 x 18/2048 x 18/4096 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the Empty Flag and Full Flag. Because of variations in skew between RCLK and WCLK, it is possible for flag assertion and deassertion to vary by one cycle between FIFOs. To avoid problems the user must create composite flags by ANDing the Empty Flags of every FIFO, and separately ANDing all Full Flags. Figure 21 demonstrates a 36-word width by using two IDT72205B/72215B/72225B/72235B/72245Bs. Any word width can be attained by adding additional IDT72205B/72215B/72225B/72235B/72245Bs. Please see the Application Note AN-83.



NOTE:
1. Do not connect any output control signals directly together.

Figure 21. Block Diagram of 256 x 36/512 x 36/1024 x 36/2048 x 36/4096 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

DEPTH EXPANSION CONFIGURATION (WITH PROGRAMMABLE FLAGS)

The IDT72205LB/72215LB/72225LB/72235LB/72245LB can easily be adapted to applications requiring more than 256/512/1024/2048/4096 words of buffering. Figure 22 shows Depth Expansion using three IDT72205LB/72215LB/72225LB/72235LB/72245LBs. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load (FL) control input.
2. All other devices must have FL in the HIGH state.
3. The Write Expansion Out (WXO) pin of each device must be tied to the Write Expansion In (WXI) pin of the next device. See Figure 24.
4. The Read Expansion Out (RXO) pin of each device must be tied to the Read Expansion In (RXI) pin of the next device. See Figure 24.
5. All Load (LD) pins are tied together.
6. The Half-Full Flag (HF) is not available in the Depth Expansion Configuration.
7. EF, FF, PAE, and PAF are created with composite flags by ORing together every respective flags for monitoring. The composite PAE and PAF flags are not precise.

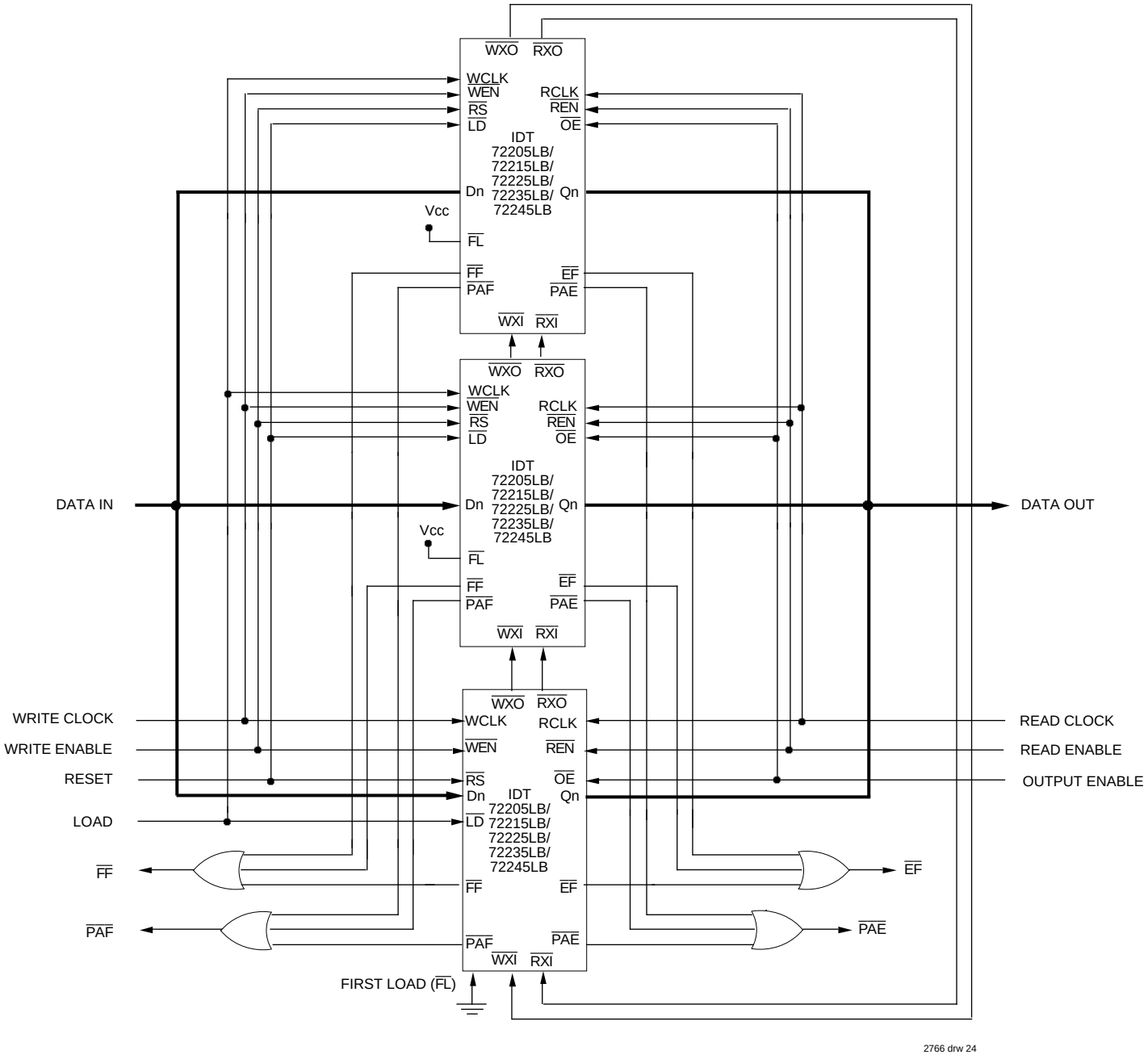
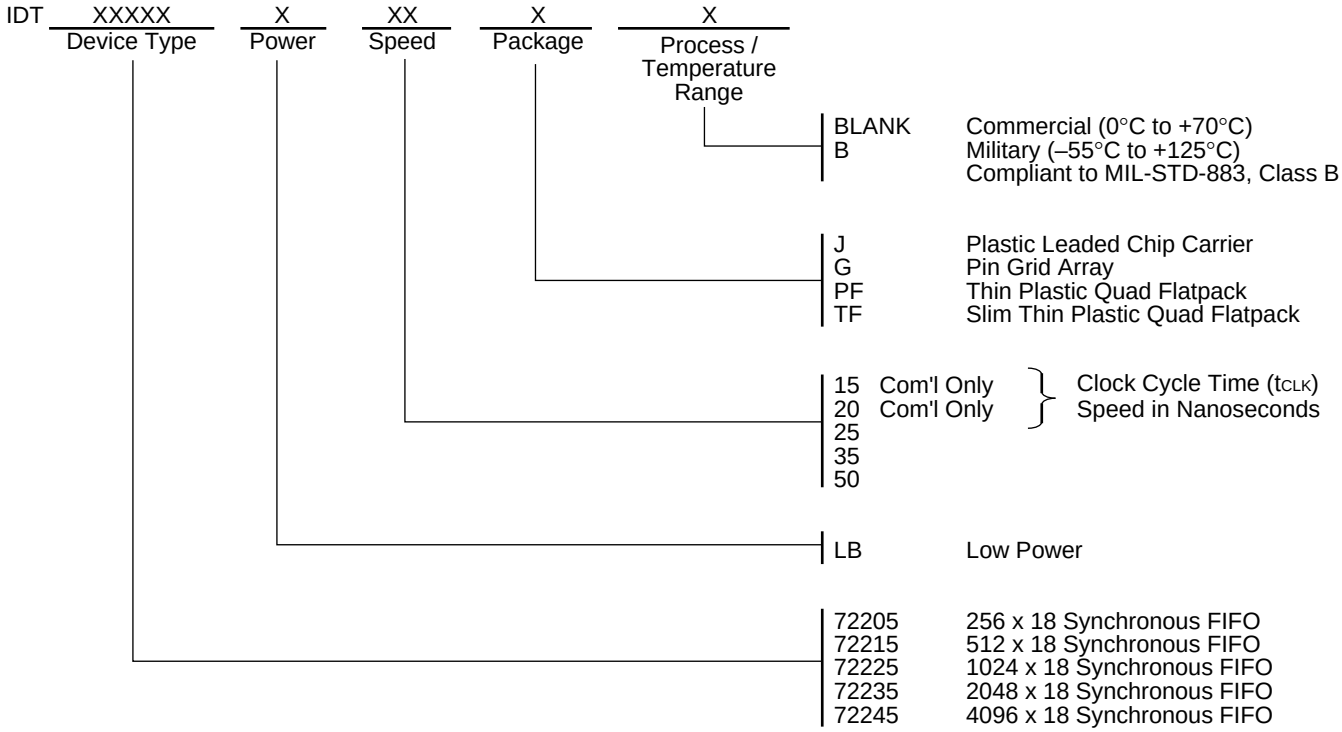


Figure 22. Block Diagram of 768 x 18/1536 x 18/3072 x 18/6144 x 18/12288 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

ORDERING INFORMATION



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