



Integrated Device Technology, Inc.

CMOS PARALLEL 64 x 5-BIT FIFO WITH FLAGS

IDT72413

FEATURES:

- First-In/First-Out Dual-Port memory—45MHz
- 64 x 5 organization
- Low-power consumption
— Active: 200mW (typical)
- RAM-based internal structure allows for fast fall-through time
- Asynchronous and simultaneous read and write
- Expandable by bit width
- Cascadable by word depth
- Half-Full and Almost-Full/Empty status flags
- IDT72413 is pin and functionally compatible with the MMI67413
- High-speed data communications applications
- Bidirectional and rate buffer applications
- High-performance CMOS technology
- Available in plastic DIP, CERDIP and SOIC
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT72413 is a 64 x 5, high-speed First-In/First-Out (FIFO) that loads and empties data on a first-in-first-out basis. It is expandable in bit width. All speed versions are cascadable in depth.

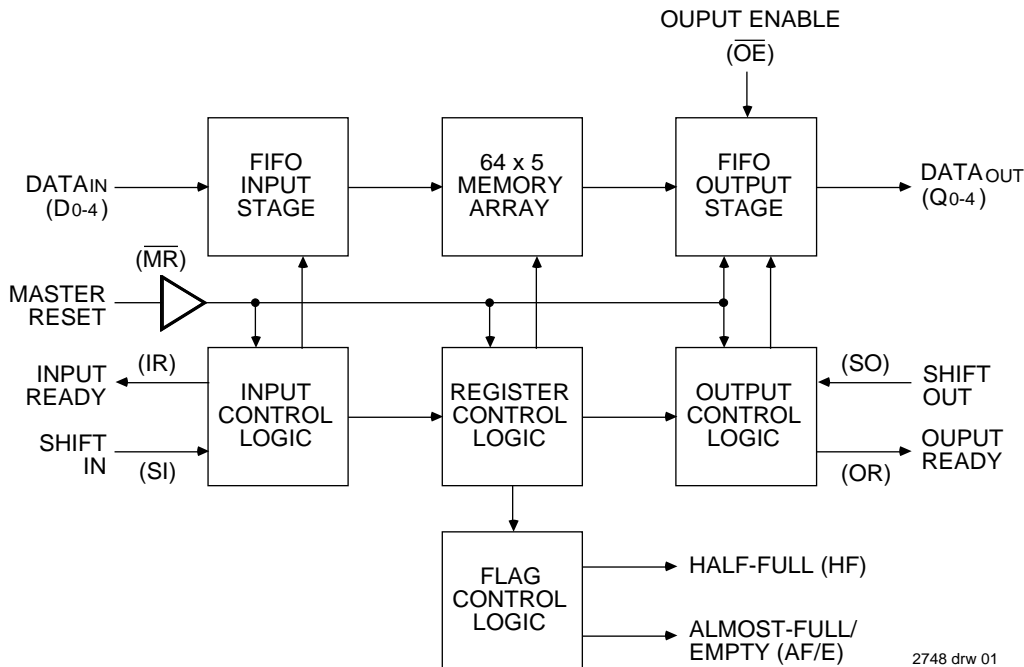
The FIFO has a Half-Full Flag, which signals when it has 32 or more words in memory. The Almost-Full/Empty Flag is active when there are 56 or more words in memory or when there are 8 or less words in memory.

The IDT72413 is pin and functionally compatible to the MMI67413. It operates at a shift rate of 45MHz. This makes it ideal for use in high-speed data buffering applications. The IDT72413 can be used as a rate buffer, between two digital systems of varying data rates, in high-speed tape drivers, hard disk controllers, data communications controllers and graphics controllers.

The IDT72413 is fabricated using IDT's high-performance CMOS process. This process maintains the speed and high output drive capability of TTL circuits in low-power CMOS.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



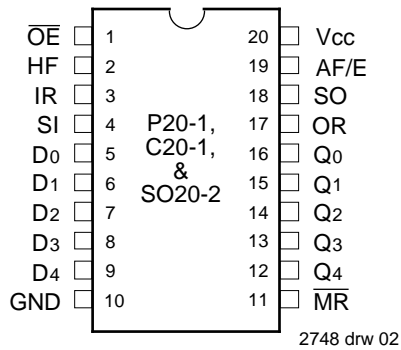
2748 drw 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

DECEMBER 1996

PIN CONFIGURATION



DIP/SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE:

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1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE:

2748 tbl 02

1. This parameter is sampled and not 100% tested.
2. Characterized values, not currently listed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Military Supply Voltage	4.5	5.0	5.5	V
VCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	—	V
VIL ⁽¹⁾	Input Low Voltage	—	—	0.8	V

NOTE:

2748 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$; Military: $V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Symbol	Parameter	Test Conditions			Min.	Max.	Unit		
IIL	Low-Level Input Current	$V_{CC} = \text{Max.}, GND \leq V_I \leq V_{CC}$			-10	—	μA		
IiH	High-Level Input Current	$V_{CC} = \text{Max.}, GND \leq V_I \leq V_{CC}$			—	10	μA		
VOL	Low-Level Output Current	$V_{CC} = \text{Min.}$	IoL (Q0-4)	Mil.	12mA	—	0.4	V	
				Com'l.	24mA				
			IoL (IR, OR) ⁽¹⁾		8mA				
			IoL (HF, AF/E)		8mA				
VOH	High-Level Output Current	$V_{CC} = \text{Min.}$	IoH (Q0-4)		-4mA	2.4	—	V	
			IoH (IR, OR)		-4mA				
			IoH (HF, AF/E)		-4mA				
Ios ⁽²⁾	Output Short-Circuit Current	$V_{CC} = \text{Max.}$	$V_O = 0V$		-20	-110	mA		
IHZ	Off-State Output Current	$V_{CC} = \text{Max.}$	$V_O = 2.4V$		—	20	μA		
ILZ		$V_{CC} = \text{Max.}$	$V_O = 0.4V$		-20	—			
Icc ⁽³⁾	Supply Current	$V_{CC} = \text{Max.}, OE = \text{HIGH}$	Inputs LOW, $f = 25\text{MHz}$	Mil.	—	70	mA		
				Com'l.	—	60			

NOTES:

2748 tbl 04

- Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25MHz.
- Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Guaranteed by design, but not currently tested.
- For frequencies greater than 25MHz, $I_{CC} = 60\text{mA} + (1.5\text{mA} \times [f - 25\text{MHz}])$ commercial and $I_{CC} = 70\text{mA} + (1.5\text{mA} \times [f - 25\text{MHz}])$ military.

OPERATING CONDITIONS

(Commercial: $V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$; Military: $V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Symbol	Parameters	Figure	Commercial		Military & Commercial		Military & Commercial		Unit
			IDT72413L45		IDT72413L35		IDT72413L25		
			Min.	Max.	Min.	Max.	Min.	Max.	
tSIH ⁽¹⁾	Shift in HIGH Time	2	9	—	9	—	16	—	ns
tSIL ⁽¹⁾	Shift in LOW Time	2	11	—	17	—	20	—	ns
tIDS	Input Data Set-up	2	0	—	0	—	0	—	ns
tIDH	Input Data Hold Time	2	13	—	15	—	25	—	ns
tSOH ⁽¹⁾	Shift Out HIGH Time	5	9	—	9	—	16	—	ns
tSOL	Shift Out LOW Time	5	11	—	17	—	20	—	ns
tMRW	Master Reset Pulse	8	20	—	30	—	35	—	ns
tMRS	Master Reset Pulse to SI	8	20	—	35	—	35	—	ns

NOTE:

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- Since the FIFO is a very high-speed device, care must be exercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length is recommended.

AC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5.0V \pm 10\%$, $T_A = 0^\circ C$ to $+70^\circ C$; Military: $V_{CC} = 5.0V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$)

Symbol	Parameters	Figure	Commercial		Mil. & Com'l		Mil. & Com'l		Unit
			IDT72413L45		IDT72413L35		IDT72413L25		
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{IN}	Shift In Rate	2	—	45	—	35	—	25	MHz
$t_{IRL}^{(1)}$	Shift In \uparrow to Input Ready LOW	2	—	18	—	18	—	28	ns
$t_{IRH}^{(1)}$	Shift In \downarrow to Input Ready HIGH	2	—	18	—	20	—	25	ns
f_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	MHz
$t_{ORL}^{(1)}$	Shift Out \downarrow to Output Ready LOW	5	—	18	—	18	—	28	ns
$t_{ORH}^{(1)}$	Shift Out \downarrow to Output Ready HIGH	5	—	19	—	20	—	25	ns
$t_{ODH}^{(1)}$	Output Data Hold Previous Word	5	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift Next Word	5	—	19	—	20	—	20	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	25	—	28	—	40	ns
t_{MRORL}	Master Reset \downarrow to Output Ready LOW	8	—	25	—	28	—	30	ns
$t_{MRIRH}^{(3)}$	Master Reset \uparrow to Input Ready HIGH	8	—	25	—	28	—	30	ns
$t_{MRIRL}^{(2)}$	Master Reset \downarrow to Input Ready LOW	8	—	25	—	28	—	30	ns
t_{MRQ}	Master Reset \downarrow to Outputs LOW	8	—	20	—	25	—	35	ns
t_{MRHF}	Master Reset \downarrow to Half-Full Flag	8	—	25	—	28	—	40	ns
t_{MRAFE}	Master Reset \downarrow to AF/E Flag	8	—	25	—	28	—	40	ns
$t_{IPH}^{(3)}$	Input Ready Pulse HIGH	4	5	—	5	—	5	—	ns
$t_{OPH}^{(3)}$	Output Ready Pulse HIGH	7	5	—	5	—	5	—	ns
$t_{ORD}^{(3)}$	Output Ready \uparrow HIGH to Valid Data	5	—	5	—	5	—	7	ns
t_{AEH}	Shift Out \uparrow to AF/E HIGH	9	—	28	—	28	—	40	ns
t_{AEL}	Shift In \uparrow to AF/E	9	—	28	—	28	—	40	ns
t_{AFL}	Shift Out \uparrow to AF/E LOW	10	—	28	—	28	—	40	ns
t_{AFH}	Shift In \uparrow to AF/E HIGH	10	—	28	—	28	—	40	ns
t_{HFH}	Shift In \uparrow to HF HIGH	11	—	28	—	28	—	40	ns
t_{HFL}	Shift Out \uparrow to HF LOW	11	—	28	—	28	—	40	ns
$t_{PHZ}^{(3)}$	Output Disable Delay	12	—	12	—	12	—	15	ns
$t_{PLZ}^{(3)}$		12	—	12	—	12	—	15	
$t_{PLZ}^{(3)}$	Output Enable Delay	12	—	15	—	15	—	20	ns
$t_{PHZ}^{(3)}$		12	—	15	—	15	—	20	

NOTES:

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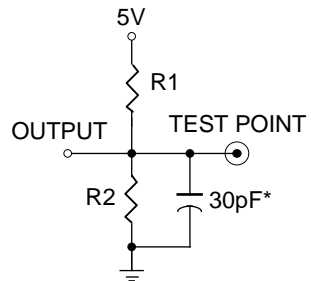
1. Since the FIFO is a very high-speed device, care must be taken in the design of the hardware and the timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1 μ F directly between VCC and GND with very short lead length is recommended.
2. If the FIFO is full, (IR = HIGH), $\overline{MR} \downarrow$ forces IR to go LOW, and $\overline{MR} \uparrow$ causes IR to go HIGH.
3. Guaranteed by design but not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2748 tbl 07

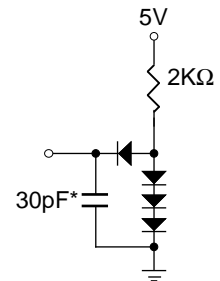
STANDARD TEST LOAD



or equivalent circuit

*Including scope and jig

DESIGN TEST LOAD



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RESISTOR VALUES FOR STANDARD TEST LOAD

IoL	R1	R2
24mA	200Ω	300Ω
12mA	390Ω	760Ω
8mA	600Ω	1200Ω

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Figure 1. Output Load

FUNCTIONAL DESCRIPTION:

The IDT72413, 65 x 5 FIFO is designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable (\overline{OE}) provides the capability of three-stating the FIFO outputs.

FIFO RESET

The FIFO must be reset upon power up using the Master Reset (\overline{MR}) signal. This causes the FIFO to enter an empty state signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Q0-4) will be LOW.

DATA INPUT

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes the Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

DATA OUTPUT

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out.

FALL-THROUGH MODE

The FIFO operates in a Fall-Through Mode when data gets shifted into an empty FIFO. After the fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH.

A Fall-Through Mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO. The fall-through delay of a RAM-based FIFO (one clock cycle) is far less than the delay of a Shift register-based FIFO.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA INPUT (D0-4)

Data input lines. The IDT72413 has a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the D0-4 lines. The data has to meet set-up and hold time requirements with respect to the rising edge of SI.

SHIFT OUT (SO)

Shift Out controls the outputs data from the FIFO.

MASTER RESET (MR)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

HALF-FULL FLAG (HF)

Half-Full Flag signals when the FIFO has 32 or more words in it.

TIMING DIAGRAMS

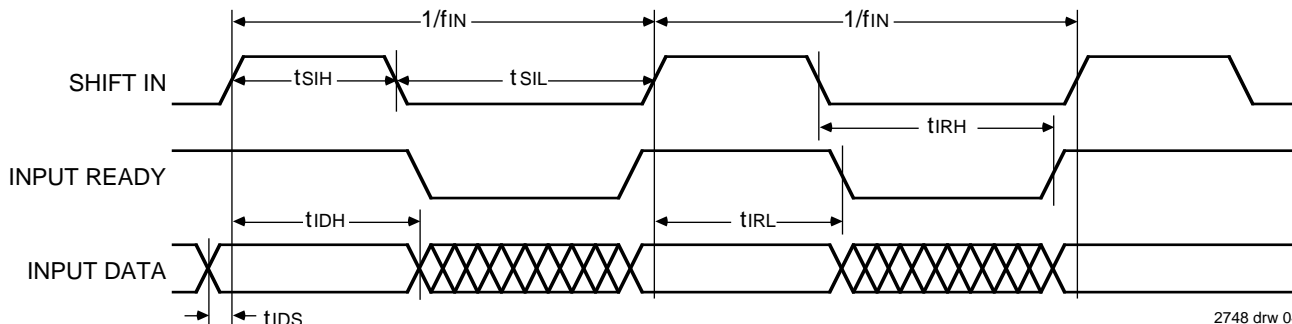


Figure 2. Input Timing

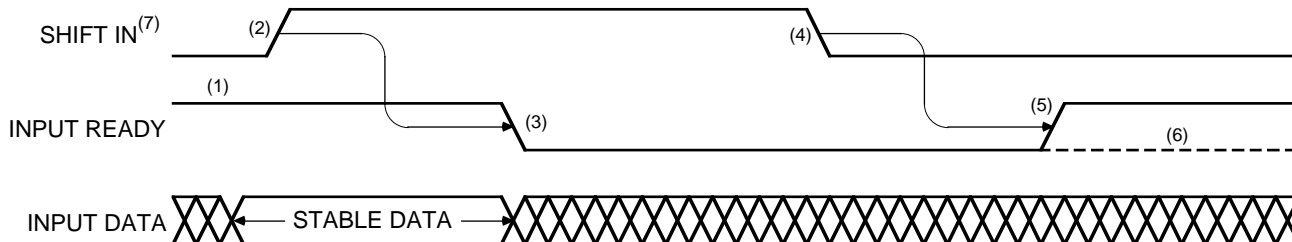
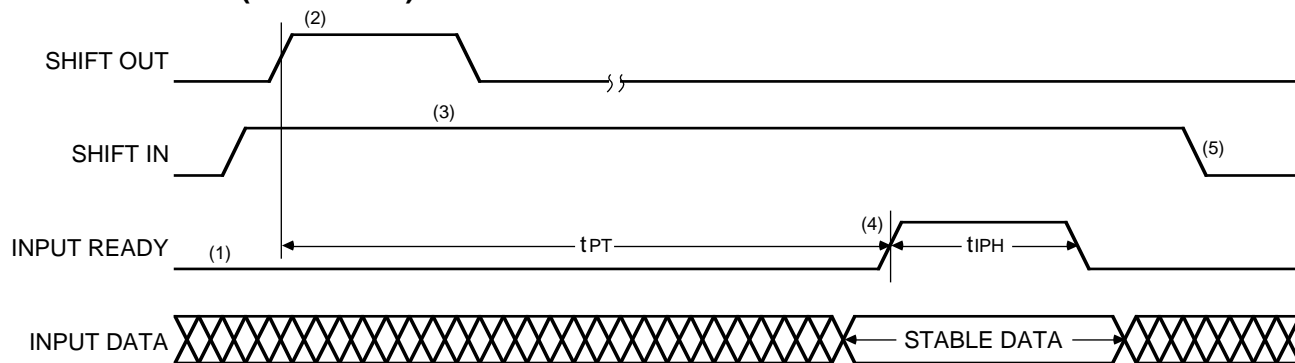


Figure 3. The Mechanism of Shifting Data Into the FIFO

NOTES:

1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the FIFO.
3. Input Ready goes LOW indicating the FIFO is unavailable for new data.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full, then the Input Ready remains LOW.
7. Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).

TIMING DIAGRAMS (Continued)

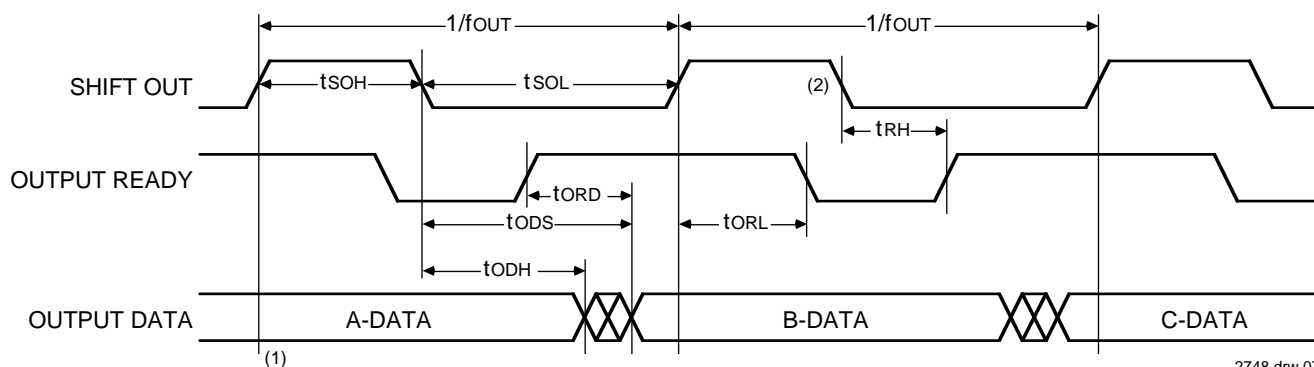


NOTES:

1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until $(t_{PT} + t_{IPH})$.

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Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH



NOTES:

1. This data is loaded consecutively A, B, C.
2. Output data changes on the falling edge of SO after a valid Shift Out sequence, i.e., OR and SO are both high together.

2748 drw 07

Figure 5. Output Timing



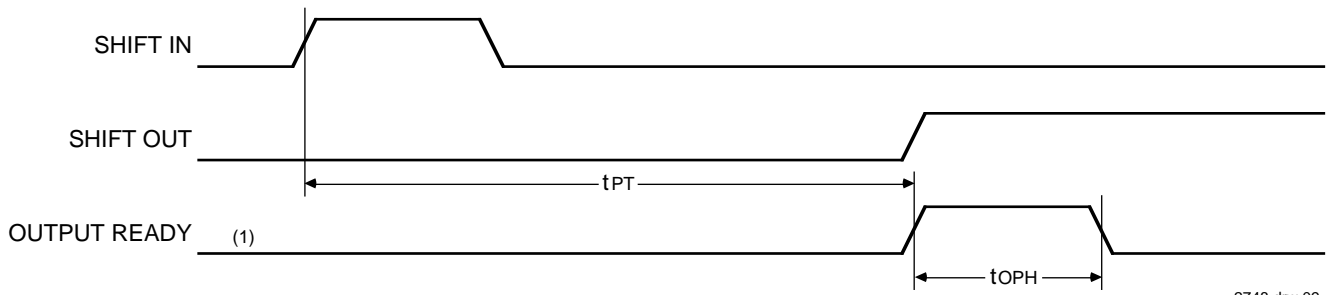
NOTES:

1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. Read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) will be available at the FIFO outputs after t_{ORD} ns.
6. If the FIFO has only one word loaded (A DATA), Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

2748 drw 08

Figure 6. The Mechanism of Shifting Data Out of the FIFO

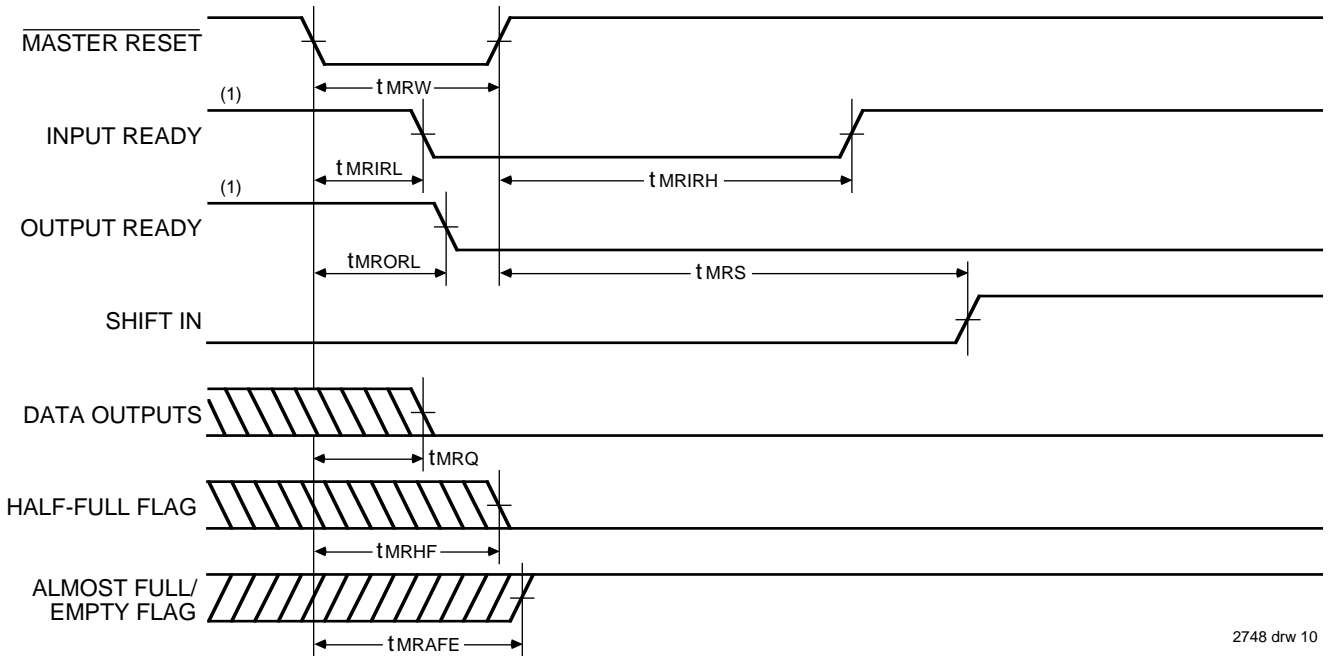
TIMING DIAGRAMS (Continued)



2748 drw 09

NOTE:
1. FIFO initially empty.

Figure 7. t_{PT} and t_{OPH} Specification

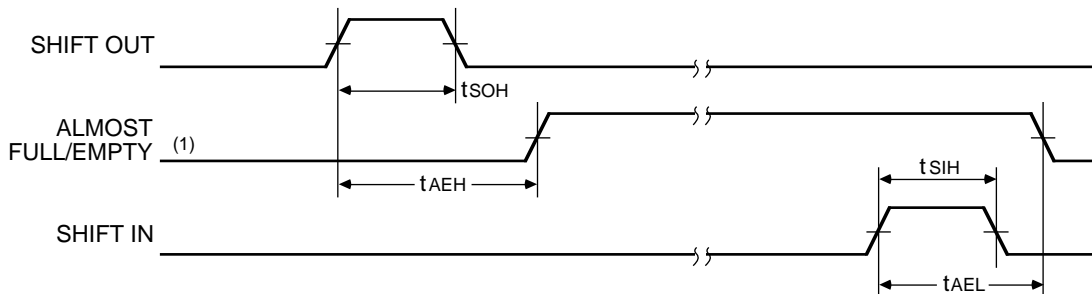


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NOTE:
1. FIFO is partially full.

Figure 8. Master Reset Timing

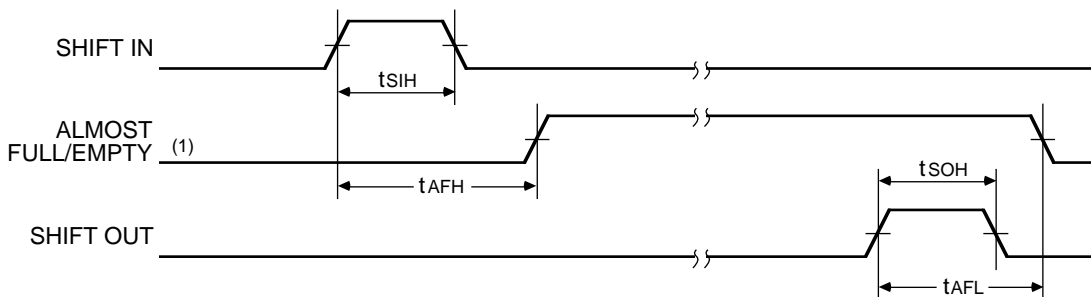
TIMING DIAGRAMS (Continued)



NOTE:
1. FIFO contains 9 words (one more than Almost-Empty).

2748 drw 11

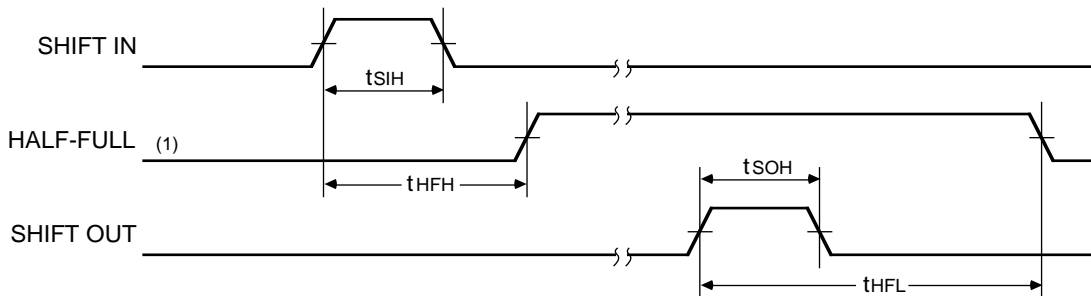
Figure 9. tAEH and tAEL Specifications



NOTE:
1. FIFO contains 55 words (one short of Almost-Full).

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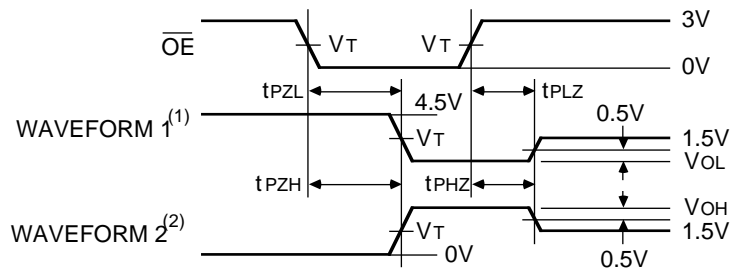
Figure 10. tAFH and tAFL Specifications



NOTE:
1. FIFO contains 31 words (one short of Half-Full).

2748 drw 13

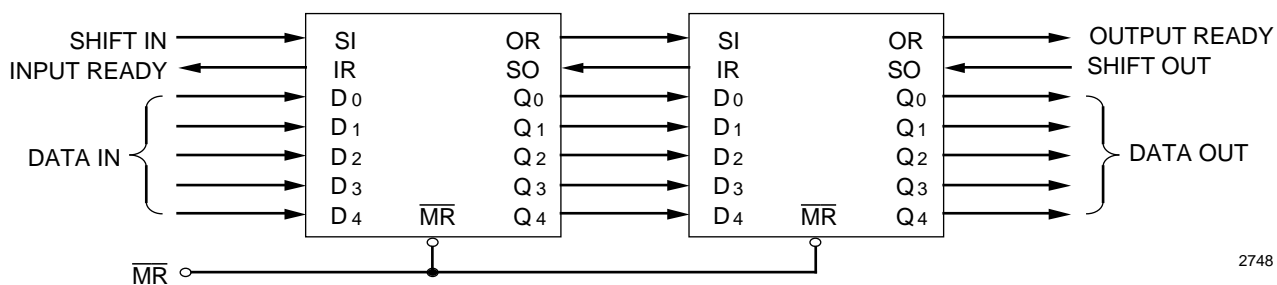
Figure 11. tHFL and tHFH Specifications



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NOTES:
1. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Figure 12. Enable and Disable



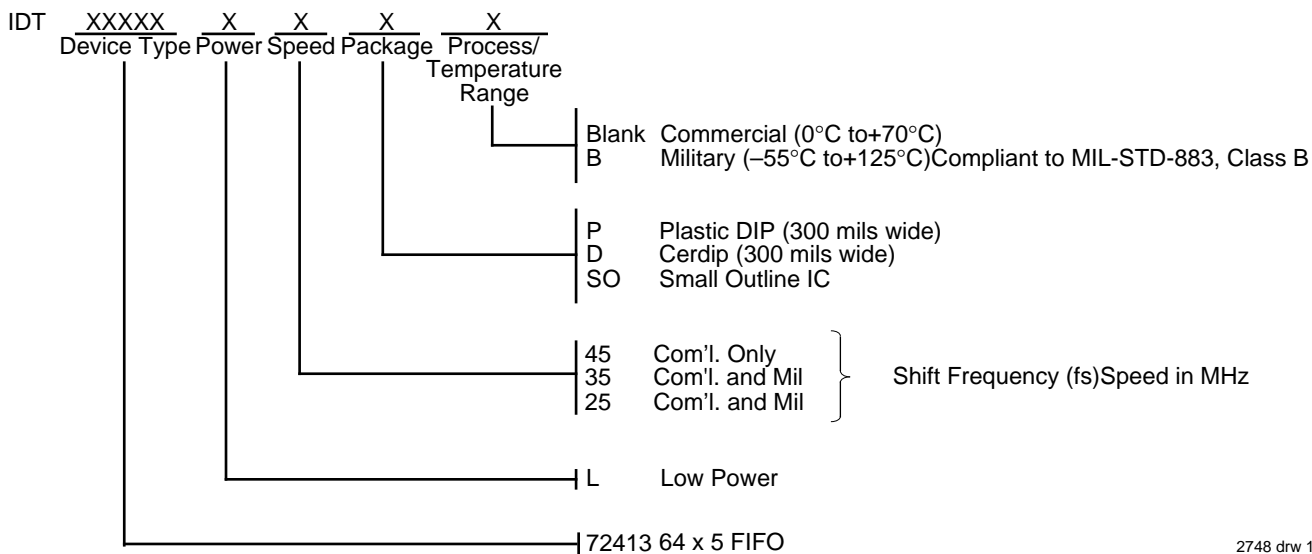
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NOTE:

- FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 15. 128 x 5 Depth Expansion

ORDERING INFORMATION



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