

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BUS TRANSCEIVER/REGISTERS

IDT54/74FCT163652/A/C
PRODUCT PREVIEW

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
- Extended commercial range of -40°C to +85°C
- VCC = 3.3V ±0.3V, Normal Range or VCC = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The IDT54/74FCT163652/A/C 16-bit registered transceivers are built using advanced dual metal CMOS technology.

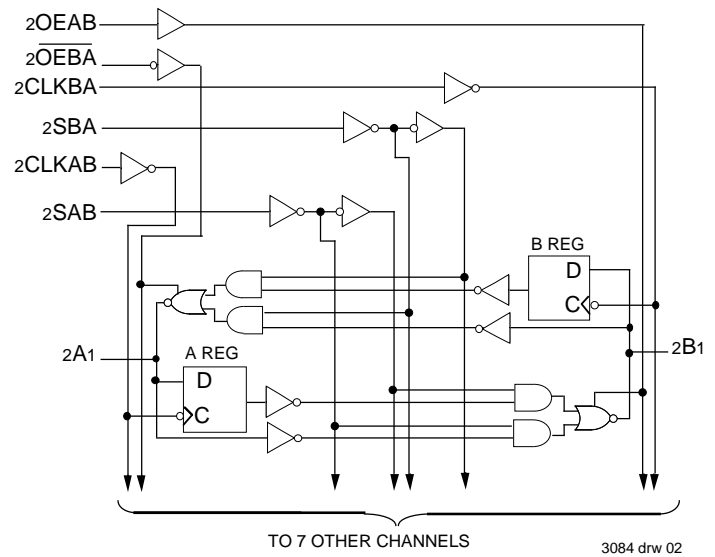
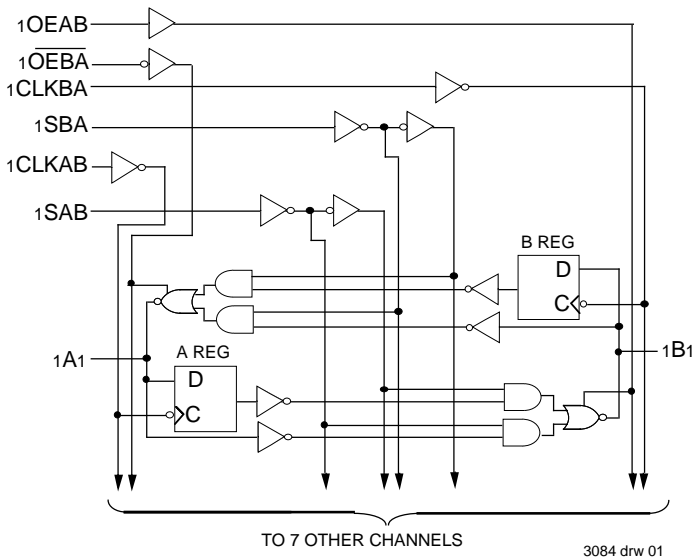
These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. For example, the xOEAB and xOEBA signals control the transceiver functions.

The xSAB and xSBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A LOW input level selects real-time data and a HIGH level selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D-flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (xCLKAB or xCLKBA), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT163652/A/C have series current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM

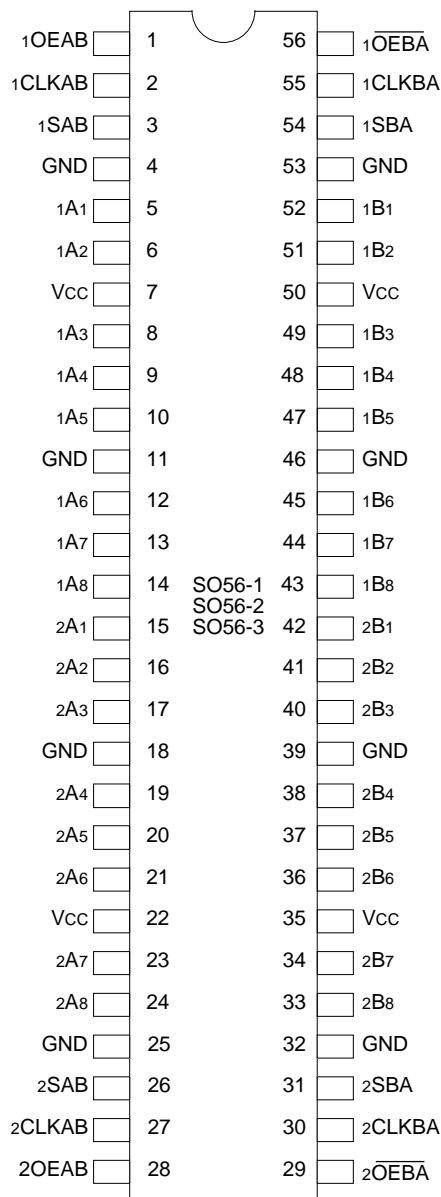


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

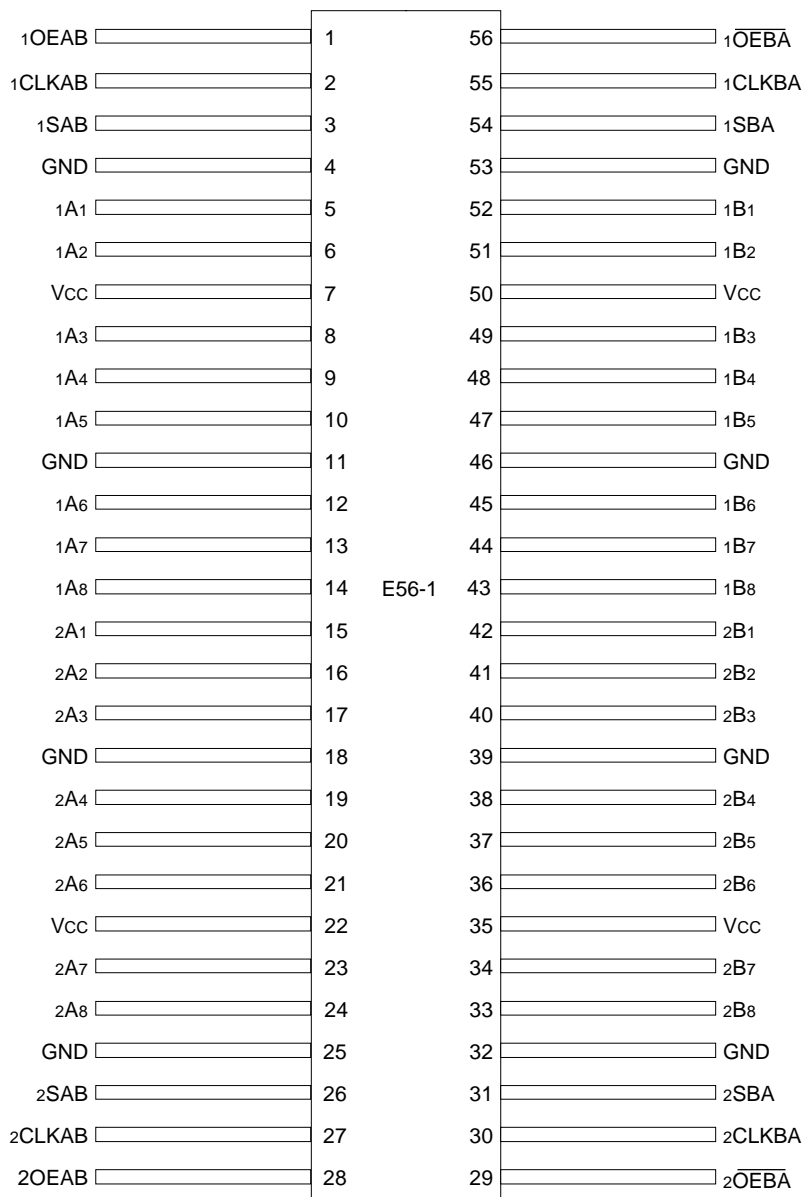
AUGUST 1996

PIN CONFIGURATIONS



SSOP/
TSSOP/TVSOP
TOP VIEW

3084 drw 03



CERPACK
TOP VIEW

3084 drw 04

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, xOEBA	Output Enable Inputs

3084 tbi 01

FUNCTION TABLE⁽²⁾

Inputs						Data I/O ⁽¹⁾		Operation or Function
xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified ⁽¹⁾	Store A, Hold B
H	H	↑	↑	X ⁽²⁾	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified ⁽¹⁾	Input	Hold A, Store B
L	L	↑	↑	X	X ⁽²⁾	Output	Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

NOTES:

3084 tbl 03

- The data output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered to load both registers.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	3.5	8.0	pF

NOTE:

3084 Ink 02

- This parameter is measured at characterization but not tested.

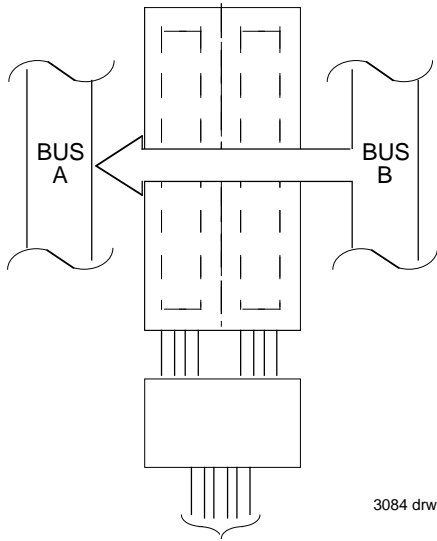
ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V _{TERM} ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +60	mA

NOTES:

3084 Ink 04

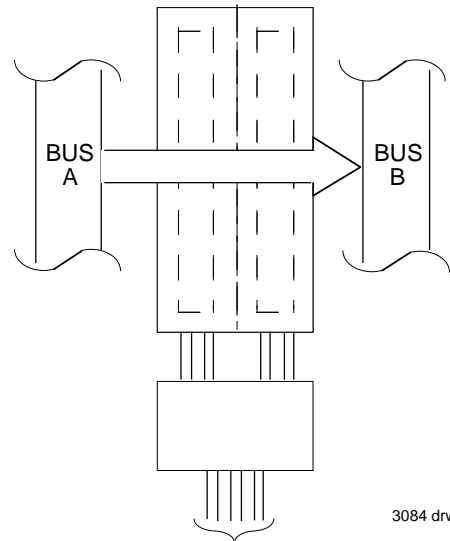
- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- Input terminals.
- Output and I/O terminals.



3084 drw 05

xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

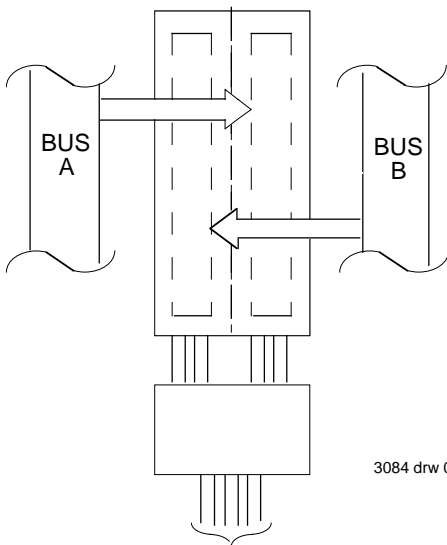
**REAL-TIME TRANSFER
 BUS B TO A**



3084 drw 06

xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

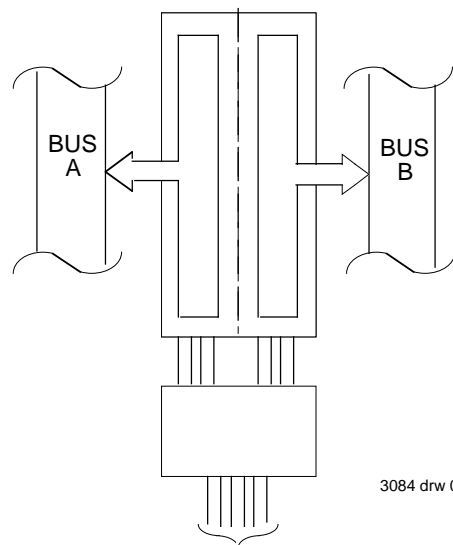
**REAL-TIME TRANSFER
 BUS A TO B**



3084 drw 07

xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

**STORAGE FROM
 A AND/OR B**



3084 drw 08

xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

**TRANSFER STORED
 DATA TO A AND/OR B**

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, VCC = 2.7V to 3.6V; Military: TA = -55°C to +125°C, VCC = 2.7V to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
VIH	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	VCC+0.5	
VIL	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins) ⁽⁶⁾	VCC = Max.	VI = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins) ⁽⁶⁾		VI = VCC	—	—	±1	
IIL	Input LOW Current (Input pins) ⁽⁶⁾		VI = GND	—	—	±1	
	Input LOW Current (I/O pins) ⁽⁶⁾		VI = GND	—	—	±1	
IOZH	High Impedance Output Current (3-State Output pins) ⁽⁶⁾	VCC = Max.	VO = VCC	—	—	±1	μA
IOZL			VO = GND	—	—	±1	
VIK	Clamp Diode Voltage	VCC = Min., IIN = -18mA		—	-0.7	-1.2	V
IODH	Output HIGH Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		-36	-60	-110	mA
IODL	Output LOW Current	VCC = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		50	90	200	mA
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL	IOH = -0.1mA	VCC-0.2	—	—	V
			IOH = -3mA	2.4	3.0	—	
		VCC = 3.0V VIN = VIH or VIL	IOH = -6mA MIL. IOH = -8mA COM'L.	2.4 ⁽⁵⁾	3.0	—	
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IOL = 0.1mA	—	—	0.2	V
			IOL = 16mA	—	0.2	0.4	
			IOL = 24mA	—	0.3	0.55	
		VCC = 3.0V VIN = VIH or VIL	IOL = 24mA	—	0.3	0.50	
IOS	Short Circuit Current ⁽⁴⁾	VCC = Max., VO = GND ⁽³⁾		-60	-135	-240	mA
VH	Input Hysteresis	—		—	150	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	VCC = Max., VIN = GND or VCC	COM'L.	—	0.1	10	μA
			MIL.	—	0.1	100	

3084 Ink 05

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = VCC - 0.6V at rated current.
- The test limit for this parameter is ±5μA at TA = -55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2.0	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOEAB} = \overline{xOEBA} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ ($xCLKBA$) 50% Duty Cycle $\overline{xOEAB} = \overline{xOEBA} = \text{GND}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.0	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.6	1.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ ($xCLKBA$) 50% Duty Cycle $\overline{xOEAB} = \overline{xOEBA} = \text{GND}$ Sixteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.0	5.0 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	3.0	5.3 ⁽⁵⁾	

NOTES:

3084 tbl 08

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$ (I_{CCL} , I_{CCH} and I_{CCZ})
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽⁴⁾

Symbol	Parameter	Condition ⁽¹⁾	FCT163652				FCT163652A				FCT163652C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	—	—	ns
tPZH tPZL	Output Enable Time xOEAB or xOEBA to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	—	—	ns
tPHZ tPLZ	Output Disable Time xOEAB or xOEBA to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	—	—	ns
tsu	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	—	—	ns
th	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	—	—	ns
tw	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

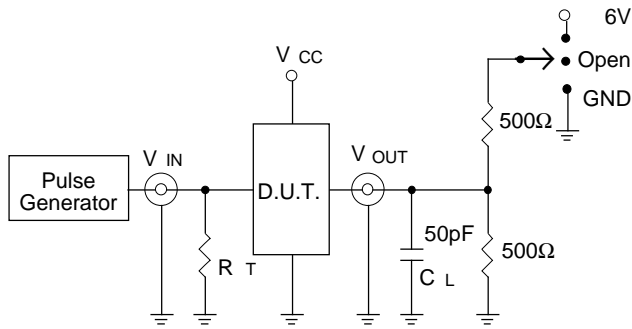
NOTES:

3084 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ± 0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3084 drw 09

SWITCH POSITION

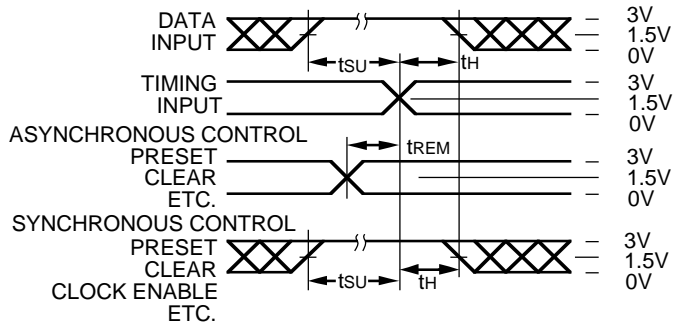
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

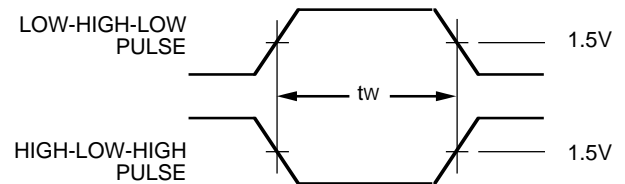
3084 Ink 10

SET-UP, HOLD AND RELEASE TIMES



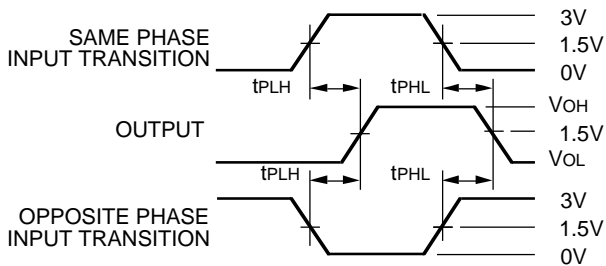
3084 drw 10

PULSE WIDTH



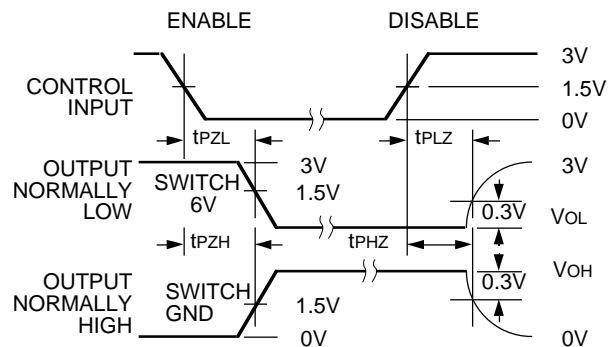
3084 drw 11

PROPAGATION DELAY



3084 drw 12

ENABLE AND DISABLE TIMES



3084 drw 13

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

