Integrated Device Technology, Inc.

512K x 8
CMOS STATIC RAM MODULE

IDT7MB4048

FEATURES:

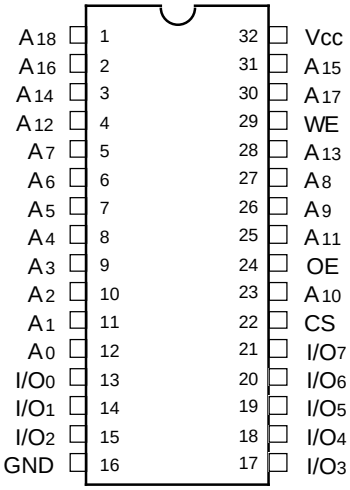
- High-density 4-megabit (512K x 8) Static RAM module
- Fast access time: 25ns (max.)
  Surface mounted plastic packages on a 32-pin, 600 mil FR-4 DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible

DESCRIPTION:

The IDT7MB4048 is a 4-megabit (512K x 8) Static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using four 1 megabit SRAMs and a decoder. The IDT7MB4048 is available with access times as fast as 25ns. The IDT7MB4048 is packaged in a 32-pin FR-4 DIP resulting in the JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7MB4048 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

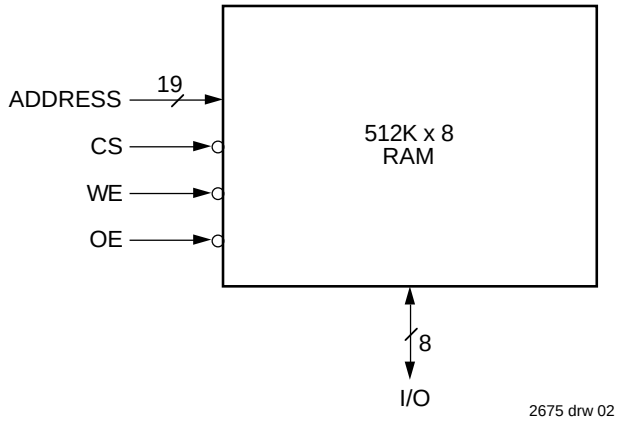
PIN CONFIGURATION



2675 drw 01

DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

I/O_{0-7}	Data Inputs/Outputs
A_{0-18}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

2675 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	D_{IN}	Active

2675 tbl 02

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE: 2675 tbl 03
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2675 tbl 05
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2675 tbl 04
1. V_{IL} = –2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2675 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

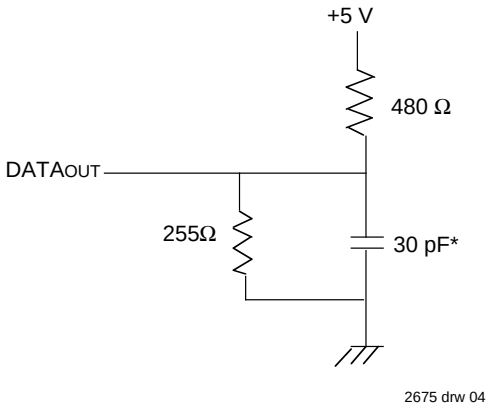
Symbol	Parameter	Test Conditions	7MB4048SxxP		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	8	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	8	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \le V_{IL}$; f = f_{MAX}, Outputs Open	—	480	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \ge V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	_	250	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \ge V_{CC}$ - 0.2V, $V_{IN} \ge V_{CC}$ - 0.2V or ≤ 0.2	—	170	mA

2675 tbl 07

AC TEST CONDITIONS

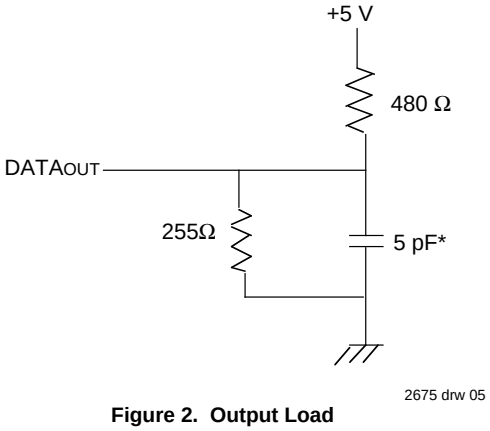
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2675 tbl 09



2675 drw 04

Figure 1. Output Load



2675 drw 05

Figure 2. Output Load (for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

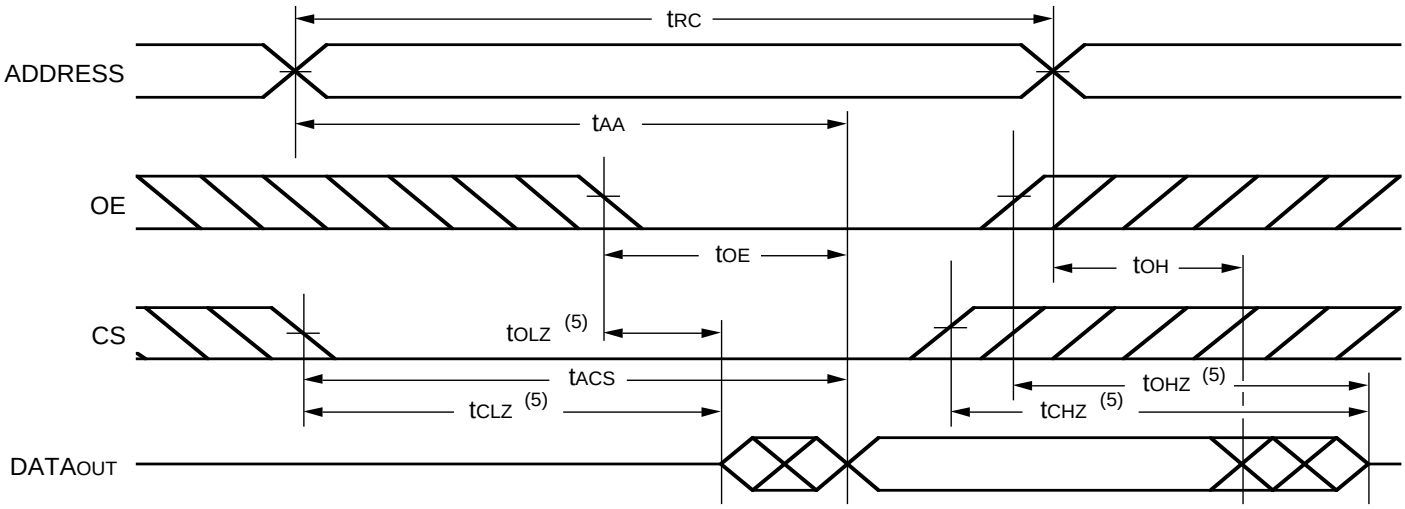
Symbol	Parameter	7MB4048 –25 Min.	7MB4048 –25 Max.	7MB4048 –30 Min.	7MB4048 –30 Max.	7MB4048 –35 Min.	7MB4048 –35 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	15	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	12	—	12	—	15	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	25	—	30	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	17	—	20	—	25	—	ns
t_{AS}(2)	Address Set-up Time	3	—	0	—	0	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End-of-Write	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	20	—	ns
t_{DH}(2)	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}(2)	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	15	—	15	—	15	ns
t_{OW}(1)	Output Active from End-of-Write	2	—	5	—	5	—	ns

NOTES

2675 tbl 10

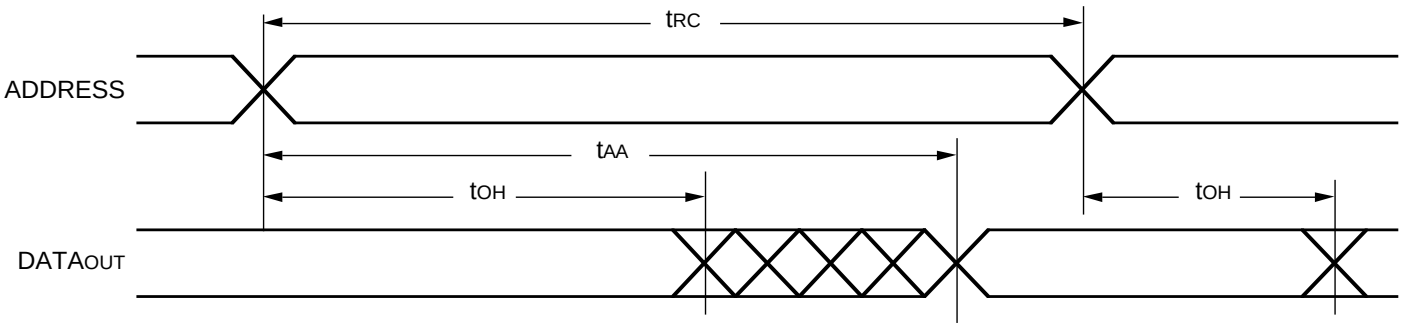
1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 3ns for $\overline{CS}$ controlled write cycles.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



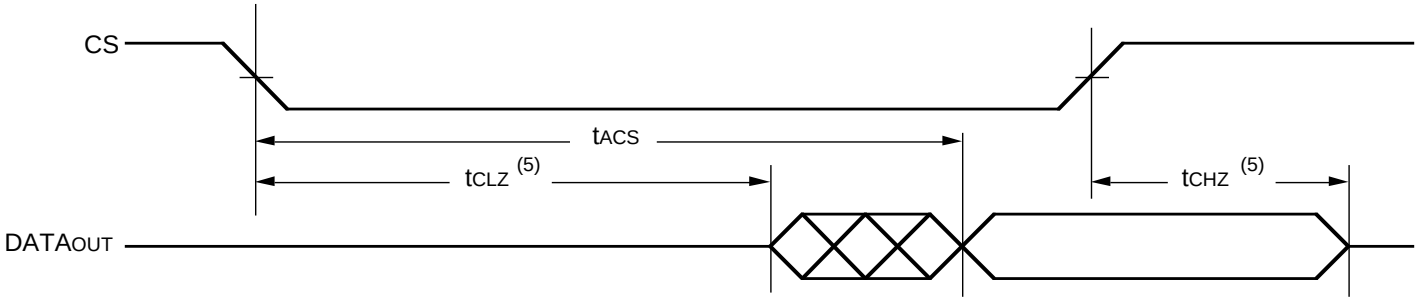
2675 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2675 drw 07

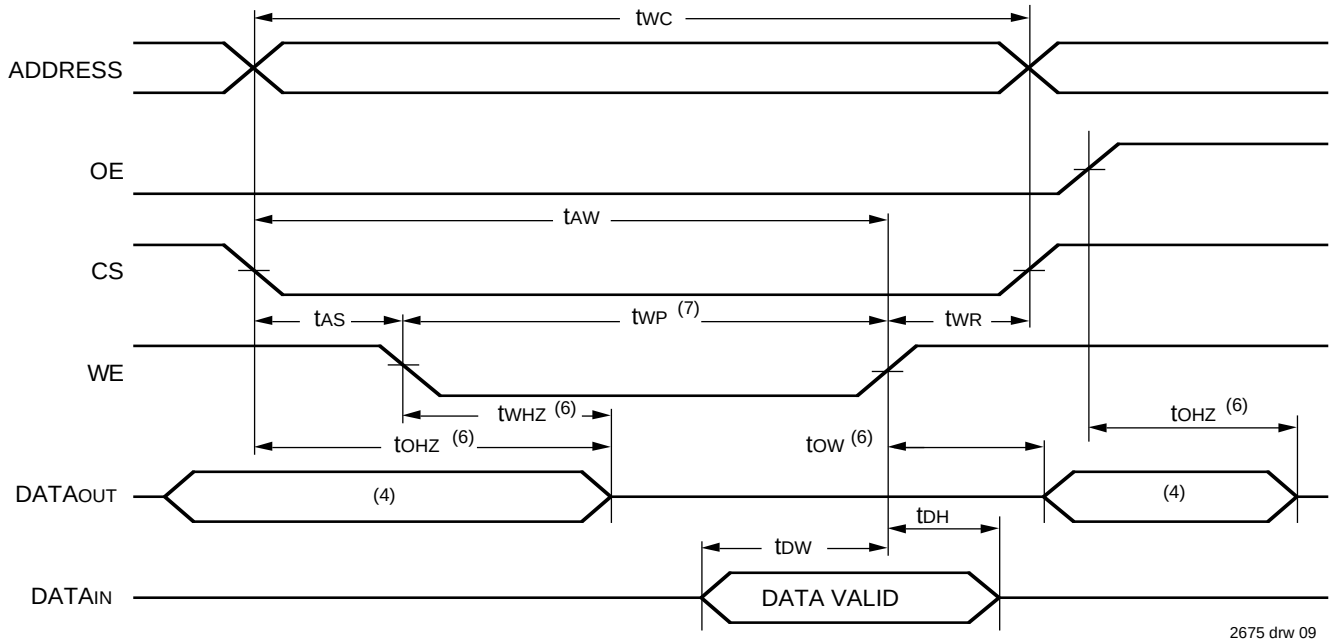
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



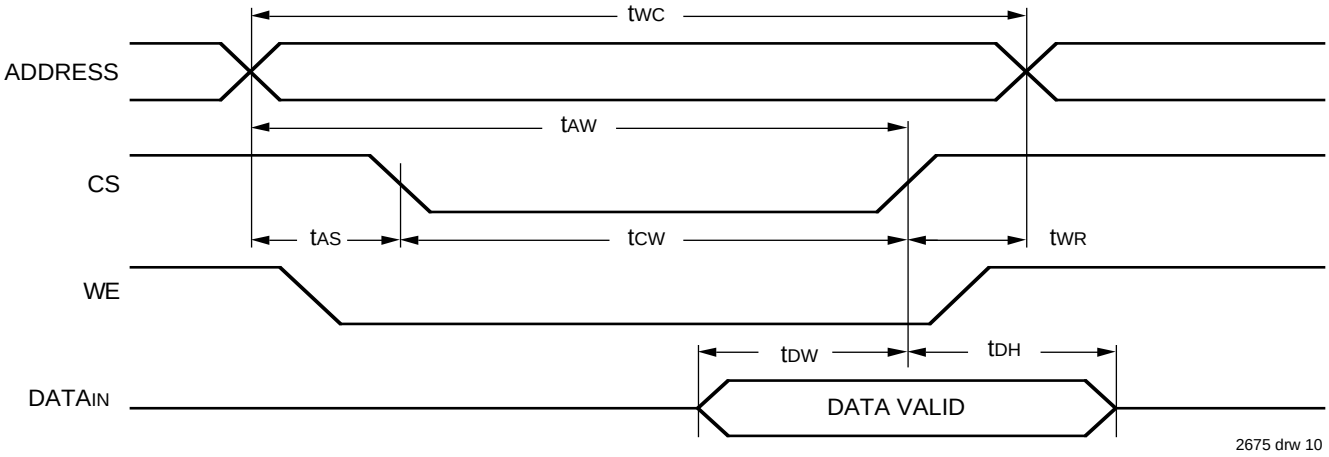
2675 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

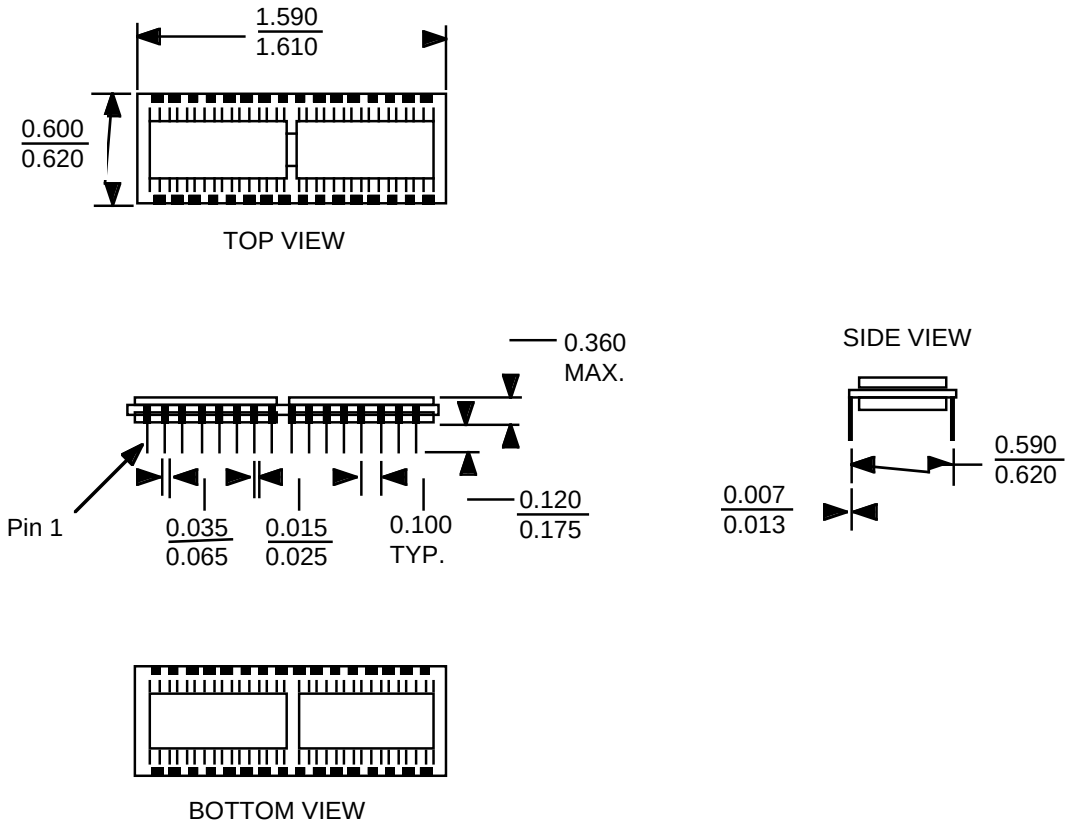


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

PACKAGE DIMENSIONS



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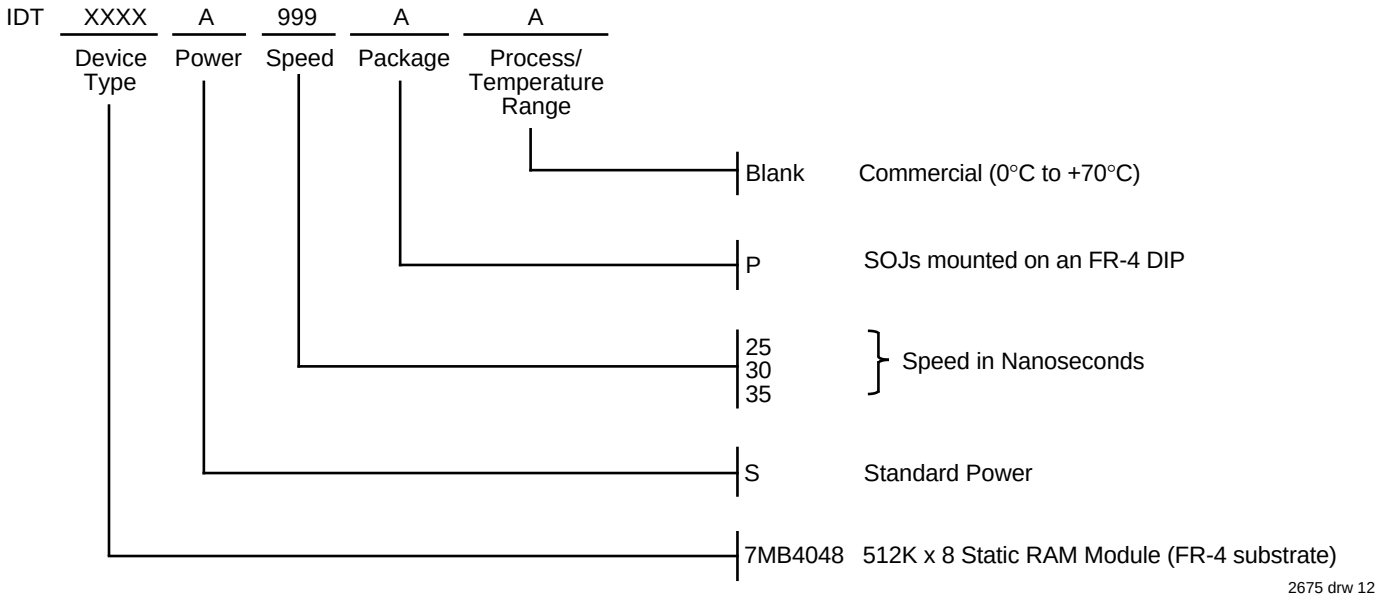
ORDERING INFORMATION(1)



2675 drw 12