Integrated Device Technology, Inc.

CMOS StaticRAM 16K (4K x 4-BIT) CACHE-TAG RAM

IDT6178S

FEATURES:

- High-speed Address to MATCH Valid time
  - Military: 12/15/20/25ns
  - Commercial: 10/12/15/20/25ns (max.)
- High-speed Address Access time
  - Military: 12/15/20/25ns
  - Commercial: 10/12/15/20/25ns (max.)
- Low-power consumption
  - IDT6178S

  Active: 300mW (typ.)
- Produced with advanced CMOS high-performance technology
- Input and output TTL-compatible
- Standard 22-pin Plastic or Ceramic DIP, 24-pin SOJ
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

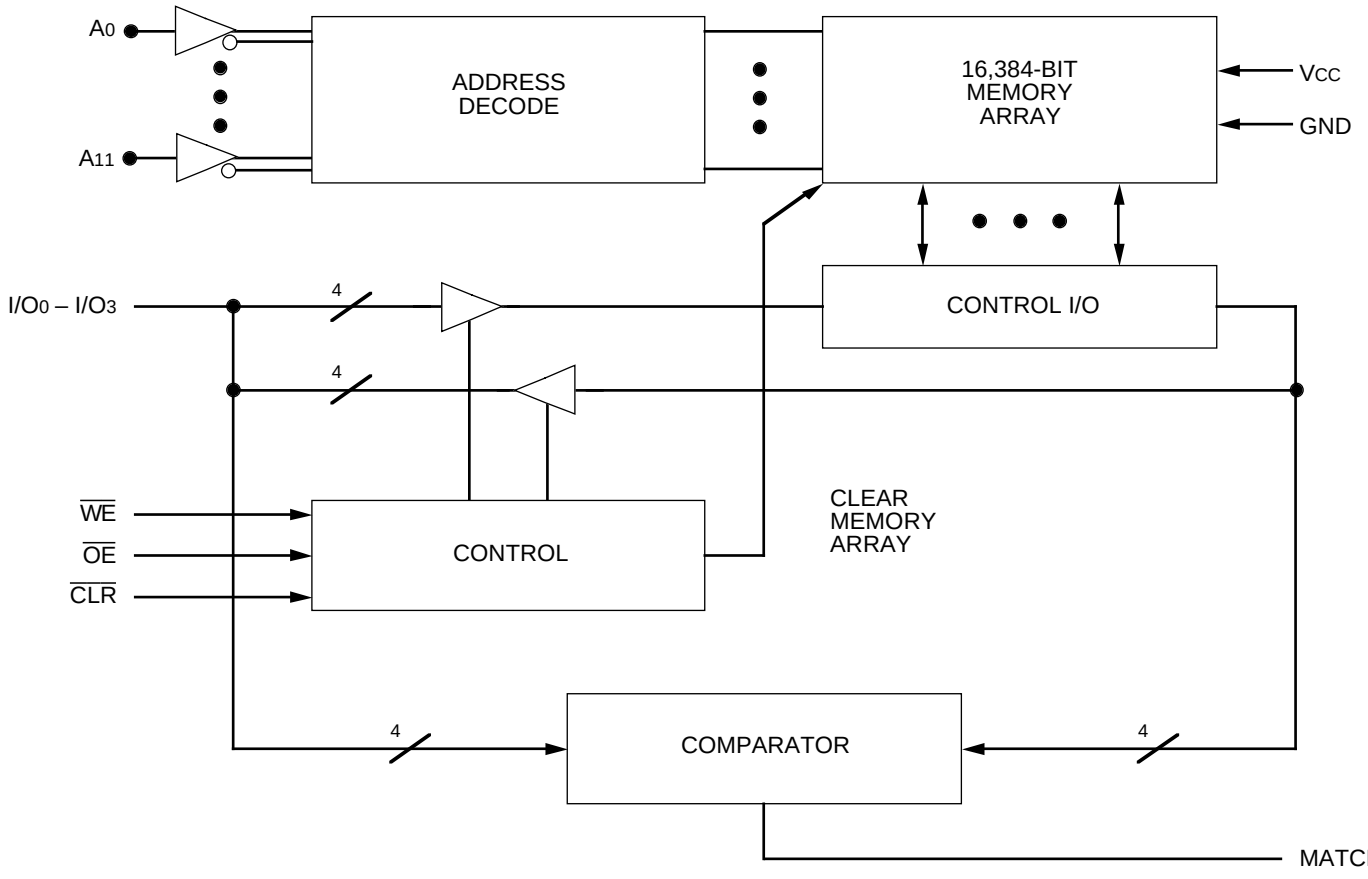
The IDT6178 is a high-speed cache address comparator sub-system consisting of a 16,384-bit StaticRAM organized as 4K x 4. Cycle Time and Address to MATCH Valid are equal. The IDT6178 features an onboard 4-bit comparator that compares RAM contents and current input data. The result is an active HIGH on the MATCH pin. The MATCH pins of several IDT6178s can be handed together to provide enabling or acknowledging signals to the data cache or processor.

The IDT6178 is fabricated using IDT's high-performance, high-reliability CMOS technology. Address to MATCH and Data to MATCH times are as fast as 10ns.

All inputs and outputs of the IDT6178 are TTL-compatible and the device operates from a single 5V supply.

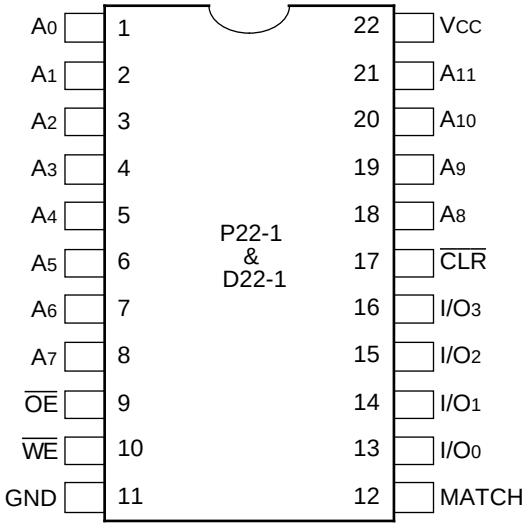
The IDT6178 is packaged in either a 22-pin, 300-mil Plastic or Ceramic DIP package or 24-pin SOJ. Military grade product is manufactured in compliance with latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



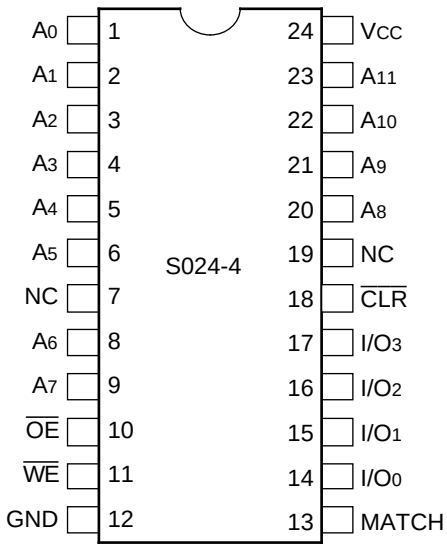
2953 drw 01

PIN CONFIGURATIONS



2953 drw 02

DIP
TOP VIEW



2953 drw 03

SOJ
TOP VIEW

PIN DESCRIPTIONS

A_0–A_{11}	Address Inputs
I/O_0–I/O_3	Data Input/Output
MATCH	Match
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
V_{CC}	Power
GND	Ground

2953 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	–55°C to +125°C	0V	5.0V ± 10%

2953 tbl 02

TRUTH TABLES(1)

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	Mode
H	H	H	Valid(2)	Match Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Clear Cycle

NOTE: 2953 tbl 03
1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. Valid Match = V_{OH}, Valid Non-Match = V_{OL}.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2953 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2(2)	–	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	–	0.8	V

NOTES: 2953 tbl 05
1. V_{IL} = –3.0V for pulse width less than 20ns, once per cycle.
2. V_{IH} = 2.5V for clear pin.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Symbol	Parameter	Condition	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2953 tbl 06
1. This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	Test Condition	6178S Min.	6178S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA (I/O_0 – I/O_3)	—	0.4	V
		I_{OL} = 10mA (I/O_0 – I/O_3)	—	0.5	V
		I_{OL} = 16mA (Match)	—	0.4	V
		I_{OL} = 20mA (Match)	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA (I/O_0 – I/O_3)	2.4	—	V
		I_{OH} = –8mA (Match)	2.4	—	V

2953 tbl 07

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter		6178S10 Max.	6178S12(1) Max.	6178S15(1) Max.	6178S20/25 Max.	Unit
I_{CC1}	Operating Power Supply Current	COM'L.	90	90	90	90	mA
	Outputs Open, V_{CC} = Max., f = 0(2)	MIL.	—	110	110	110	mA
I_{CC2}	Dynamic Operating Current	COM'L.	180	160	140	140	mA
	Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	MIL.	—	180	160	160	mA

NOTES:
1. Military values are preliminary only.
2. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs change.

2953 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 2 and 3
AC Test Load for Match Cycle	See Figure 1

2953 tbl 09

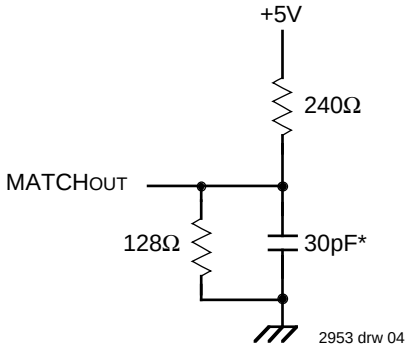


Figure 1. AC Test Load for MATCH

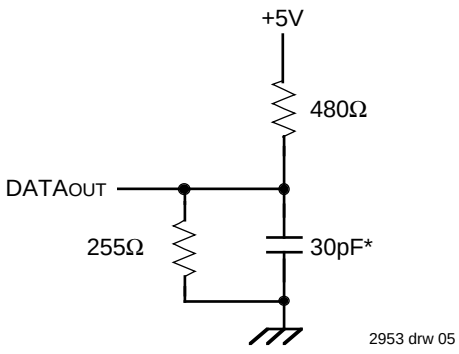


Figure 2. AC Test Load

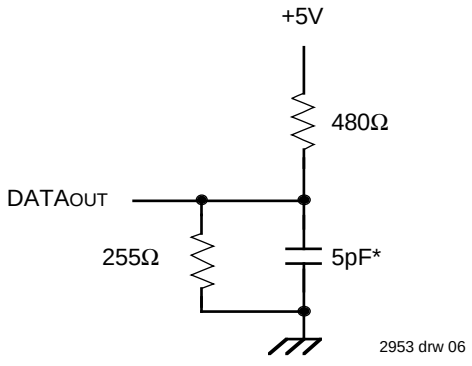


Figure 3. AC Test Load (for t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

* Including scope and jig.

CYCLE DESCRIPTION

Match Cycle: A match cycle occurs when all control signals ($\overline{OE}$, $\overline{WE}$, $\overline{CLR}$) are HIGH. At that time, data supplied to the RAM on the I/O pins is compared with the data stored at the specified address. The totem-pole match output is HIGH when there is a match at all data bits, and drives LOW if there is not a match.

Write Cycle: The write cycle is conventional, occuring when $\overline{WE}$ is LOW and $\overline{CLR}$ is HIGH. $\overline{OE}$ may be either HIGH or LOW, since it is overridden by $\overline{WE}$. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes HIGH during write cycles since the data at the specified address is the same as the data (being written) at the I/Os of the RAM.

Read Cycle: When $\overline{WE}$ and $\overline{CLR}$ are HIGH and $\overline{OE}$ is LOW, the RAM is in a read cycle. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes HIGH during read cycles since the data at the specified address is the same as the data (being read) at the I/Os of the RAM.

Clear Cycle: When $\overline{CLR}$ is asserted, every bit in the RAM is cleared to zero. If $\overline{OE}$ is LOW during a clear cycle, the RAM I/Os will be driven. However, this data is not necessarily zeros, even after a considerable time. The Match pin is enabled, but its state is not predicable.

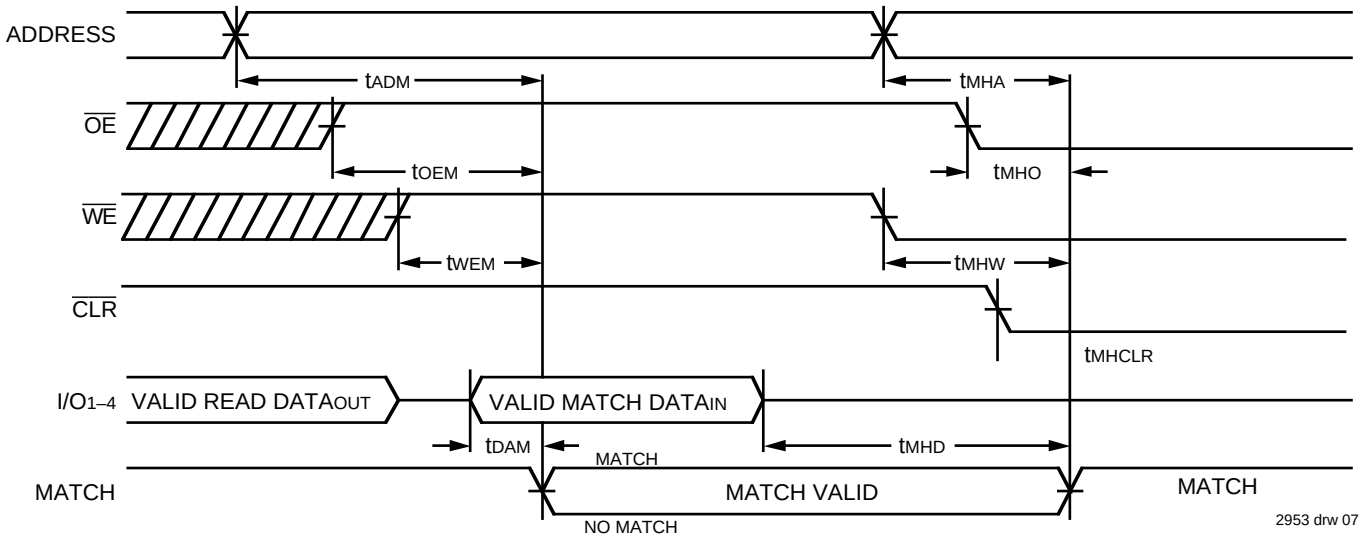
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10(1) Min.	6178S10(1) Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20 Min.	6178S20 Max.	6178S25 Min.	6178S25 Max.	Unit
Match Cycle												
t_{ADM}	Address to Match Valid	—	10	—	12	—	15	—	20	—	25	ns
t_{DAM}	Data Input to Match Valid	—	8	—	11	—	13	—	15	—	15	ns
t_{MHO}	Match Valid Hold from $\overline{OE}$	0	—	0	—	0	—	0	—	0	—	ns
t_{OEM}	$\overline{OE}$ HIGH to Match Valid	—	10	—	12	—	15	—	20	—	20	ns
t_{MHW}	Match Valid Hold from $\overline{WE}$	0	—	0	—	0	—	0	—	0	—	ns
t_{WEM}	$\overline{WE}$ HIGH to Match Valid	—	10	—	12	—	15	—	20	—	20	ns
t_{MHCLR}	Match Valid Hold from $\overline{CLR}$	0	—	0	—	0	—	0	—	0	—	ns
t_{MHA}	Match Valid Hold from Address	3	—	3	—	3	—	3	—	3	—	ns
t_{MHD}	Match Valid Hold from Data	3	—	3	—	3	—	3	—	3	—	ns

NOTE:
1. 0°C to +70°C temperature range only.

2953 tbl 10

TIMING WAVEFORM OF MATCH CYCLE(1)



2953 drw 07

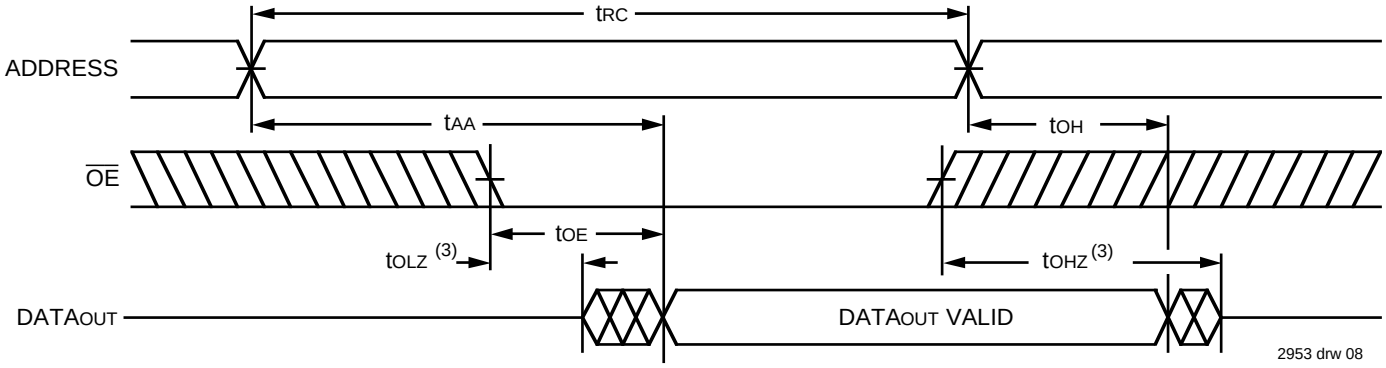
NOTE:
1. It is not recommended to let address and data input pins float while MATCH pin is active.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

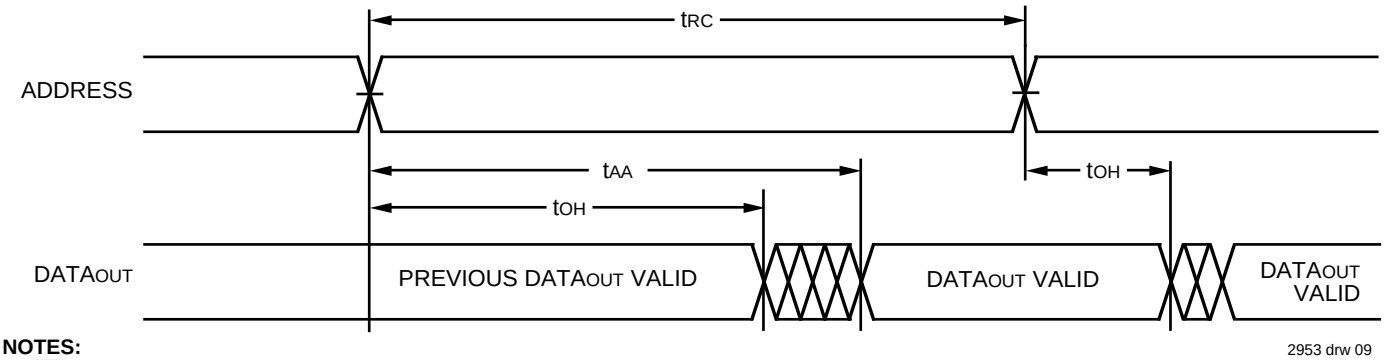
Symbol	Parameter	6178S10[1] Min.	6178S10[1] Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20/25 Min.	6178S20/25 Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20/25	ns
t_{OE}	Output Enable Access Time	—	7	—	8	—	10	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z Time	2	—	2	—	2	—	2	—	ns
t_{OHZ}[2]	Output Disable to Output in High-Z Time	—	6	—	7	—	9	—	12	ns

NOTES: 2953 tbl 11
1. 0°C to +70°C temperature range only.
2. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1,2]



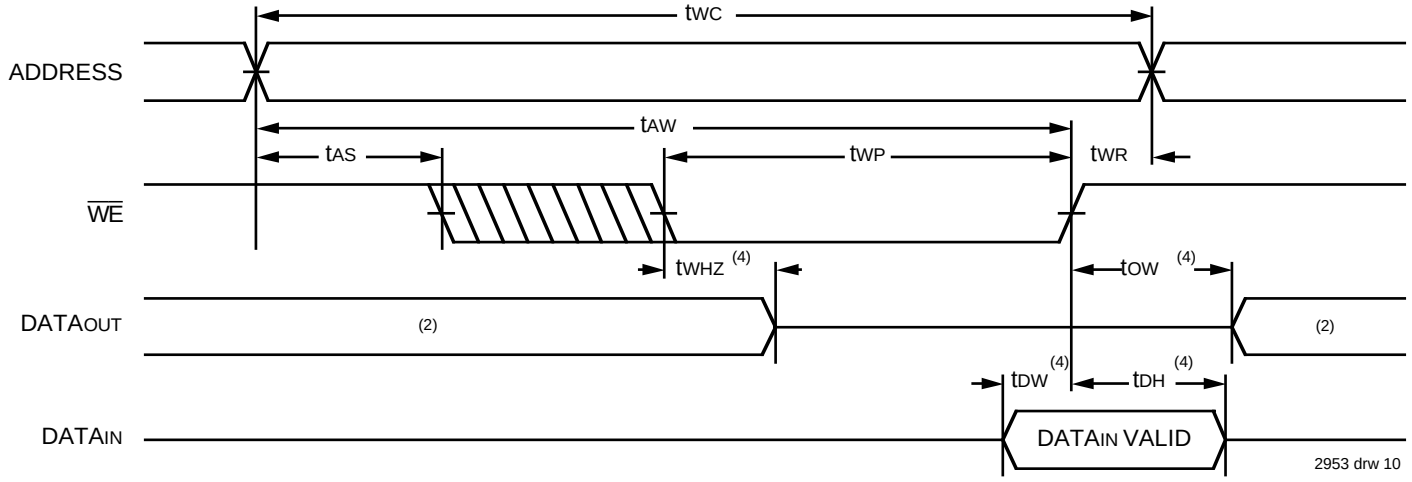
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Output enable is continuously active, $\overline{OE}$ is LOW.
3. Transition is measured ±200V from steady state.

AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10(1) Min.	6178S10(1) Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20/25 Min.	6178S20/25 Max.	Unit
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	8	—	10	—	12	—	14	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	10	—	12	—	14	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	6	—	8	—	10	—	12	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tWHZ(2)	Write Enable to Output in High-Z	—	5	—	6	—	7	—	9	ns
tOW(2)	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

NOTES:
2953 tbl 12
1. 0°C to +70°C temperature range only.
2. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE(1,3)



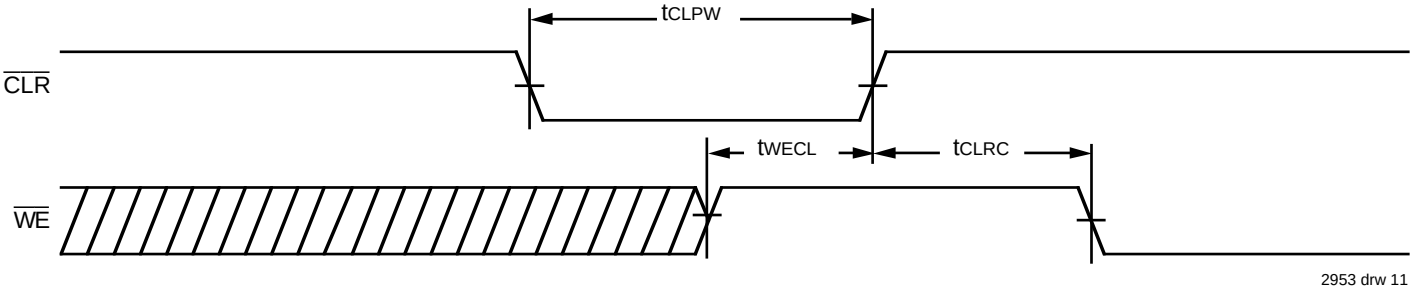
NOTES:
1. $\overline{WE}$ must be HIGH during all address transitions.
2. During this period, I/O pins are in the output state and the input signals must not be applied.
3. $\overline{OE}$ is HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified tWP.
4. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10(1) Min.	6178S10(1) Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20/25 Min.	6178S20/25 Max.	Unit
Clear Cycle										
tCLPW(2)	$\overline{CLR}$ Pulse Width	12	—	15	—	20	—	25	—	ns
tCLRC	$\overline{CLR}$ HIGH to $\overline{WE}$ LOW	5	—	5	—	5	—	5	—	ns
tPOCL(3)	Power on Reset	50	—	60	—	80	—	100	—	ns
tWECL	$\overline{WE}$ HIGH to Clear HIGH	5	—	5	—	5	—	5	—	ns

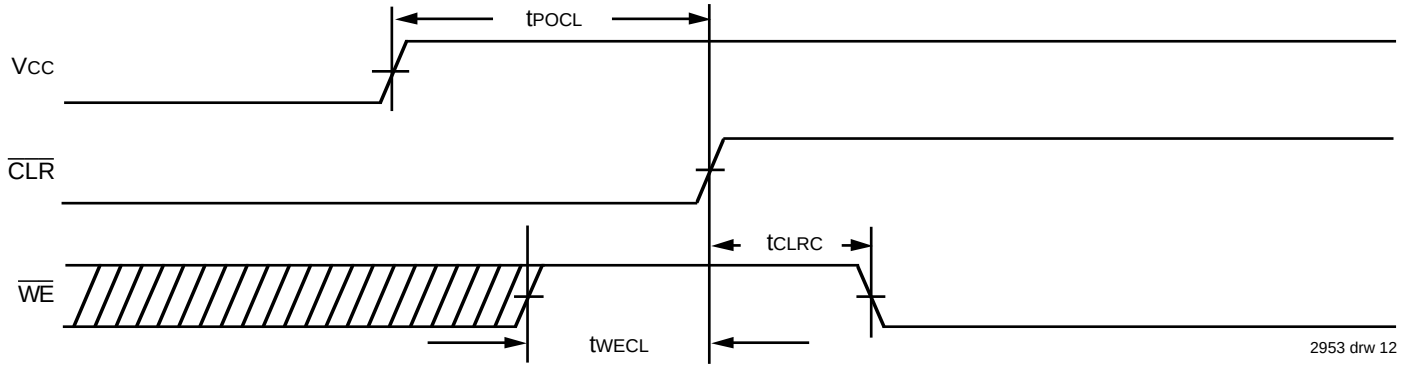
NOTES:
2953 tbl 13
1. 0°C to +70°C temperature range only.
2. Recommended duty cycle of 10% maximum.
3. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

TIMING WAVEFORM OF CLEAR CYCLE



2953 drw 11

POWER ON RESET TIMING



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ORDERING INFORMATION

IDT 6178 S XX X X

6178	S	XX	X	X
Device Type	Power	Speed	Package	Process/ Temperature

Process/Temperature:
- Blank — Commercial (0°C to +70°C)
- B — Military (–55°C to +125°C, Compliant to MIL-STD-883, Class B)

Package:
- P — 300 mil Plastic DIP (P22-1)
- Y — 300 mil Small Outline, J bend (SO24-4)
- D — 300 mil Ceramic DIP (D22-1)

Speed (Speed in nanoseconds):
- 10 — Commercial only
- 12
- 15
- 20
- 25

2953 drw 13