Integrated Device Technology, Inc.

# CMOS STATIC RAM 256K (64K x 4-BIT)

**IDT61298SA**

## FEATURES:

- 64K x 4 high-speed static RAM
- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- High speed (equal access and cycle times)
  — Commercial: 12/15 ns (max.)
- JEDEC standard pinout
- 300 mil 28-pin SOJ
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

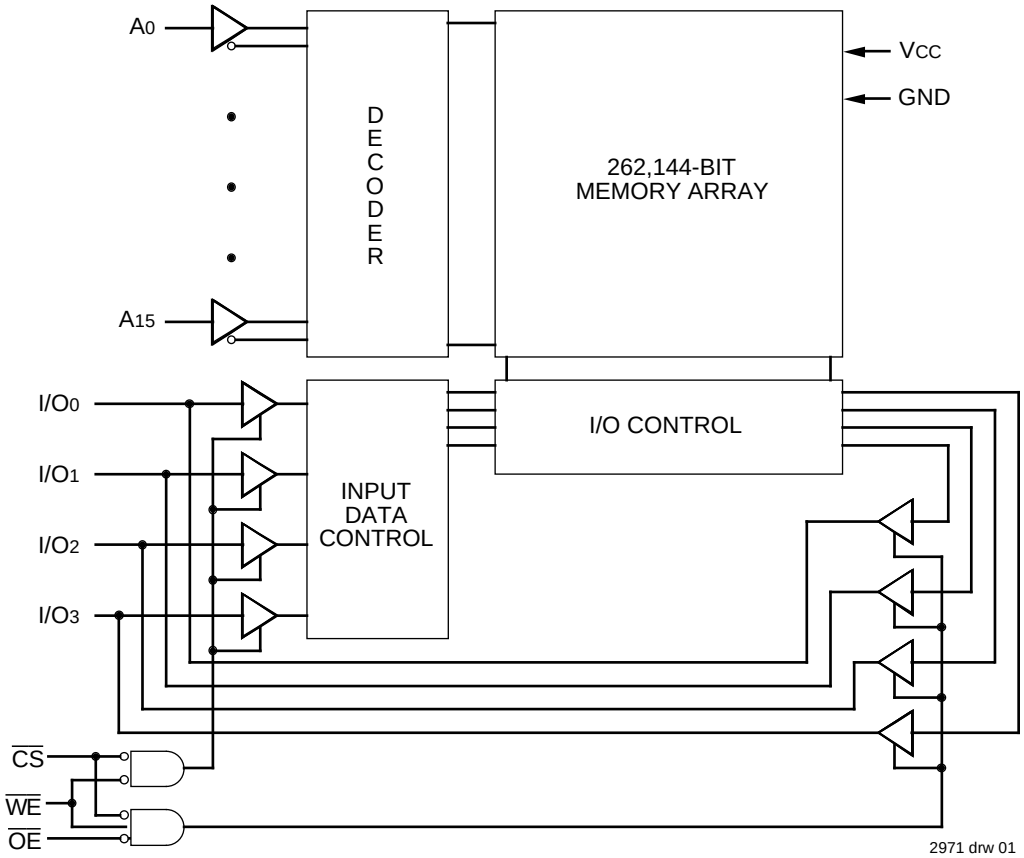
The IDT61298SA is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications.

The IDT61298SA features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61298SA's overall flexibility in high-speed memory applications.

Access times as fast as 12ns are available. The IDT61298SA offers a reduced power standby mode, $I_{SB1}$, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability.

All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous

## FUNCTIONAL BLOCK DIAGRAM

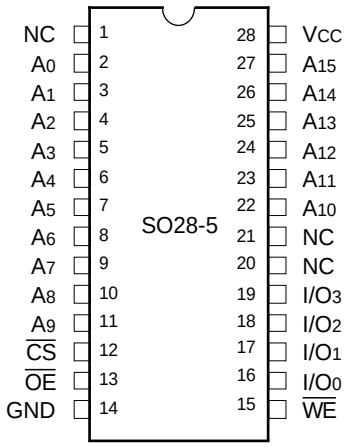


## DESCRIPTION (Continued)

circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT61298SA is packaged in a 300 mil, 28-pin SOJ, providing improved board-level packing densities.

## PIN CONFIGURATION




2971 drw 02

**SOJ**
**TOP VIEW**

## PIN DESCRIPTIONS

| Name | Description |
|---|---|
| $A_0$–$A_{14}$ | Addresses |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $\overline{CS}$ | Chip Select |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| GND | Ground |
| $V_{CC}$ | Power |

2971 tbl 04

## TRUTH TABLE(1,2)

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | I/O | Function |
|---|---|---|---|---|
| L | L | H | $DATA_{OUT}$ | Read Data |
| L | X | L | $DATA_{IN}$ | Write Data |
| L | H | H | High-Z | Outputs Disabled |
| H | X | X | High-Z | Deselected - Standby ($I_{SB}$) |
| $V_{HC}$(3) | X | X | High-Z | Deselected - Standby ($I_{SB1}$) |

**NOTES:** 2971 tbl 01

1. H = $V_{IH}$, L = $V_{IL}$, x = Don't care.
2. $V_{LC}$ = 0.2V, $V_{HC}$ = $V_{CC}$ -0.2V.
3. Other inputs ≥$V_{HC}$ or ≤$V_{LC}$.

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Com'l. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

**NOTES:** 2971 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{TERM}$ must not exceed $V_{CC}$ + 0.5V.

## CAPACITANCE

($T_A$ = +25°C, f = 1.0MHz, SOJ Package)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 5 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 3dV | 7 | pF |

**NOTE:** 2971 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Temperature | GND | Vcc |
|---|---|---|---|
| Commercial | 0°C to +70°C | 0V | 5V ± 10% |

2971 tbl 05

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | $V_{CC}$ + 0.5V | V |
| $V_{IL}$ | Input Low Voltage | –0.5(1) | — | 0.8 | V |

**NOTE:** 2971 tbl 06
1. $V_{IL}$ (min.) = –1.5V for pulse width less than 10ns, once per cycle.

## DC ELECTRICAL CHARACTERISTICS(1)

($V_{CC}$ = 5V ± 10%, $V_{LC}$ = 0.2V, $V_{HC}$ = $V_{CC}$ - 0.2V)

| Symbol | Parameter | 61298SA12 | | 61298SA15 | | Unit |
|---|---|---|---|---|---|---|
| | | Com'l. | Mil. | Com'l. | Mil. | |
| $I_{CC}$ | Dynamic Operating Current $\overline{CS}$ = $V_{IL}$, Outputs Open $V_{CC}$ = Max., f = $f_{MAX}$(2) | 160 | — | 140 | — | mA |
| $I_{SB}$ | Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ $V_{IH}$, $V_{CC}$ = Max., Outputs Open, f = $f_{MAX}$(2) | 50 | — | 45 | — | mA |
| $I_{SB1}$ | Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ $V_{HC}$, $V_{CC}$ = Max., f = 0(2), $V_{LC}$ ≥ $V_{IN}$ ≥ $V_{HC}$ | 20 | — | 20 | — | mA |

**NOTES:** 2971 tbl 07
1. All values are maximum guaranteed values.
2. $f_{MAX}$ = 1/$t_{RC}$ (all address inputs are cycling at $f_{MAX}$); f = 0 means no address input lines are changing.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

2971 tbl 08

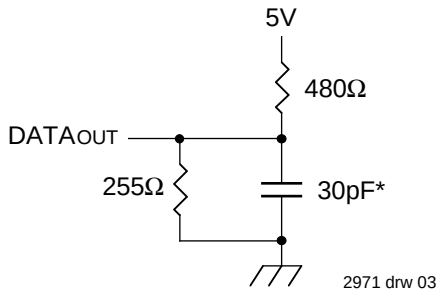



**Figure 1. AC Test Load**

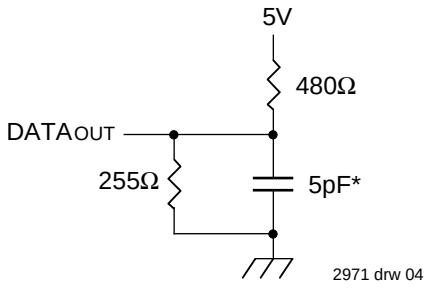



**Figure 2. AC Test Load (for $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{OW}$, $t_{WHZ}$)**

*Includes scope and jig capacitances

## DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Condition | IDT61298SA Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = Max.,<br>$V_{IN}$ = GND to $V_{CC}$ | —<br> | —<br> | 5<br> | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IH}$,<br>$V_{OUT}$ = GND to $V_{CC}$ | —<br> | —<br> | 5<br> | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA, $V_{CC}$ = Min.<br>$I_{OL}$ = 10mA, $V_{CC}$ = Min. | —<br>— | —<br>— | 0.4<br>0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –4mA, $V_{CC}$ = Min. | 2.4 | — | — | V |

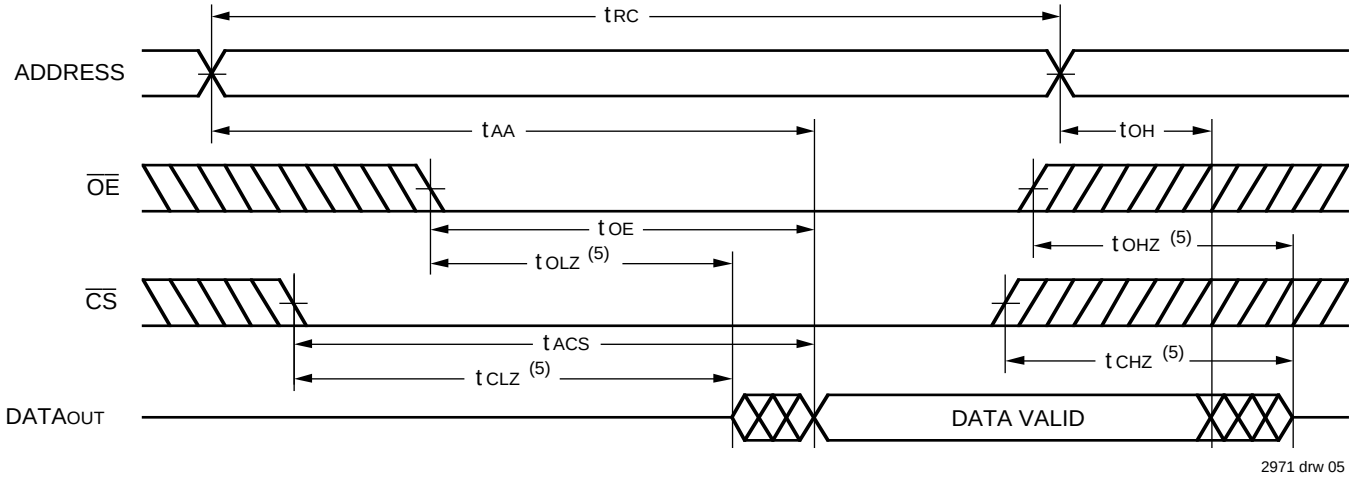
2971 tbl 09

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0V ± 10%)

| Symbol | Parameter | 61298SA12 Min. | 61298SA12 Max. | 61298SA15 Min. | 61298SA15 Max. | Unit |
|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 12 | — | 15 | — | ns |
| $t_{AA}$ | Address Access Time | — | 12 | — | 15 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 12 | — | 15 | ns |
| $t_{CLZ}$(1) | Chip Select to Output in Low-Z | 4 | — | 4 | — | ns |
| $t_{CHZ}$(1) | Chip Deselect to Output in High-Z | — | 6 | — | 7 | ns |
| $t_{OE}$ | Output Enable to Output Valid | — | 6 | — | 7 | ns |
| $t_{OLZ}$(1) | Output Enable to Output in Low-Z | 0 | — | 0 | — | ns |
| $t_{OHZ}$(1) | Output Disable to Output in High-Z | — | 6 | — | 6 | ns |
| $t_{OH}$ | Output Hold from Address Change | 3 | — | 3 | — | ns |
| $t_{PU}$(1) | Chip Select to Power-Up Time | 0 | — | 0 | — | ns |
| $t_{PD}$(1) | Chip Deselect to Power-Down Time | — | 12 | — | 15 | ns |
| **Write Cycle** | | | | | | |
| $t_{WC}$ | Write Cycle Time | 12 | — | 15 | — | ns |
| $t_{CW}$ | Chip Select to End-of-Write | 9 | — | 10 | — | ns |
| $t_{AW}$ | Address Valid to End-of-Write | 9 | — | 10 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 9 | — | 10 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | ns |
| $t_{DW}$ | Data Valid to End-of-Write | 6 | — | 7 | — | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | ns |
| $t_{WHZ}$(1) | Write Enable to Output in High-Z | — | 6 | — | 6 | ns |
| $t_{OW}$(1) | Output Active from End-of-Write | 4 | — | 4 | — | ns |

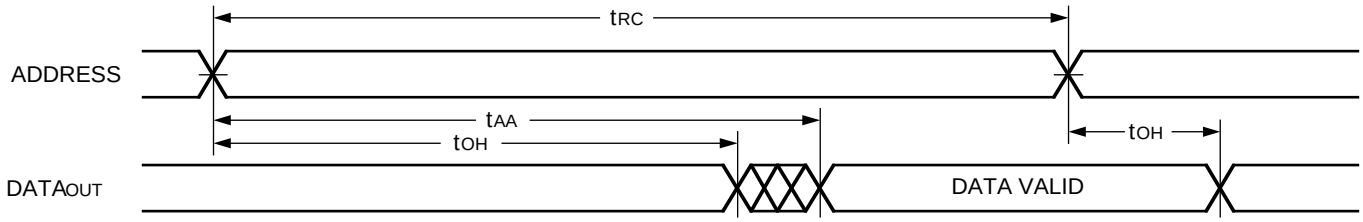
NOTES: 2971 tbl 10
1. This parameter is guaranteed with AC test load (Figure 2) by device characterization, but is not production tested.

## TIMING WAVEFORM OF READ CYCLE NO. 1(1)



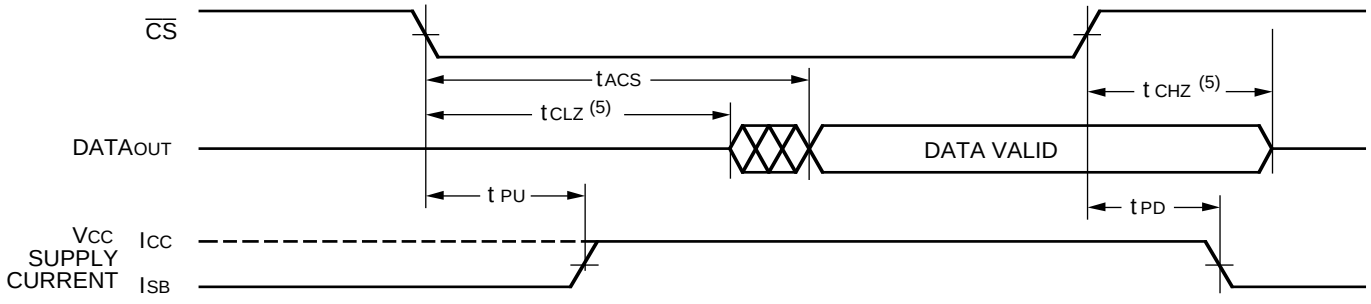

2971 drw 05

## TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)




2971 drw 06

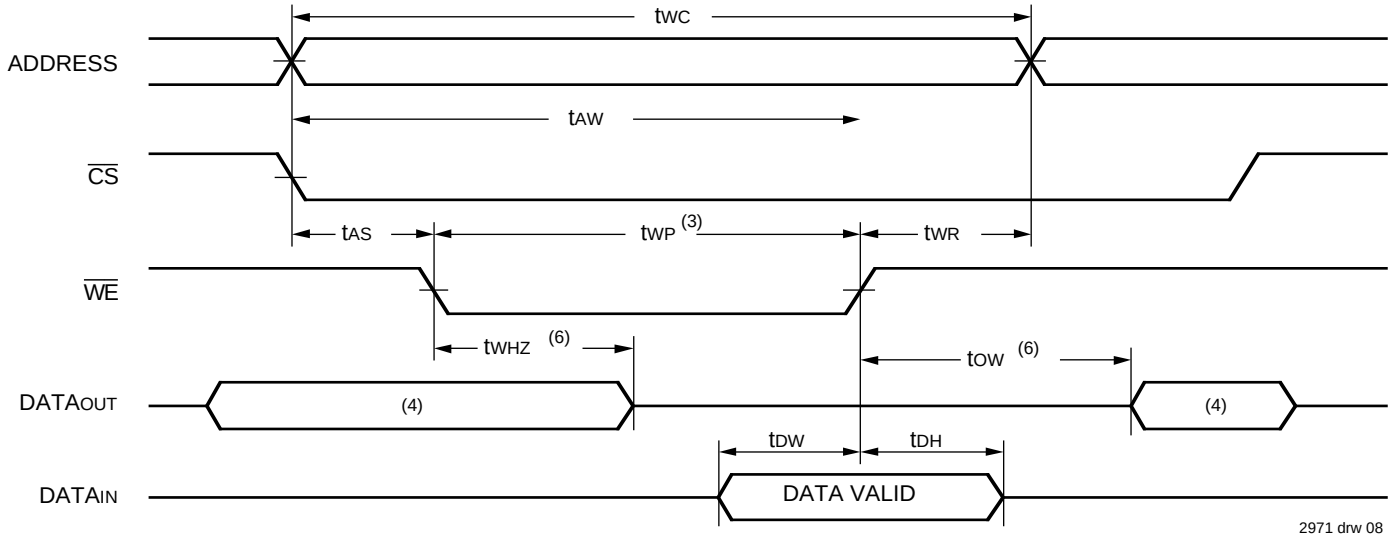
## TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



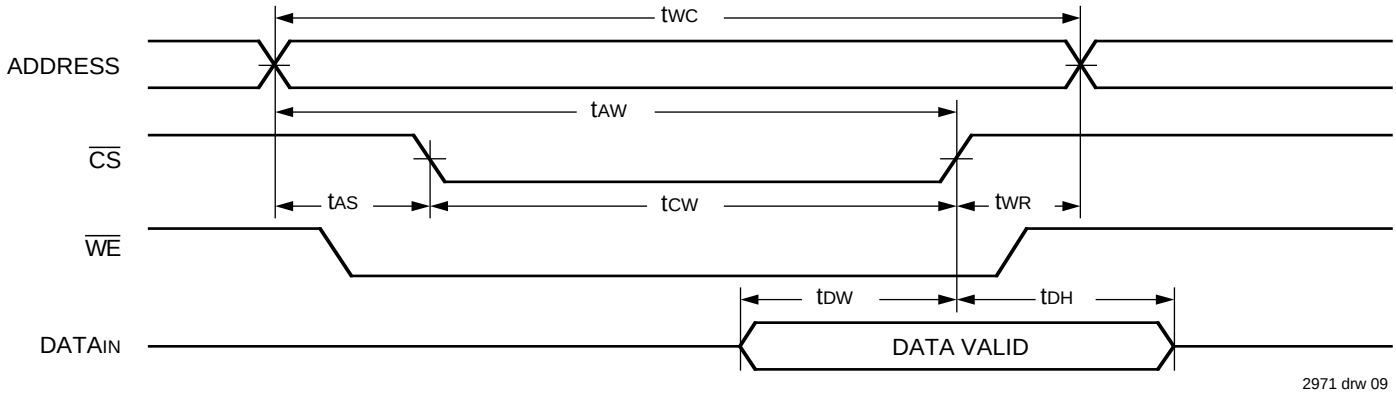

2971 drw 07

**NOTES:**
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)




## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)




**NOTES:**
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified $t_{WP}$.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

## ORDERING INFORMATION