Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

IDT71B74

FEATURES:

- High-speed address to MATCH comparison time
  - — Commercial: 8/10/12/15/20ns (max.)
- High-speed address access time
  - — Commercial: 8/10/12/15/20ns (max.)
- High-speed chip select access time
  - — Commercial: 6/7/8/10ns (max.)
- Power-ON Reset Capability
- Low power consumption
  - — 830mW (typ.) for 12ns parts
  - — 880mW (typ.) for 10ns parts
  - — 920mW (typ.) for 8ns parts
- Produced with advanced BiCMOS high-performance technology
- Input and output directly TTL-compatible
- Standard 28-pin plastic DIP and 28-pin SOJ (300 mil)

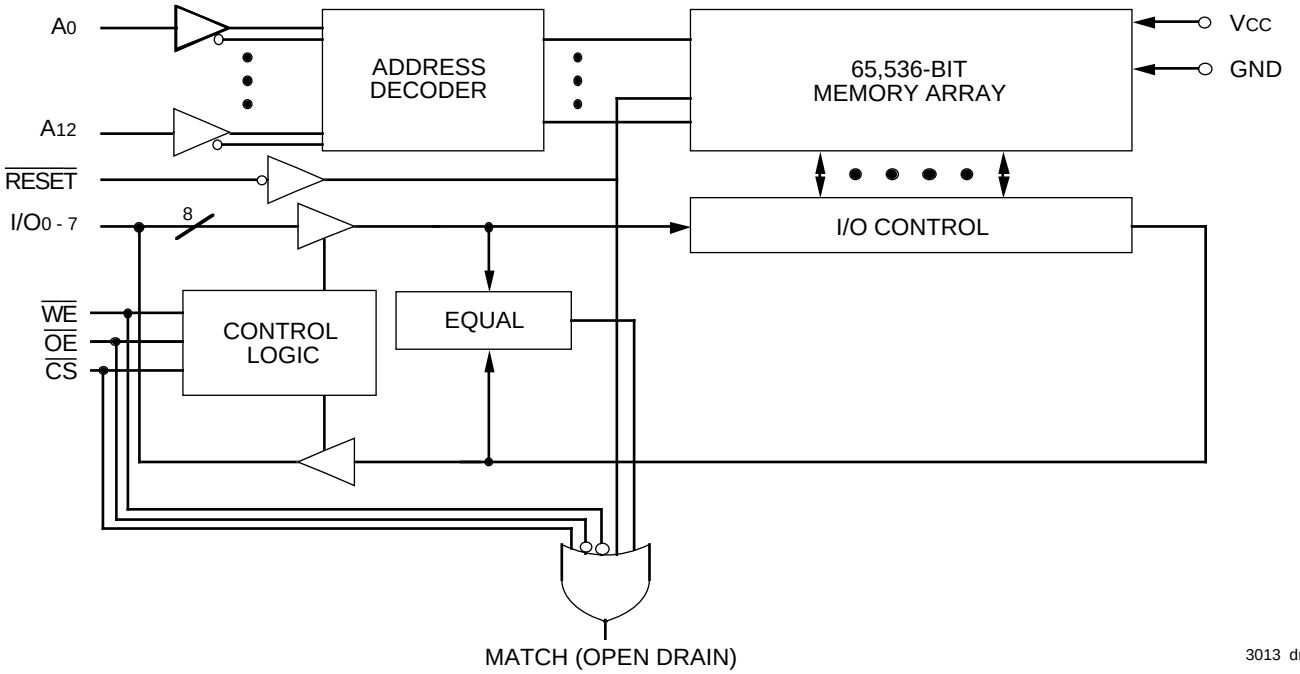
DESCRIPTION:

The IDT71B74 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT71B74 can map 8K cache words into a 2 megabyte address space by using the 21 bits of address organized with the 13 LSBs for the cache address bits and the 8 higher bits for cache data bits. Two IDT71B74s can be combined to provide 29 bits of address comparison, etc. The IDT71B74 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B74 can also be used as a resettable 8K x 8 high-speed static RAM.

The IDT71B74 is fabricated using IDT's high-performance, high-reliability BiCMOS technology. Address access times as fast as 8ns, chip select times of 6ns and address-to-match times of 8ns are available.

The MATCH pin of several IDT71B74s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput.

FUNCTIONAL BLOCK DIAGRAM



3013 drw 01

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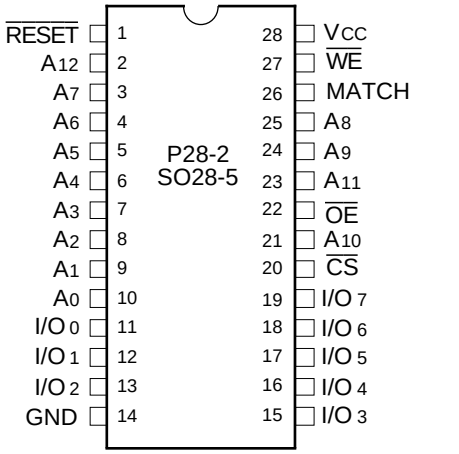
PIN CONFIGURATION



3013 drw 02

DIP/SOJ
TOP VIEW

TRUTH TABLE(1, 2)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	$\overline{RESET}$	MATCH	I/O	Function
X	X	X	L	HIGH	—	Reset all bits to LOW
X	H	X	H	HIGH	Hi-Z	Deselect chip
H	L	H	H	LOW	D_{IN}	No MATCH
H	L	H	H	HIGH	D_{IN}	MATCH
H	L	L	H	HIGH	D_{OUT}	Read
L	L	X	H	HIGH	D_{IN}	Write

NOTES: 3013 tbl 01
1. H = V_{IH}, L = V_{IL}, X = DON'T CARE
2. HIGH = High-Z (pulled up by an external resistor), and LOW = V_{OL}.

PIN DESCRIPTIONS

Pin Names	Description
$A_{0–12}$	Address
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{RESET}$	Memory Reset
MATCH	Data/Memory Match (Open Drain)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

3013 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3013 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ Package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3013 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage(1)	2.2	—	6.0(4)	V
V_{IHR}	$\overline{RESET}$ Input Voltage	2.5(2)	—	6.0	V
V_{IL}	Input LOW Voltage	–0.5(3)	—	0.8	V

3013 tbl 05

NOTES:
1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ–10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.
4. V_{TERM} must not exceed V_{CC} + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

3013 tbl 06

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter		71B74S8	71B74S10	71B74S12	71B74S15	71B74S20	Unit
I_{CC}	Dynamic Operating Current	$\overline{WE}$ = V_{LC}	230	210	200	190	180	mA
	Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	$\overline{WE}$ = V_{HC}	210	200	170	160	150	mA

3013 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only input addresses are cycling at f_{MAX}.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

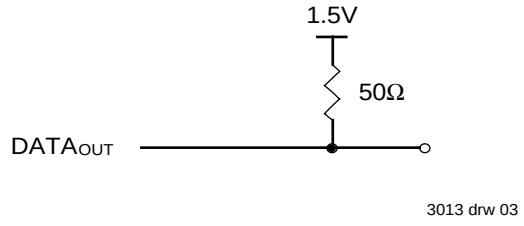
Symbol	Parameter	Test Condition	IDT71B74S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 22mA MATCH	—	0.5	V
		I_{OL} = 18mA MATCH	—	0.4	
		I_{OL} = 10mA, V_{CC} = Min. (Except MATCH)	—	0.5	
		I_{OL} = 8mA, V_{CC} = Min. (Except MATCH)	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min. (Except MATCH)	2.4	—	V

3013 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

3013 tbl 09



3013 drw 03

Figure 1. AC Test Load

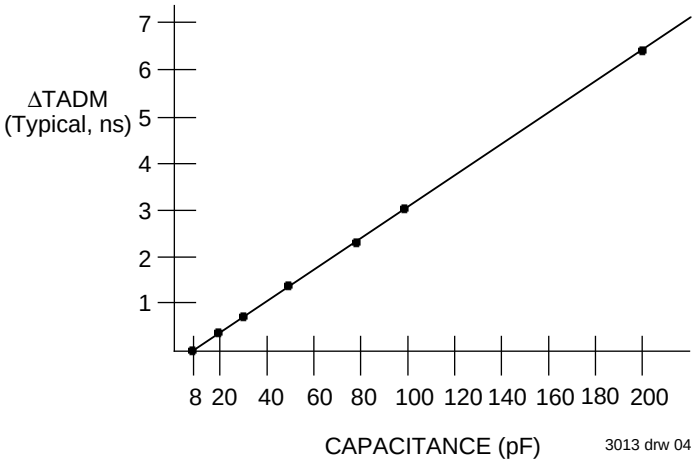
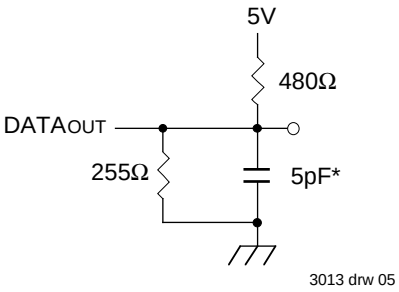


Figure 1A. Lumped Capacitive Load Typical Derating Curve



*Includes scope and jig.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

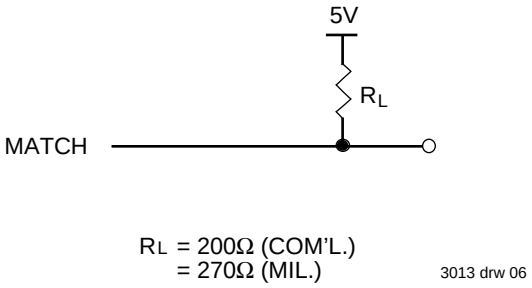


Figure 3. AC Test Load for MATCH

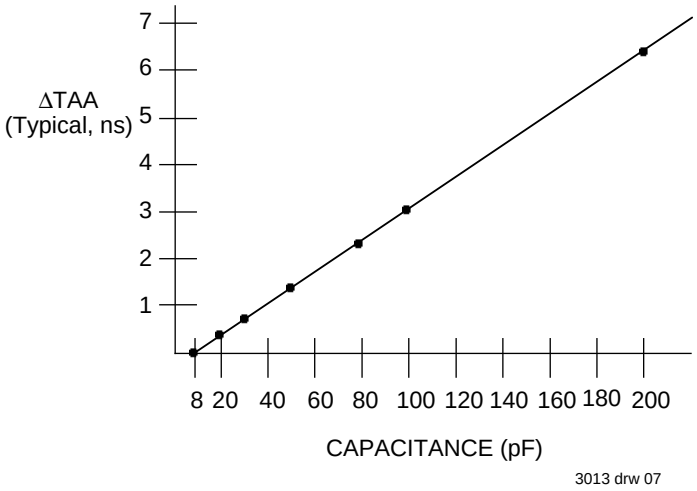
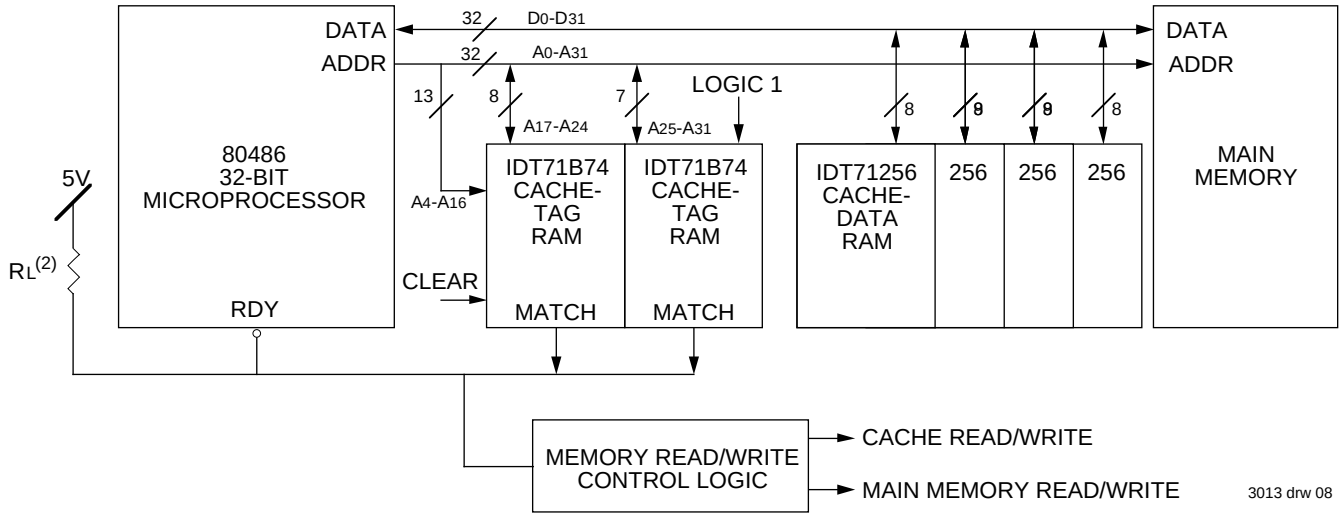


Figure 3A. Lumped Capacitive Load Typical Derating Curve



NOTES:
1. For more information refer to IDT Application Notes AN-07 and AN-78 and Technical Notes TN-11 and TN-13.
2. $R_L = 200\Omega$.

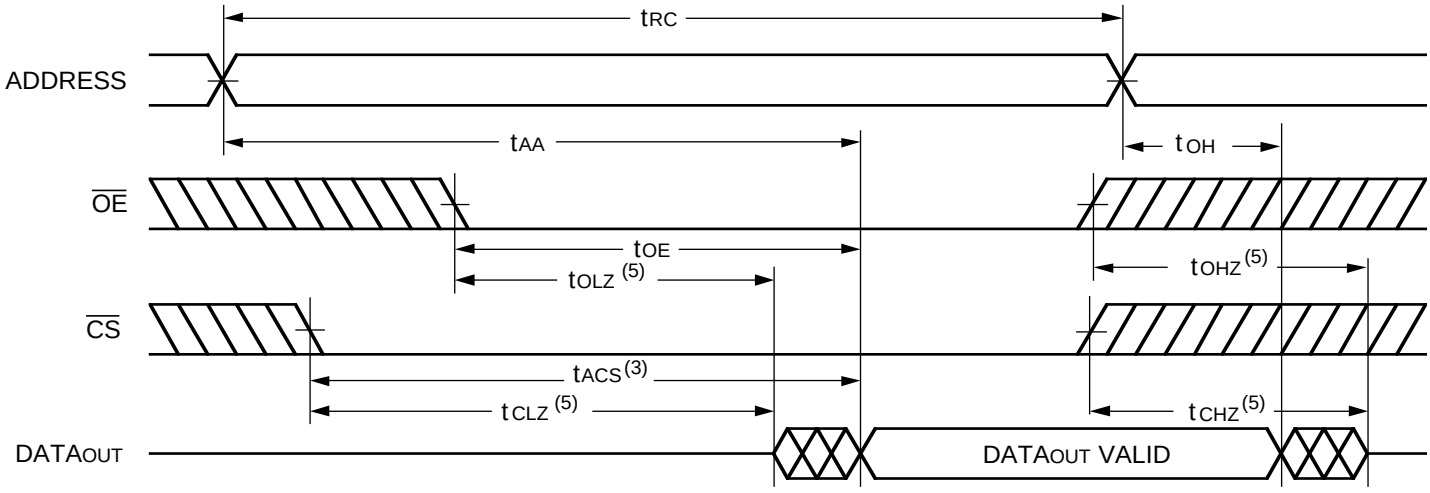
Figure 4. Example of Cache Memory System Block Diagram

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	6	—	7	—	8	—	8	—	10	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	2	—	2	—	2	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	6	—	8	—	9	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	ns
t_{CHZ}(1)	Chip Select to Output in High-Z	—	4	—	5	—	5	—	7	—	8	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	4	—	4	—	5	—	5	—	8	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns

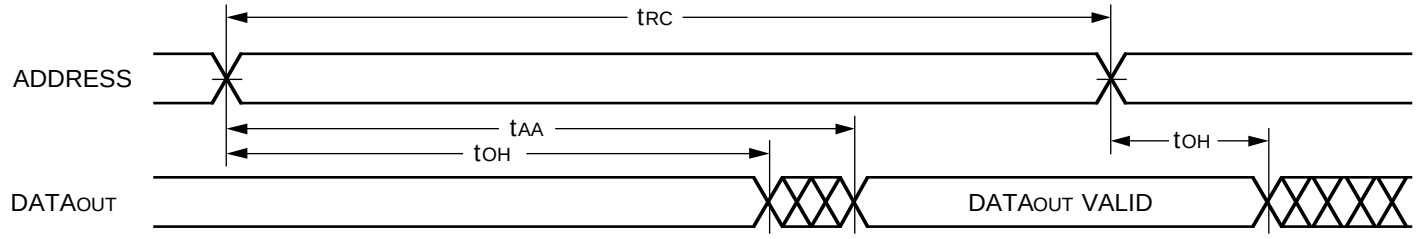
NOTE: 3013 tbl 10
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



3013 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



NOTES: 3013 drw 10
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is continuously active, $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

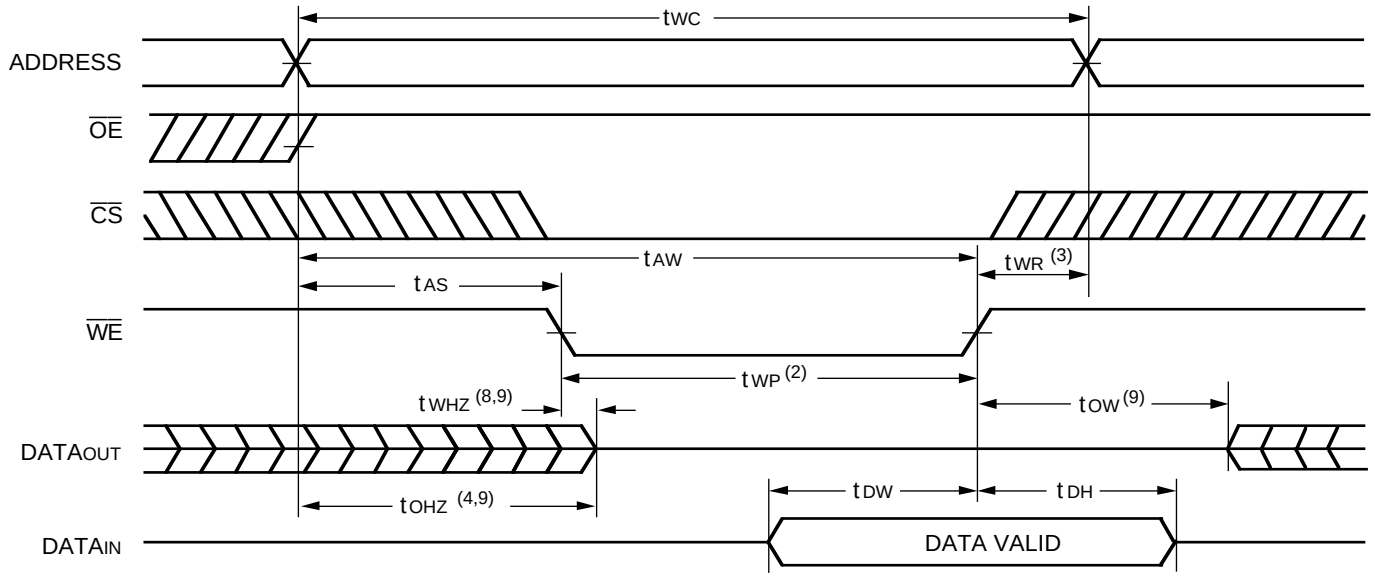
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
t_{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
t_{CW}	Chip Select to End of Write	7	—	8	—	9	—	10	—	15	—	ns
t_{AW}	Address Valid to End of Write	7	—	8	—	9	—	10	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	9	—	10	—	15	—	ns
t_{WR}	Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	5	—	5	—	5	—	5	—	5	ns
t_{DW}	Data Valid to End of Write	5	—	5	—	6	—	8	—	10	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	2	—	2	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

3013 tbl 11

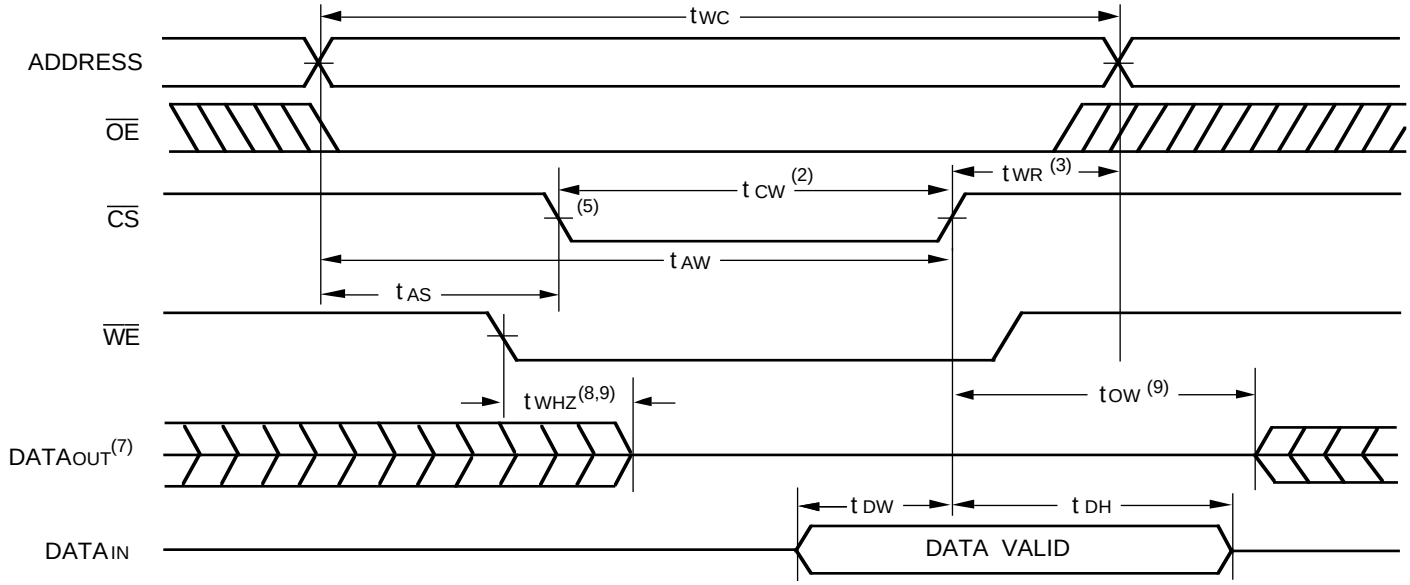
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled Timing, $\overline{OE}$ HIGH During Write)[1, 6]



3013 drw 11

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{WE}$ and a LOW $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{OE}$ is continuously HIGH, $\overline{OE} \geq V_{IH}$. If during the $\overline{WE}$ controlled write cycle the $\overline{OE}$ is LOW, t_{WP} must be greater or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and the data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during the $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW} timing.
7. $DATA_{OUT}$ is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. t_{WHZ} is not included if $\overline{OE}$ remains HIGH during the write cycle. If $\overline{OE}$ is LOW during the Write Enabled write cycle then t_{WHZ} must be added to t_{WP} and t_{CW}.
9. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled Timing)(1, 6)



3013 drw 12

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{WE}$ and a LOW $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{OE}$ is continuously HIGH, $\overline{OE} \geq V_{IH}$. If during the $\overline{WE}$ controlled write cycle the $\overline{OE}$ is LOW, t_{WP} must be greater or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and the data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during the $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW} timing.
7. $DATA_{OUT}$ is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. t_{WHZ} is not included if $\overline{OE}$ remains HIGH during the write cycle. If $\overline{OE}$ is LOW during the Write Enabled write cycle then t_{WHZ} must be added to t_{WP} and t_{CW}.
9. Transition is measured ±200mV from steady state.

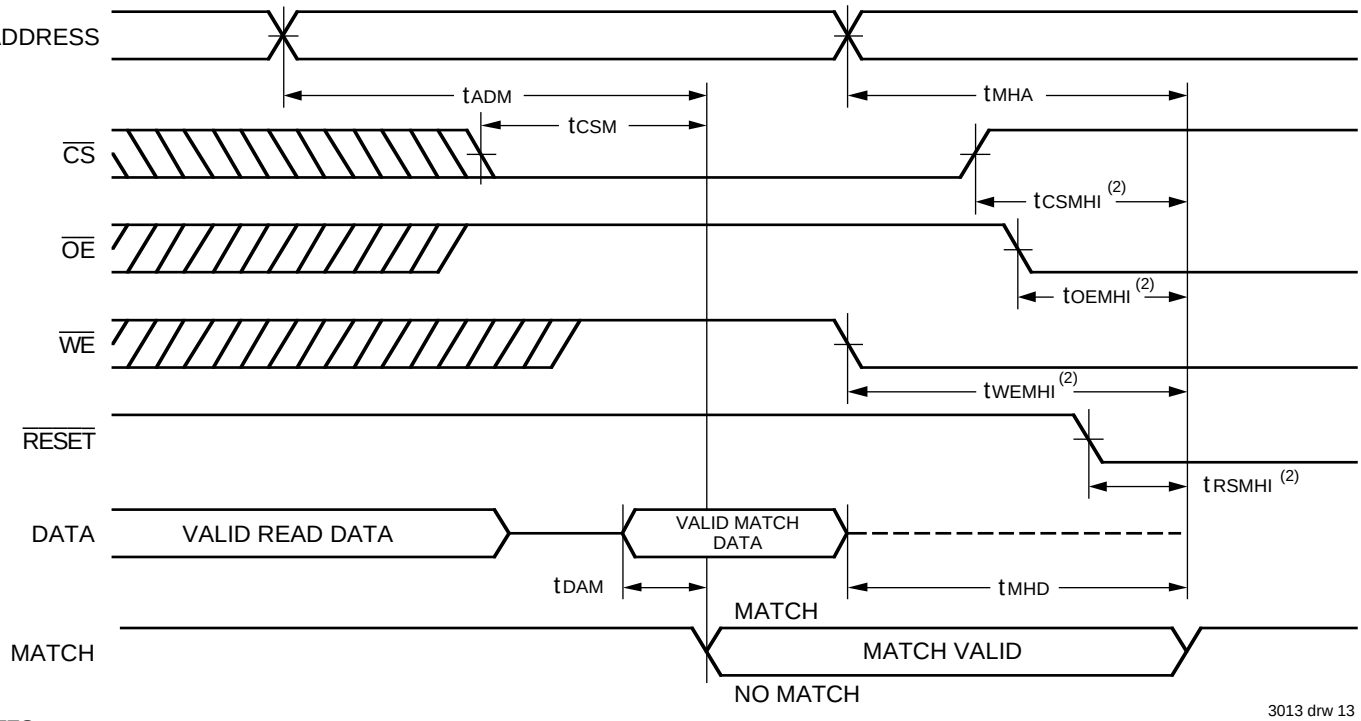
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Match Cycle												
t_{ADM}	Address to MATCH Valid	—	8	—	10	—	12	—	15	—	20	ns
t_{CSM}	Chip Select to MATCH Valid	—	7	—	7	—	8	—	10	—	10	ns
t_{CSMHI}(1)	Chip Select to MATCH HIGH	—	7	—	8	—	8	—	8	—	8	ns
t_{DAM}	Data Input to MATCH Valid	—	7	—	8	—	10	—	12	—	12	ns
t_{OEMHI}(1)	$\overline{OE}$ LOW to MATCH HIGH	—	7	—	8	—	10	—	10	—	10	ns
t_{WEMHI}(1)	$\overline{WE}$ LOW to MATCH HIGH	—	7	—	8	—	10	—	10	—	10	ns
t_{RSMHI}(1)	$\overline{RESET}$ LOW to MATCH HIGH	—	8	—	10	—	10	—	12	—	15	ns
t_{MHA}	MATCH Valid Hold From Address	2	—	2	—	2	—	2	—	2	—	ns
t_{MHD}	MATCH Valid Hold From Data	2	—	2	—	2	—	2	—	2	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3013 tbl 12

MATCH TIMING(1)



3013 drw 13

NOTES:
1. It is not recommended to float data and address input pins while the MATCH pin is active.
2. Transition is measured at ±200mV from steady state.

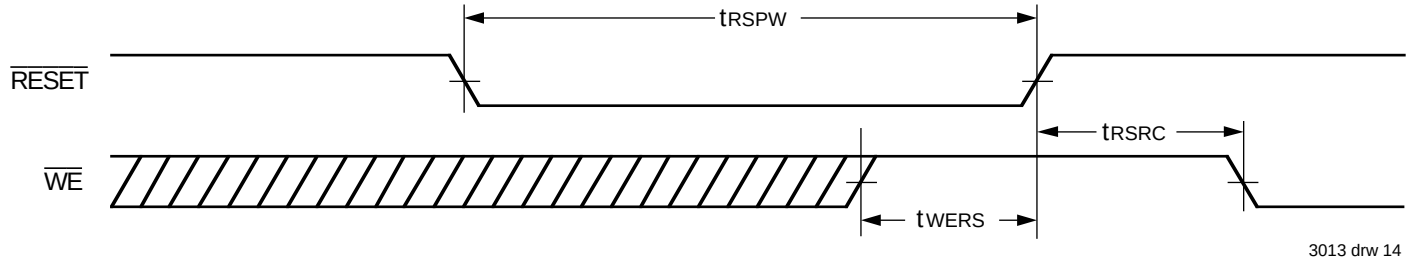
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B74S8		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle												
t_{RSPW}(1)	Reset Pulse Width	30	—	35	—	35	—	40	—	45	—	ns
t_{WERS}	$\overline{WE}$ HIGH to Reset HIGH	5	—	5	—	5	—	5	—	5	—	ns
t_{RSRC}	Reset HIGH to $\overline{WE}$ LOW	25	—	25	—	25	—	30	—	30	—	ns
t_{PORS}(2)	Power On Reset	100	—	100	—	100	—	120	—	120	—	ns

3013 tbl 13

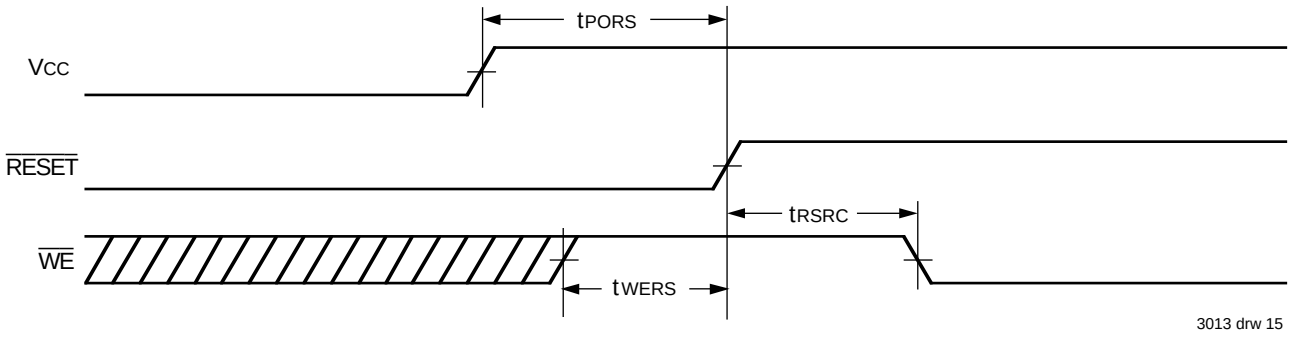
NOTES:
1. Recommended duty cycle = 10% maximum.
2. This parameter is guaranteed with the AC Load (Figure 1) by device characterization, but is not production tested.

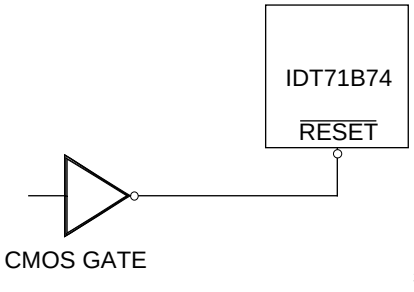
RESET TIMING



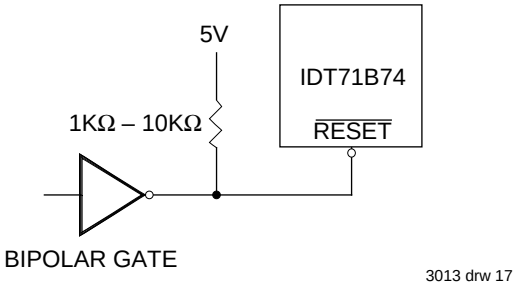
3013 drw 14

POWER ON RESET TIMING





Driving the $\overline{\text{RESET}}$ pin with CMOS logic.



Driving the $\overline{\text{RESET}}$ pin with bipolar logic.

Figure 5.

ORDERING INFORMATION