Integrated Device Technology, Inc.

3.3V PENTIUM™ CLOCK SYNTHESIZER

IDT74FCT3907
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Generates keyboard, floppy disk, system reference, PCI and CPU clocks
- 6 copies of PCI clock & 4 copies of CPU clock available
- 14.31818MHz crystal input
- CPU clock output skew <250ps
  Bus clock output skew <500ps
- 0.03% output frequency accuracy
- Power-on reset
- Selectable CPU clock frequency (50/60/66.66MHz)
- Internal loop filter
- V_{CC} = 3.3 ±0.3V
- Available in 28 pin SOIC
- Supports Pentium™ processor based designs
- Meets Intel Pentium™ processor 3.3V Clock Driver specification (External Draft 1.0)

DESCRIPTION:

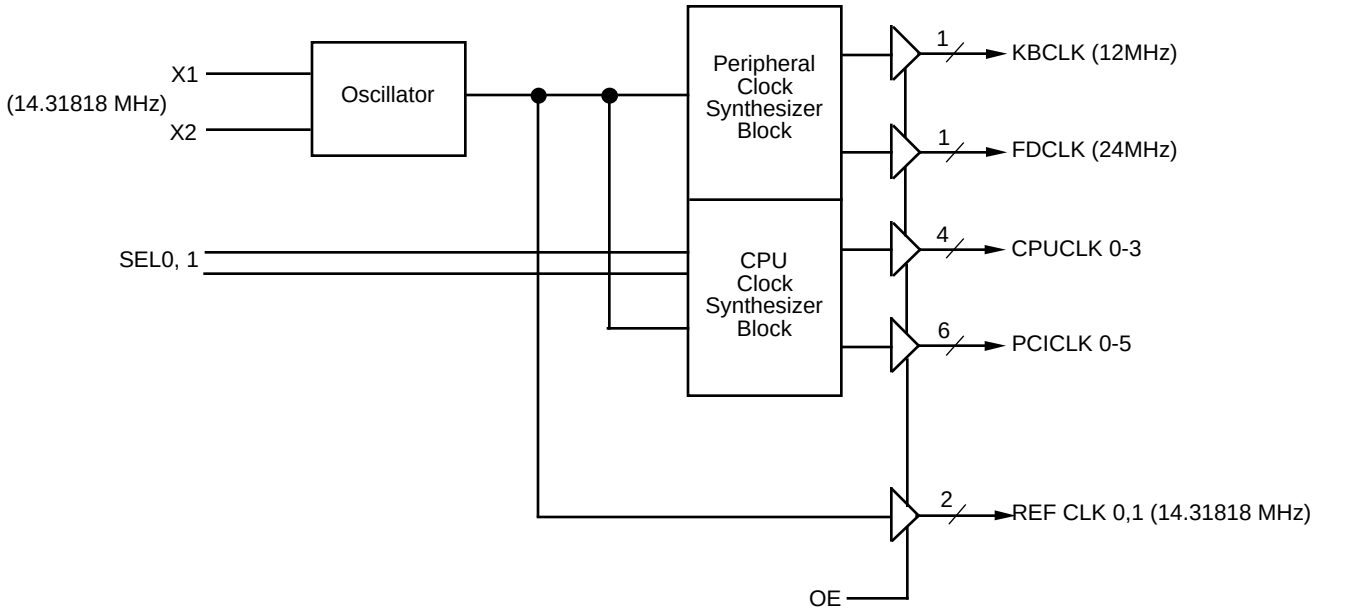
The IDT74FCT3907 Clock synthesizer is built using advanced dual metal CMOS technology. This device uses a 14.31818 MHz crystal input to synthesize the various motherboard clock frequencies.

The output frequencies supported by the IDT74FCT3907 are as follows:

Reference clocks (2) = 14.31818MHz
Keyboard clock (1) = 12MHz
Floppy disk clock (1) = 24MHz
CPU clock (4) = 50/60/66.66 MHz (Selectable by SEL pins)
Bus clock (6) = CPU clock ÷ 2

The SEL0, 1 pins are used to choose appropriate CPUCLK and PCICLK frequencies or to put the device in a test mode. In the test mode, the device outputs various divisors of the test clock frequency. Refer to the function table in this datasheet for details on the different operating modes.

FUNCTIONAL BLOCK DIAGRAM



3245 drw 01

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Pentium™ is a trademark of Intel Corp.

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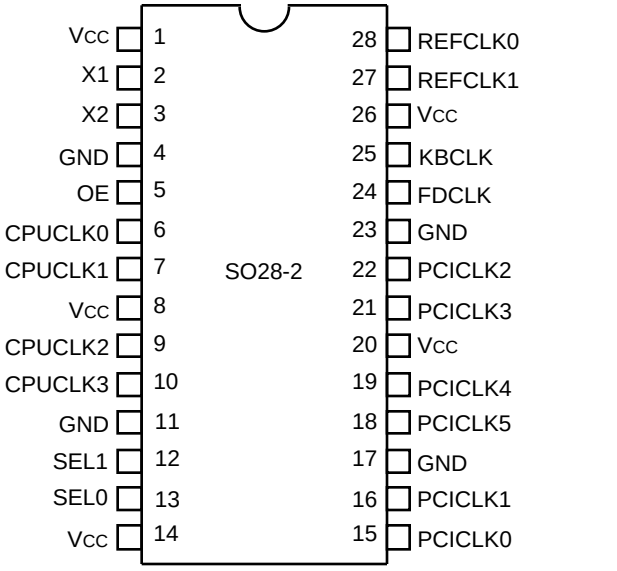
PIN CONFIGURATION



3245 drw 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	0 to +70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–60 to +60	mA

3245 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input, Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

3245 lnk 02

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Name	I/O	Description
X1	I	14.31818 MHz Crystal Input. This is also the test clock input.
X2	O	14.31818 MHz Crystal Output
SEL0, 1	I	CPUCLK Control Inputs
KBCLK	O	Keyboard Clock (12MHz)
FDCLK	O	Floppy Disk Clock (24MHz)
REFCLK 0, 1	O	Reference Clocks (14.31818 MHz)
CPUCLK 0-3	O	CPU Clocks
PCICLK 0-5	O	PCI Bus Clocks
OE	I	Output Enable

3245 tbl 03

FUNCTION TABLE

OE	SEL0	SEL1	INPUT CLK	CPUCLK	PCICLK	REFCLK	FDCLK	KBCLK
0	X	X	14.31818MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	14.31818MHz	50MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	0	1	14.31818MHz	60MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	1	0	14.31818MHz	66.66MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	1	1	TCLK (Test Clock)	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8

3245 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.	V_{CC}–0.6V	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4,6]	V_{CC} = Max., V_O = GND[3]		–43	–135	–206	mA
I_{OS}	Short Circuit Current[4,7]	V_{CC} = Max., V_O = GND[3]		–34	–135	–195	mA
I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	3.0	4.0	mA

3245 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. The test limit for this parameter is ±5µA at T_A = –55°C.
6. Applies to CPUCLK.
7. Applies to PCICLK.

DYNAMIC OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODH}	CPUCLK Output HIGH Current	V_{IN} = V_{IH} or V_{IL},	V_{CC} = 3.135V (3.3V –5%)	–23		—	mA
		V_{OUT} = 2.4V	V_{CC} = 3.465V (3.3V +5%)	—		–109	
I_{ODH}	PCICLK Output HIGH Current	V_{IN} = V_{IH} or V_{IL},	V_{CC} = 3.135V	–14.5		—	mA
		V_{OUT} = 2.4V	V_{CC} = 3.465V	—		–100	
I_{ODL}	CPUCLK Output LOW Current	V_{IN} = V_{IH} or V_{IL},	V_{CC} = 3.135V	16		—	mA
		V_{OUT} = 0.4V	V_{CC} = 3.465V	—		40	
I_{ODL}	PCICLK Output LOW Current	V_{IN} = V_{IH} or V_{IL},	V_{CC} = 3.135V	9.4		—	mA
		V_{OUT} = 0.4V	V_{CC} = 3.465V	—		38	

3245 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. The test limit for this parameter is ±5µA at T_A = –55°C.

OSCILLATOR CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions[1]	Min.	Typ.[2]	Max.	Unit
C_{X1}	X1 Input Capacitance			20		pF
C_{X2}	X2 Output Capacitance			20		pF
I_{IH}	X1 Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		5		µA
I_{IL}	X1 Input LOW Current	V_{CC} = Max., V_{IN} = GND		–5		µA
I_{ODH}	X2 Output HIGH Current	V_{OUT} = V_{CC}		–1		mA
I_{ODL}	X2 Output LOW Current	V_{OUT} = GND		1		mA

3245 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} –0.6V			—	2.0	30	µA
I_C	Total Power Supply Current	V_{CC} = Max.	CPUCLK = 50MHz	V_{IN} = V_{CC}	—			mA
		Outputs Open	CPUCLK = 60MHz	V_{IN} = GND	—			
		50% Duty Cycle OE = V_{CC}	CPUCLK = 66.66MHz		—			

3245 tbl 08

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Per TTL driven input (V_{IN} = V_{CC} -0.6V); all other inputs at V_{CC} or GND.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			74FCT3907						
			66.66MHz		60MHz		50MHz		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{CPU}	CPUCLK Period	TBD	15	—	16.7	—	20	—	ns
t_{CPUH}	CPUCLK HIGH Time[3]		4	—	4	—	4	—	ns
t_{CPUL}	CPUCLK LOW Time[4]		4	—	4	—	4	—	ns
t_{R1}, t_{F1}	CPUCLK Rise, Fall Times (Between 0.4V & 2.4V)		0.8	2.0	0.8	2.0	0.8	2.0	ns
$t_{SK1}(o)$	CPUCLK Output Skew		—	250	—	250	—	250	ps
$t_{SK1}(p)$	CPUCLK Pulse Skew $\lvert t_{PLH}-t_{PHL}\rvert$		—		—		—		ps
t_{PCI}	PCICLK Period		30	—	33.3	—	40	—	ns
t_{PCIH}	PCICLK HIGH Time		12	—	13.3	—	16	—	ns
t_{PCIL}	PCICLK LOW Time		12	—	13.3	—	16	—	ns
t_{R2}, t_{F2}	PCICLK Rise, Fall Time (Between 0.4V & 2.4V)		0.5	2.0	0.5	2.0	0.5	2.0	ns
$t_{SK2}(o)$	PCICLK Output Skew		—	500	—	500	—	500	ps
$t_{SK2}(p)$	PCICLK Pulse Skew $\lvert t_{PLH}-t_{PHL}\rvert$		—		—		—		ps
$t_{SK3}(o)$	CPUCLK to PCICLK Output Delay		1.0	5.0	1.0	5.0	1.0	5.0	ns
t_{PS}	CPUCLK, PCICLK Period Stability		—	250	—	250	—	250	ps
t_{CLOCK}	CPUCLK Lock Time		—	2	—	2	—	2	ms
t_{PLOCK}	PCICLK Lock Time		—	3	—	3	—	3	ms
t_{PZL} t_{PZH}	Output Enable Time OE to KBCLK, FDCLK, REFCLK, CPUCLK, PCICLK (Test Mode)		1.5	8.0	1.5	8.0	1.5	8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time OE to KBCLK, FDCLK, REFCLK, CPUCLK, PCICLK (Test Mode)		1.5	8.0	1.5	8.0	1.5	8.0	ns

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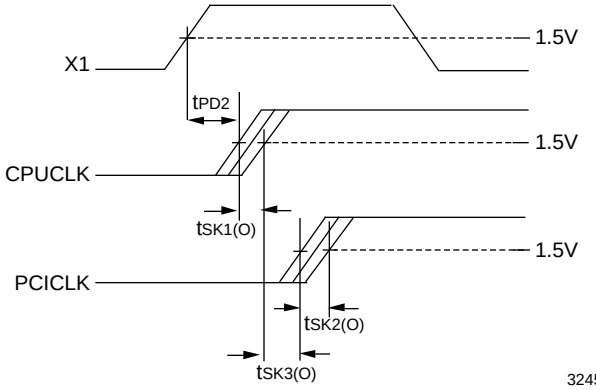
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST WAVEFORMS

PROPAGATION DELAY, OUTPUT SKEW



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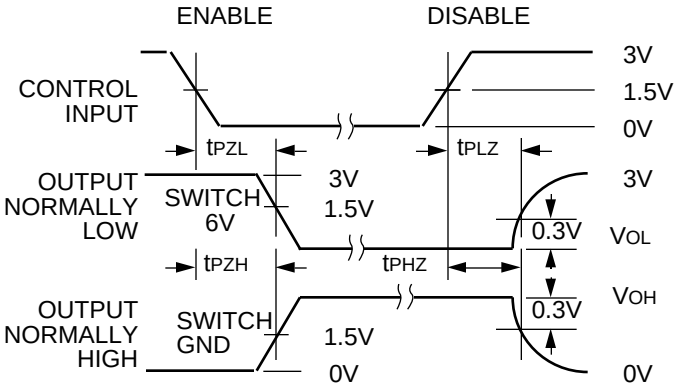
ENABLE AND DISABLE TIMES



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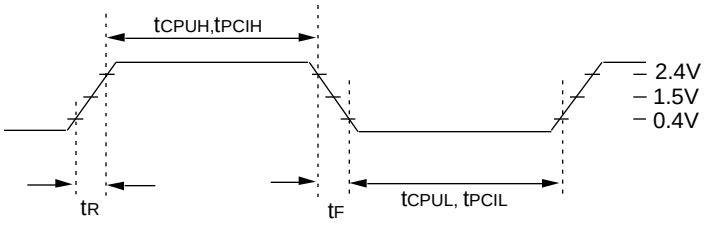
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

PULSE WIDTH, RISE/FALL TIMES



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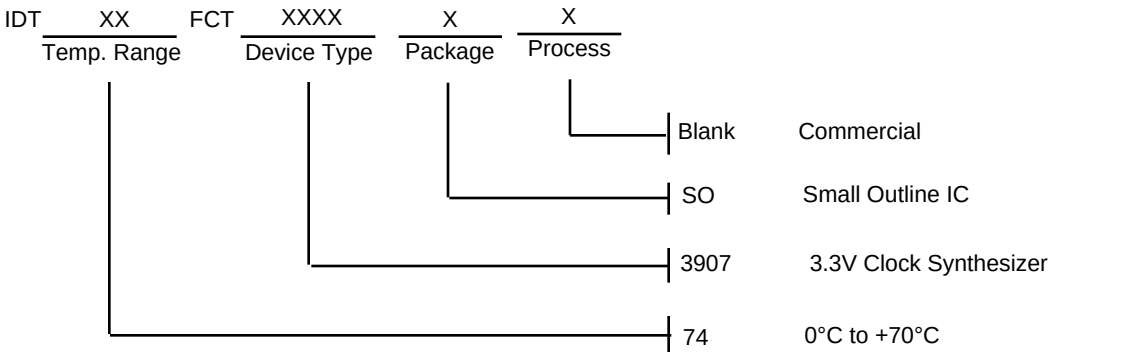
ORDERING INFORMATION



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