Integrated Device Technology, Inc.

3.3V LOW SKEW PLL-BASED CMOS CLOCK DRIVER

IDT74FCT3932-100
IDT74FCT32932-100
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew
- 16 programmable frequency configurations
- 17 3-state outputs: ±24 mA FCT3932
  ±8 mA FCT32932
- Output configuration:
  BANK1: 4 outputs
  BANK2: 8 outputs
  BANK3: 5 outputs
- Dedicated feedback output (Q_FB)
- Maximum output frequency: 100MHz
- V_{CC} = 3.3V ±0.3V
- Inputs can be driven from 3.3V or 5V components
- Available in 48 SSOP, TSSOP packages
- Suited to SDRAM applications

DESCRIPTION:

The FCT3932 uses phase-lock loop technology to lock the frequency and phase of the feedback to the input reference clock. It provides a large number of low skew outputs that are configurable in 16 different modes using the CNTRL 1-4 inputs. A dedicated output, Q_FB, is provided to supply the PLL feedback and it should be connected to the FEEDBACK input. Q_FB is located adjacent to FEEDBACK to minimize the delay in the feedback path. In order to offset any delay in the output path from the FCT3932 output to a receiving device, feedback path delay should be made to match this output path delay.

The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The FCT3932 requires no external loop filter components.

The FCT3932 provides 17 outputs grouped in 3 banks with individual 3-state control and an additional dedicated feedback output with no disable. Connecting Q_FB to FEEDBACK ensures uninterrupted PLL operation when all outputs are disabled.

Individual bank 3-state allows users to disable unused outputs in order to limit power dissipation or minimize switching noise. It also allows users to shut down outputs in low power modes while maintaining phase lock.

The FCT3932 provides a LOCK pin that goes high when the device is phase-locked.

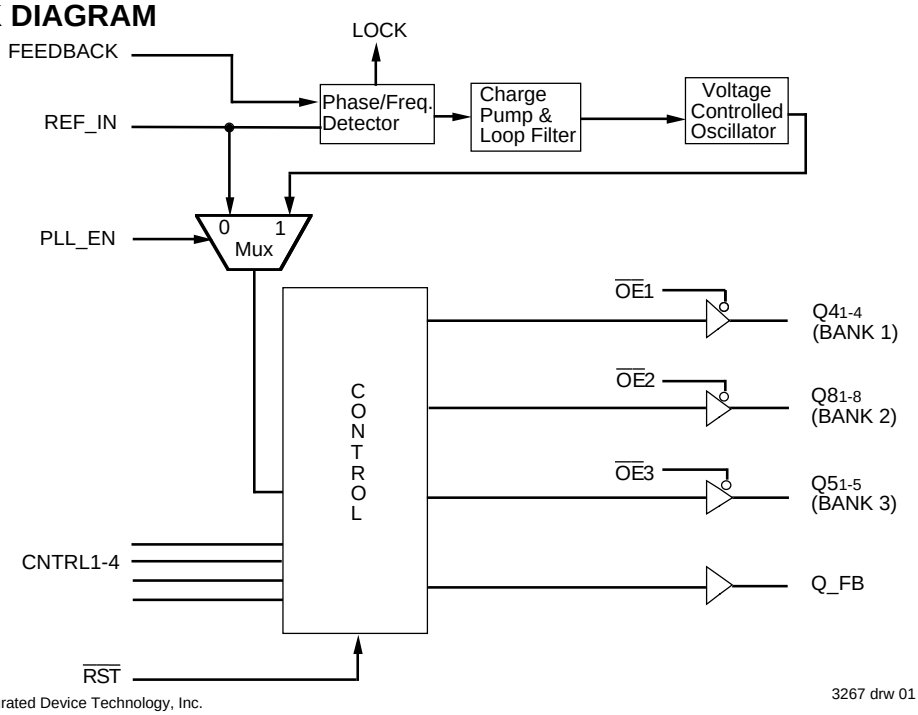
The user can bypass the PLL for testability purposes by deasserting PLL_EN. In this "test" mode, the input frequency is not limited to the specified range.

The FCT3932 provides an asynchronous reset input, $\overline{RST}$, which resets all outputs. This initializes all internal registers so that outputs start up in a known state.

APPLICATIONS:

SDRAM DIMM Clock, Caches, high speed microprocessors, motherboard clock distribution to DIMMs.

FUNCTIONAL BLOCK DIAGRAM



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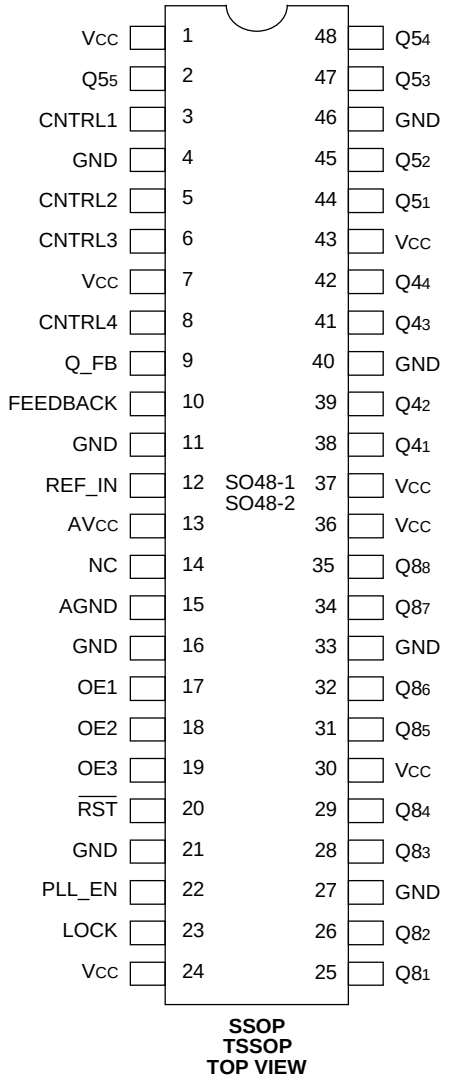
PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

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*NC = No connect

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.2	5.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.7	8.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Name	I/O	Description
REF_IN	I	Reference clock input.
FEEDBACK	I	Feedback input to phase detector.
$Q4_{1-4}$	O	BANK1 clock outputs.
$Q8_{1-8}$	O	BANK2 clock outputs.
$Q5_{1-5}$	O	BANK3 clock outputs.
$\overline{OE}$1-3	I	Output enable controls for BANKS 1, 2 and 3 (Active LOW).
CNTRL1-4	I	Control lines to select output configuration (see table).
Q_FB	O	Dedicated PLL feedback output.
$\overline{RST}$	I	Asynchronous reset (Active LOW).
PLL_EN	I	Disables phase-lock for low frequency testing (Refer to functional block diagram).
LOCK	O	PLL "LOCK" indicator (HIGH when PLL is locked).

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OUTPUT FREQUENCY CONFIGURATION AND INPUT FREQUENCY RANGE TABLE

MODE	CNTRL 4 3 2 1	Q_FEEDBACK	Q_BANK1 (4 outputs)	Q_BANK2 (8 outputs)	Q_BANK3 (5 outputs)	F_{IN} Range
0	0 0 0 0	F (divide-by-1)	$\overline{F}$	F	F	50-100MHz
1	0 0 0 1	F (divide-by-1)	$\overline{F}$	F	F/2	50-100MHz
2	0 0 1 0	F (divide-by-1)	F	F	F	50-100MHz
3	0 0 1 1	F (divide-by-1)	F	F/2	F/2	50-100MHz
4	0 1 0 0	F (divide-by-1)	F	F/3	F	50-100MHz
5	0 1 0 1	F (divide-by-3)	3F	3F	F	16.7-33.3MHz
6	0 1 1 0	F (divide-by-3)	3F	F	3F	16.7-33.3MHz
7	0 1 1 1	F (divide-by-3)	3F	3F	3F	16.7-33.3MHz
8	1 0 0 0	F (divide-by-2)	2F	2F	2F	25-50MHz
9	1 0 0 1	F (divide-by-2)	2F	F	2F	25-50MHz
10	1 0 1 0	F (divide-by-2)	2F	F	F	25-50MHz
11	1 0 1 1	F (divide-by-2)	2F	F	F/2	25-50MHz
12	1 1 0 0	F (divide-by-2)	2F	F/2	F	25-50MHz
13	1 1 0 1	F (divide-by-4)	4F	2F	4F	12.5-25MHz
14	1 1 1 0	F (divide-by-4)	4F	2F	2F	12.5-25MHz
15	1 1 1 1	F (divide-by-4)	4F	2F	F	12.5-25MHz

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–75		mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	75		mA
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	—	6	mA

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TYPE 1 DRIVER - FCT3932

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.2[4]	2.4	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	—	—	0.2	V
			I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	

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TYPE 2 DRIVER - FCT32932

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4[4]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.05mA	—	—	0.2	V
			I_{OL} = 4mA	—	0.2	0.4	
			I_{OL} = 8mA	—	0.3	0.5	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. V_{OH} = V_{CC} –0.6V at rated current.

INPUT TIMING REQUIREMENTS

Symbol	Parameter		Min.	Max.	Unit
$t_{RISE/FALL}$	Rise/Fall Times REF_IN input (0.8V to 2.0V)		—	3.0	ns
Frequency	Input Frequency REF_IN input	Modes 0, 1, 2, 3, 4	50	100	MHz
		Modes 5, 6, 7	16.7	33.3	
		Modes 8, 9, 10, 11, 12	25	50	
		Modes 13, 14, 15	12.5	25	
Duty Cycle	Input Duty Cycle, REF_IN input		25	75	%

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OUTPUT FREQUENCY SPECIFICATIONS

Mode	Parameter		Min.	Max.	Unit
0, 1, 2, 3,4	Operating frequency	F, $\overline{F}$ Outputs	50	100	MHz
		F/2 Outputs	25	50	
		F/3 Outputs	16.7	33.3	
5, 6, 7	Operating frequency	3F Outputs	50	100	
		F Outputs	16.7	33.3	
8, 9, 10, 11, 12	Operating frequency	2F Outputs	50	100	
		F Outputs	25	50	
		F/2 Outputs	12.5	25	
13, 14, 15	Operating frequency	4F Outputs	50	100	
		2F Outputs	25	50	
		F Outputs	12.5	25	

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} –0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. All Outputs Open 50% Duty Cycle	V_{IN} = V_{CC} F = 50Mhz V_{IN} = GND MODE 10	—	72		µA/ MHz/ bit
I_C	Total Power Supply Current[5,6]	V_{CC} = Max. PLL_EN = 1, LOCK = 1, MODE 10 REF_IN frequency = 50MHz. All outputs open		—	62		mA

NOTES:

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1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f) + I_{LOAD}$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f = SYNC input frequency
   I_{LOAD} = Dynamic Current due to load.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE(7)

Symbol	Parameter		Condition(1)	Min.(2)	Max.	Unit
t_{PD}(3) REF_IN-Q_FB	Propagation Delay (REF_IN input to Q outputs)		No Load	–0.5	+0.5	ns
$t_{RISE/FALL}$	Rise/Fall Time (between 0.8 and 2.0V)	FCT3932	C_L = 20pF for FCT3932	0.5	1.5	ns
All Outputs		FCT32932	C_L = 10pF for FCT32932	0.5	2.0	
t_{PW}(3)	Output Duty Cycle			45	55	%
t_{SKEWr}(3,4)	Output to Output Skew (All outputs at same frequency rising edge)			—	500	ps
t_{SKEWf}(3,4)	Output to Output Skew (All outputs at same frequency falling edge)			—	500	ps
$t_{SKEWall}$(3,4)	Output to Output Skew (All outputs, rising edge any frequency)			—	1.0	ns
t_{LOCK}(5)	Time required to acquire Phase-Lock from time REF_IN input signal is received			1	10	ms
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$x (LOW-to-HIGH) to Q			3.0	8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$x (HIGH-to-LOW) to Q			3.0	8.0	ns

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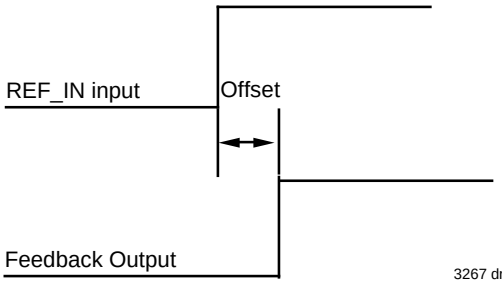
GENERAL AC SPECIFICATION NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. These specifications are guaranteed but not production tested.
4. Under equally loaded conditions, as specified under test conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered-on and Q_FB properly connected to the FEEDBACK pin.
6. The tPD spec gives the limits of the phase offset between the REF_IN input and the Q_FB output.
7. The AC specifications are only guaranteed with the decoupling scheme shown in figure 2.

t_{PD} = ±0.5ns



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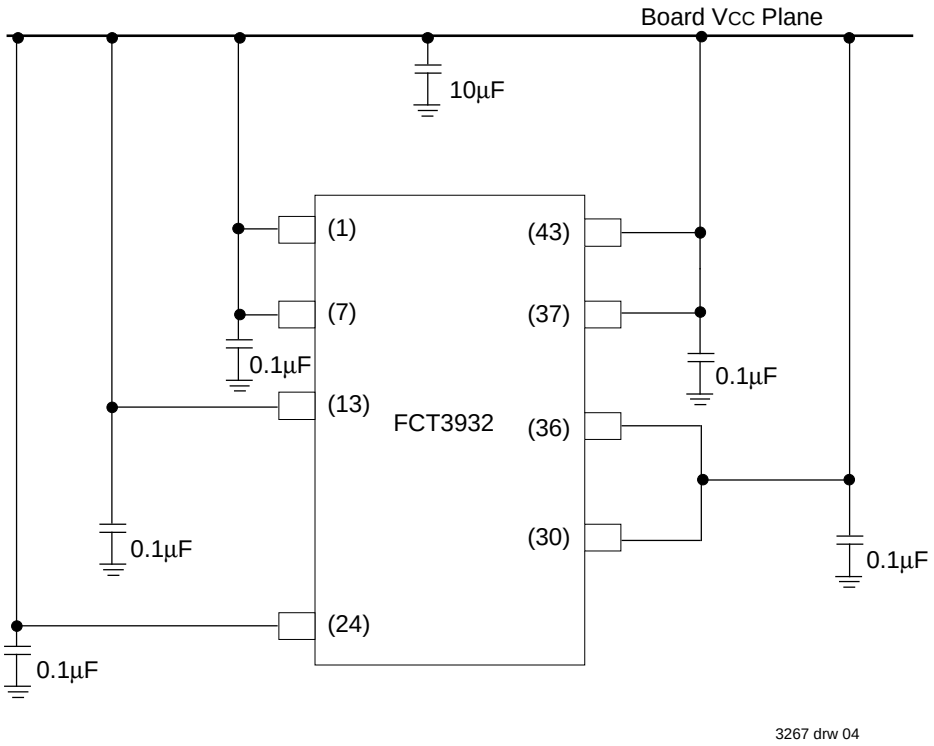
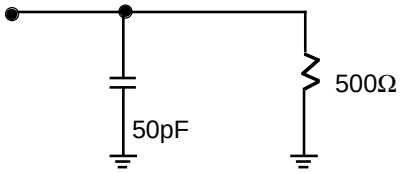


Figure 2. Recommended Decoupling for the FCT3932/FCT32932

NOTES:

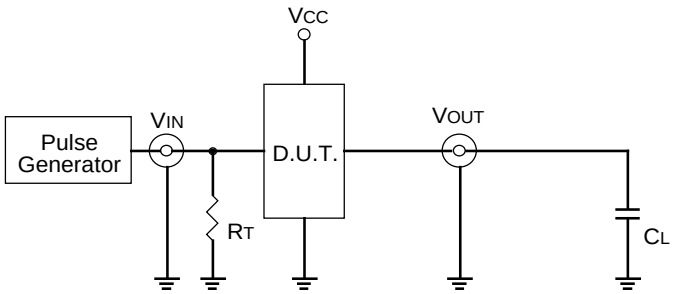
1. Figure 2 shows a decoupling scheme which will be effective in most FCT3932 applications. The following guidelines should be followed for stable, jitter-free operation:
   a. All decoupling capacitors should be connected as close to the package as possible. (Preferably at the device pins).
   b. The 10µF and 0.1µF bypass capacitors provide protection from power supply and ground plane transients.

STANDARD LOAD (USED WHEN SPECIFIED)



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT



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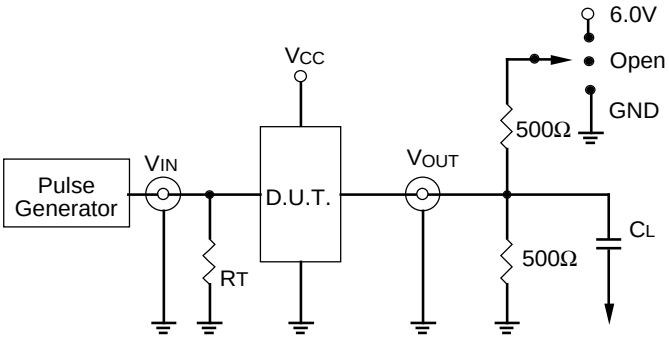
ENABLE/DISABLE TEST CIRCUIT



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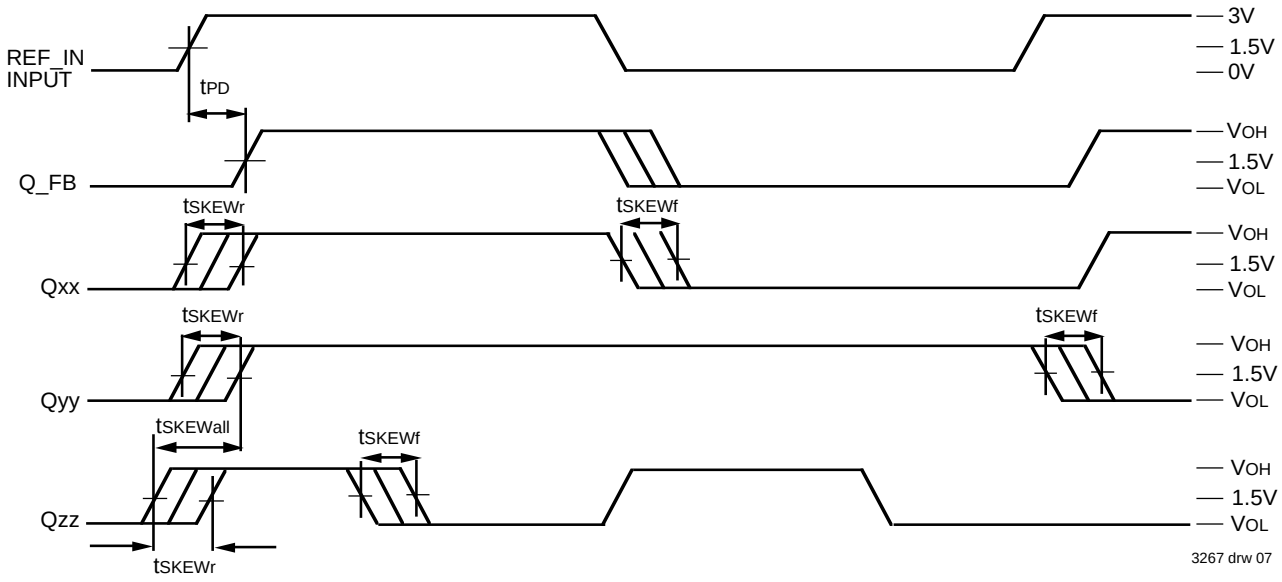
PROPAGATION DELAY, OUTPUT SKEW



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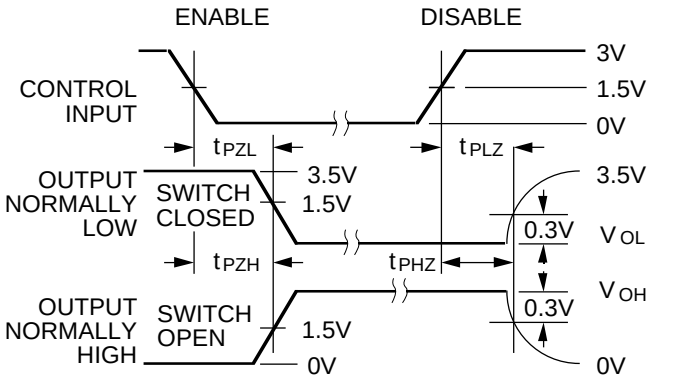
ENABLE AND DISABLE TIMES



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NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: $t_F \leq 2.5ns$; $t_R \leq 2.5ns$

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

ORDERING INFORMATION