Integrated Device Technology, Inc.

HIGH-SPEED 64K x 16 BANK-SWITCHABLE DUAL-PORTED SRAM WITH EXTERNAL BANK SELECTS

ADVANCED
IDT707288S/L

FEATURES:

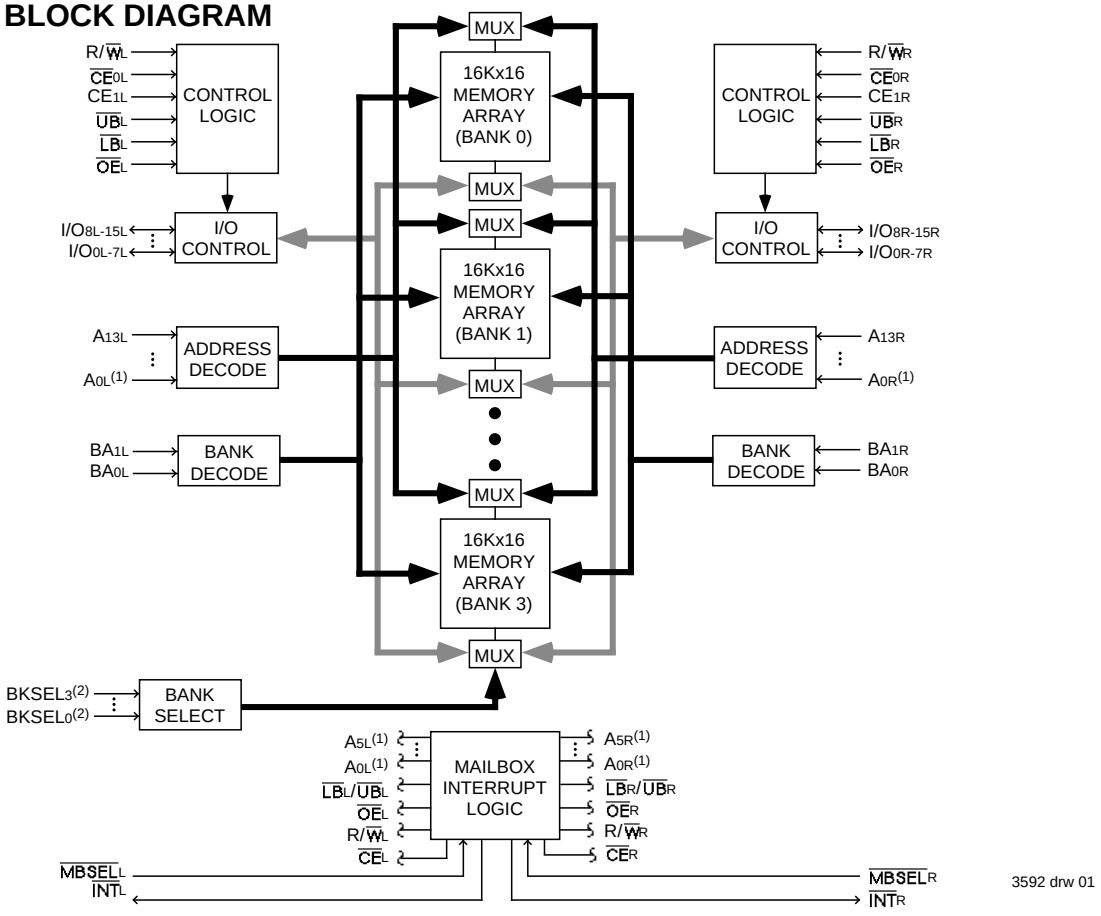
- 64K x 16 Bank-Switchable Dual-Ported SRAM Architecture
  - Four independent 16K x 16 banks
  - 1 Megabit of memory on chip
- Fast asynchronous address-to-data access time: 20ns
- User-controlled input pins included for bank selects
- Independent port controls with asynchronous address & data busses
- Four 16-bit mailboxes available to each port for inter-processor communications; interrupt option
- Interrupt flags with programmable masking
- Dual Chip Enables allow for depth expansion without external logic
- $\overline{UB}$ and $\overline{LB}$ are available for bus matching to x8 or x16 busses; also support very fast banking
- TTL-compatible, single 5V (±10%) power supply
- Available in a 100-pin Thin Quad Plastic Flatpack (TQFP) and a 108-pin ceramic Pin Grid Array (PGA)

DESCRIPTION:

The IDT707288 is a high-speed 64K x 16 (1M bit) Bank-Switchable Dual-Ported SRAM organized into four independent 16K x 16 banks. The device has two independent ports with separate controls, addresses, and I/O pins for each port, allowing each port to asynchronously access any 16K x 16 memory block not already accessed by the other port. Accesses by the ports into specific banks are controlled via bank select pin inputs under the user's control. Mailboxes are provided to allow inter-processor communications. Interrupts are provided to indicate mailbox writes have occurred. An automatic power down feature controlled by the chip enables ($\overline{CE}_0$ and CE_1) permits the on-chip circuitry of each port to enter a very low standby power mode and allows fast depth expansion.

The IDT707288 offers a maximum address-to-data access time as fast as 20ns, while typically operating on only 900mW of power, and is available in a 100-pin Thin Quad Plastic Flatpack (TQFP) and a 108-pin ceramic Pin Grid Array (PGA).

FUNCTIONAL BLOCK DIAGRAM



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NOTES:

1. The first six address pins for each port serve dual functions. When $\overline{MBSEL}$ = V_{IH}, the pins serve as memory address inputs. When $\overline{MBSEL}$ = V_{IL}, the pins serve as mailbox address inputs.
2. Each bank has an input pin assigned that allows the user to toggle the assignment of that bank between the two ports. Refer to Table I for more details.

FUNCTIONALITY:

The IDT707288 is a high-speed asynchronous 64K x 16 Bank-Switchable Dual-Ported SRAM, organized in four 16K x 16 banks. The two ports are permitted independent, simultaneous access into separate banks within the shared array. There are four user-controlled Bank Select input pins , and each of these pins is associated with a specific bank within the memory array. Access to a specific bank is gained by placing the associated Bank Select pin in the appropriate state: V_{IH} assigns the bank to the left port, and V_{IL} assigns the bank to the right port (See Truth Table I). Once a bank is assigned to a particular port, the port has full access to read and write within that bank. Each port can be assigned as many banks within the array as needed, up to and including all four banks.

The IDT707288 provides mailboxes to allow inter-processor communications. Each port has four 16-bit mailbox registers available to which it can write and read and which the opposite port can read only. These mailboxes are external to the common SRAM array, and are accessed by setting $\overline{MBSEL}$ = V_{IL} while setting $\overline{CE}$ = V_{IH}. Each mailbox has an associated interrupt: a port can generate an interrupt to the opposite port by writing to the upper byte of any one of its four 16-bit mailboxes. The interrupted port can clear the interrupt by reading the upper byte. This read will not alter the contents of the mailbox.

If desired, any source of interrupt can be independently masked via software. Two registers are provided to permit interpretation of interrupts: the Interrupt Cause Register and the Interrupt Status Register. The Interrupt Cause Register gives the user a snapshot of what has caused the interrupt to be generated - the specific mailbox written to. The information in this register provides post-mask signals: Interrupt sources that have been masked will not be updated. The Interrupt Status Register gives the user the status of all bits that could potentially cause an interrupt regardless of whether they have been masked. Truth Table II gives a detailed explanation of the use of these registers.

PIN NAMES

A_0 - A_{13} (1,6)	Address Inputs
BA_0 - BA_1 (1)	Bank Address Inputs
$\overline{MBSEL}$ (1)	Mailbox Access Control Gate
BKSEL(2)	Bank Select Inputs
R/$\overline{W}$ (1)	Read/Write Enable
$\overline{OE}$ (1)	Output Enable
$\overline{CE0}$, CE1 (1)	Chip Enables
$\overline{UB}$, $\overline{LB}$ (1)	I/O Byte Enables
I/O_0 – I/O_{15} (1)	Bidirectional Data Input/Output
$\overline{INT}$ (1)	Interrupt Flag (Output)(3)
V_{CC} (4)	+5V Power
GND (5)	Ground

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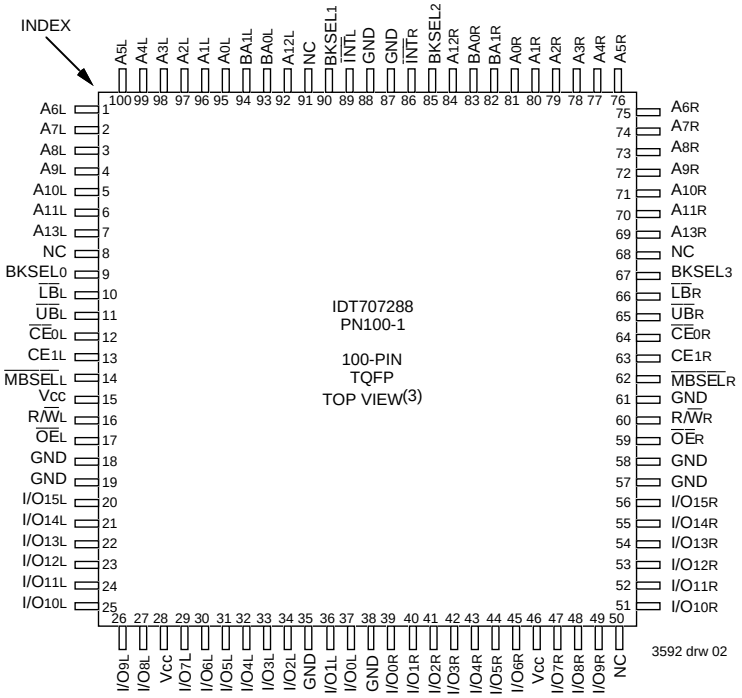
NOTES:
1. Duplicated per port.
2. Each bank has an input pin assigned that allows the user to toggle the assignment of that bank between the two ports. Refer to Table I for more details.
3. Generated upon mailbox access.
4. All Vcc pins must be connected to power supply.
5. All GND pins must be connected to ground supply.
6. The first six address pins for each port serve dual functions. When $\overline{MBSEL}$ = V_{IH}, the pins serve as bank address or memory address inputs. When $\overline{MBSEL}$ = V_{IL}, the pins serve as mailbox address inputs.

PIN CONFIGURATIONS (1,2)



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CON'T.) [1,2]

	A	B	C	D	E	F	G	H	J	K	L	M
12	81 A7R	80 A8R	77 A11R	74 BK SEL3	72 $\overline{UB}$R	69 $\overline{MB}$ $\overline{SEL}$R	68 GND	65 GND	63 NC	60 I/O13R	57 I/O10R	54 NC
11	84 A4R	83 A5R	78 A10R	76 A13R	73 $\overline{LB}$R	70 CE1R	67 R/$\overline{W}$R	64 GND	61 I/O14R	59 I/O12R	56 I/O9R	53 NC
10	87 A1R	86 A2R	82 A6R	79 A9R	75 NC	71 $\overline{CE}$0R	66 $\overline{OE}$R	62 I/O15R	58 I/O11R	55 NC	51 I/O8R	50 I/O7R
09	90 BA0R	88 A0R	85 A3R							52 NC	49 Vcc	47 I/O5R
08	92 BK SEL2	91 A12R	89 BA1R							48 I/O6R	46 I/O4R	45 I/O3R
07	95 GND	94 GND	93 $\overline{INT}$R			IDT707288 G108-1				44 I/O2R	43 I/O1R	42 I/O0R
06	96 $\overline{INT}$L	97 BK SEL1	98 NC			108-Pin PGA[3] Top View				39 I/O1L	40 I/O0L	41 GND
05	99 A12L	100 BA0L	102 A0L							35 I/O4L	37 I/O2L	38 GND
04	101 BA1L	103 A1L	106 A4L							31 Vcc	34 I/O5L	36 I/O3L
03	104 A2L	105 A3L	1 A7L	4 A10L	8 BK SEL0	12 CE1L	17 GND	21 I/O14L	25 I/O10L	28 NC	32 I/O7L	33 I/O6L
02	107 A5L	2 A8L	5 A11L	7 NC	10 $\overline{UB}$L	13 $\overline{MB}$ $\overline{SEL}$L	16 $\overline{OE}$L	19 GND	22 I/O13L	24 I/O11L	29 NC	30 I/O8L
01	108 A6L	3 A9L	6 A13L	9 $\overline{LB}$L	11 $\overline{CE}$0L	14 Vcc	15 R/$\overline{W}$L	18 NC	20 I/O15L	23 I/O12L	26 I/O9L	27 NC

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NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

ASSIGNING THE BANKS VIA THE EXTERNAL BANK SELECTS

There are four bank select pins available on the IDT707288, and each of these pins is associated with a specific bank within the memory array. The pins are user-controlled inputs: access to a specific bank is assigned to a particular port by setting the input to the appropriate level. The process of assigning the banks is detailed in Truth Table I. Once a bank is assigned to a port, the owning port has full access to read and write within that bank. The opposite port is unable to access that bank until the user reassigns the port. Access by a port to a bank which it does not control will have no effect if written, and if read unknown values on D_0-D_{15} will be returned. Each port can be assigned as many banks within the array as needed, up to and including all four banks.

The bank select pin inputs must be set at either V_{IH} or V_{IL} - these inputs are not tri-statable. When changing the bank select inputs (changing the bank assignments), the device must be write-disabled ($\overline{CE}$ and/or R/$\overline{W}$ set to V_{IH}).

TRUTH TABLE I – MEMORY BANK ASSIGNMENT ($\overline{CE}$ AND/OR R/$\overline{W}$ = V_{IH})(2,3)

BKSEL0	BKSEL1	BKSEL2	BKSEL3	BANK AND DIRECTION(1)
H	X	X	X	BANK 0 LEFT
X	H	X	X	BANK 1 LEFT
X	X	H	X	BANK 2 LEFT
X	X	X	H	BANK 3 LEFT
L	X	X	X	BANK 0 RIGHT
X	L	X	X	BANK 1 RIGHT
X	X	L	X	BANK 2 RIGHT
X	X	X	L	BANK 3 RIGHT

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NOTES:

1. Bank 0 refers to the first 16Kx16 memory spaces, Bank 1 to the second 16Kx16 memory spaces, Bank 2 to the third 16Kx16 memory spaces, and Bank 3 to the fourth 16Kx16 memory spaces. 'LEFT' indicates the bank is assigned to the left port; 'RIGHT' indicates the bank is assigned to the right port.
2. The bank select pin inputs must be set at either V_{IH} or V_{IL} - these inputs are not tri-statable. When changing the bank select inputs (changing the bank assignments), the device must be write-disabled ($\overline{CE}$ and/or R/$\overline{W}$ set to V_{IH}).
3. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = Don't Care.

MAILBOX INTERRUPTS AND INTERRUPT CONTROL REGISTERS

If the user chooses to use the mailbox interrupt function, four mailbox locations are assigned to each port. These mailbox locations are external to the memory array. The mailboxes are accessed by taking $\overline{MBSEL}$ Low while holding $\overline{CE}$ High.

The mailboxes are 16 bits wide: the message is user-defined since these are addressable SRAM locations. An interrupt is generated to the opposite port upon writing to the upper byte of any mailbox location. A port can read the message it has just written in order to verify it: this read will not alter the status of the interrupt sent to the opposite port. The interrupted port can clear the interrupt by reading the upper byte of the applicable mailbox. This read will not alter the contents of the mailbox. The use of mailboxes to generate interrupts to the opposite port and the reading of mailboxes to clear interrupts is detailed in Truth Table II.

If desired, any of the mailbox interrupts can be independently masked via software. Masking of the interrupt sources is done in the Mask Register. The masks are individual and independent: a port can mask any combination of interrupt sources with no effect on the other sources. Each port can modify only its own Mask Register. The use of this register is detailed in Truth Table II.

Two registers are provided to permit interpretation of interrupts: these are the Interrupt Cause Register and the Interrupt Status Register. The Interrupt Cause Register gives the user a snapshot of what has caused the interrupt to be generated - a specific semaphore granted to that port or a specific mailbox written to by the opposite port. The information in this register provides post-mask signals: interrupt sources that have been masked will not be updated. The Interrupt Status Register gives the user the status of all bits that could potentially cause an interrupt regardless of whether they have been masked. The use of the Interrupt Cause Register and the Interrupt Status Register is detailed in Truth Table II.

TRUTH TABLE II – MAILBOX INTERRUPTS ($\overline{CE}$ = V_{IH})(8,9)

$\overline{MB}$																									
$\overline{SEL}$	R/$\overline{W}$	$\overline{UB}$	$\overline{LB}$	A5	A4	A3	A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	DESCRIPTION
L	X	X	X	L	L	L	L	L	L	RESERVED (7)																RESERVED (7)
L	X	X	X	⋮	⋮	⋮	⋮	⋮	⋮	RESERVED (7)																RESERVED (7)
L	(1)	(1)	(1)	H	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 0 - SET INTERRUPT ON OPPOSITE PORT
L	(1)	(1)	(1)	H	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 1 - SET INTERRUPT ON OPPOSITE PORT
L	(1)	(1)	(1)	H	L	L	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 2 - SET INTERRUPT ON OPPOSITE PORT
L	(1)	(1)	(1)	H	L	L	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 3 - SET INTERRUPT ON OPPOSITE PORT
↯	H	(2)	(2)	H	L	L	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 0 - CLEAR OPPOSITE PORT INTERRUPT
↯	H	(2)	(2)	H	L	L	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 1 - CLEAR OPPOSITE PORT INTERRUPT
↯	H	(2)	(2)	H	L	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 2 - CLEAR OPPOSITE PORT INTERRUPT
↯	H	(2)	(2)	H	L	L	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MAILBOX 3 - CLEAR OPPOSITE PORT INTERRUPT
L	(3)	(3)	(3)	H	L	H	L	L	L	(4)	(4)	(4)	(4)	(5)	(5)	(5)	(5)	(6)	(6)	(6)	(6)	X	X	X	X	MAILBOX INTERRUPT CONTROLS
L	X	X	X	⋮	⋮	⋮	⋮	⋮	⋮	RESERVED (7)																RESERVED (7)
L	X	X	X	H	H	H	H	H	H	RESERVED (7)																RESERVED (7)

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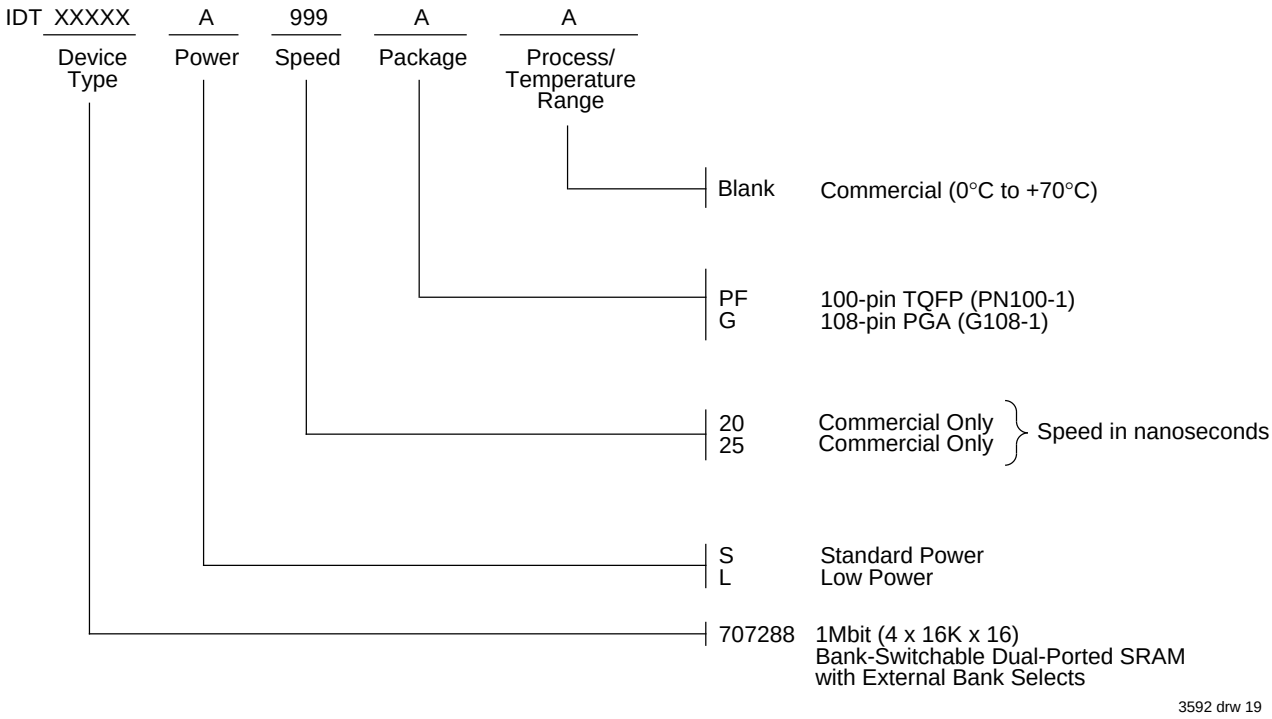
NOTES:

1. There are four independent mailbox locations available to each side, external to the standard memory array. The mailboxes can be written to in either 8-bit or 16-bit widths. The upper byte of each mailbox has an associated interrupt to the opposite port. The mailbox interrupts can be individually masked if desired, and the status of the interrupt determined by polling the Interrupt Status Register (see Note 6 for this table). A port can read its own mailboxes to verify the data written, without affecting the interrupt which is sent to the opposite port.
2. These registers allow a port to read the data written to a specific mailbox location by the opposite port. Reading the upper byte of the data in a particular mailbox clears the interrupt associated with that mailbox without modifying the data written. Once the address and R/$\overline{W}$ are stable, the actual clearing of the interrupt is triggered by the transition of $\overline{MBSEL}$ from V_{IH} to V_{IL}.
3. This register contains the Mask Register (bits D_0-D_3), the Interrupt Cause Register (bits D_4-D_7), and the Interrupt Status Register (bits D_8-D_{11}). The controls for R/$\overline{W}$, $\overline{UB}$, and $\overline{LB}$ are manipulated in accordance with the appropriate function. See Notes 4, 5, and 6 for this table. Bits D_{12}-D_{15} are "Don't Care".
4. This register, the Mask Register, allows the user to independently mask the various interrupt sources. Writing V_{IH} to the appropriate bit (D_0 = Mailbox 0, D_1 = Mailbox 1, D_2 = Mailbox 2, and D_3 = Mailbox 3) disables the interrupt, while writing V_{IL} enables the interrupt. All four bits in this register must be written at the same time. This register can be read at any time to verify the mask settings. The masks are individual and independent: any single interrupt source can be masked with no effect on the other sources. Each port can modify only its own mask settings.
5. This register, the Interrupt Cause Register, gives the user a snapshot of what has caused the interrupt to be generated. Reading V_{OL} for a specific bit (D_4 = Mailbox 0, D_5 = Mailbox 1, D_6 = Mailbox 2, and D_7 = Mailbox 3) indicates that the associated interrupt source has generated an interrupt. Acknowledging the interrupt clears the bit in this register (see Note 2 for this table). This register provides post-mask information: if the interrupt source has been masked, the associated bit in this register will not update.
6. This register, the Interrupt Status Register, gives the user the status of all interrupt sources that could potentially cause an interrupt regardless of whether they have been masked. Reading V_{OL} for a specific bit (D_8 = Mailbox 0, D_9 = Mailbox 1, D_{10} = Mailbox 2, and D_{11} = Mailbox 3) indicates that the associated interrupt source has generated an interrupt. Acknowledging the interrupt clears the associated bit in this register (see Note 2 for this table). This register provides pre-mask information: regardless of whether an interrupt source has been masked, the associated bit in this register will update.
7. Access to registers defined as "RESERVED" will have no effect, if written, and if read unknown values on D_0-D_{15} will be returned.
8. These registers are not guaranteed to initialize in any known state. At power-up, the initialization sequence should include the set-up of these registers.
9. 'L' = V_{IL} or V_{OL}, 'H' = V_{IH} or V_{OH}, 'X' = Don't Care.

ORDERING INFORMATION



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