Integrated Device Technology, Inc.

LOW POWER 3V CMOS SRAM 1 MEG (128K x 8-BIT)

ADVANCE INFORMATION
IDT71L024

FEATURES:

- 128K x 8 Organization
- Wide Operating Voltage Range: 2.7V to 3.6V
- Speed Grades: 70ns, 100ns
- Low Operating Power: 25mA (max)
- Low Standby Power: 5µA (max)
- Low-Voltage Data Retention: 1.5V (min)
- Available in 32-pin, 13.4mm x 8mm Type I TSOP package

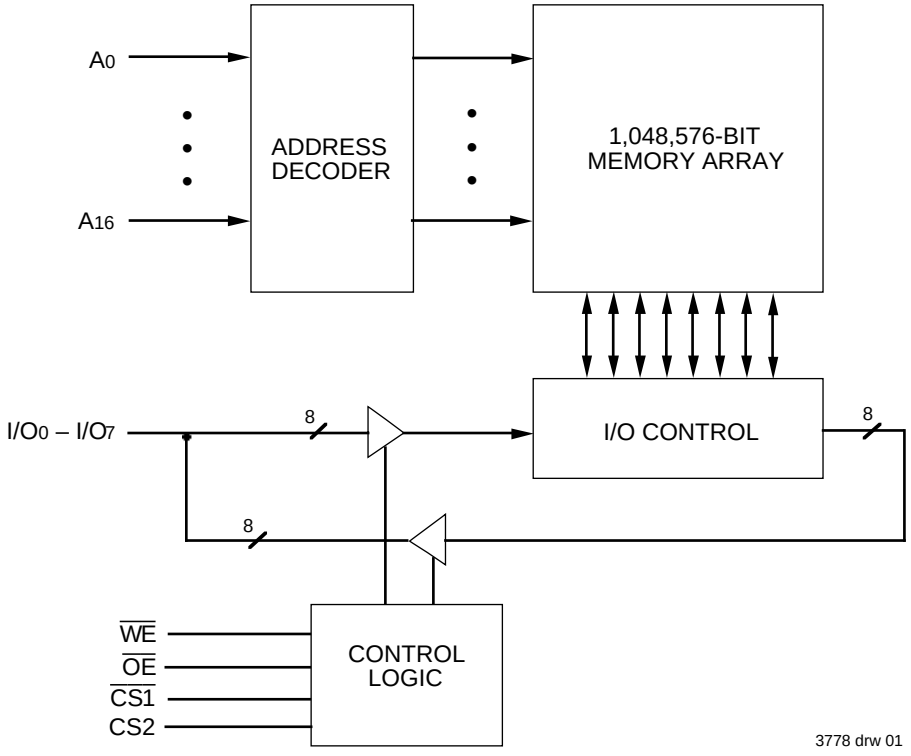
DESCRIPTION:

The IDT71L024 is a 1,048,576-bit very low-power Static RAM organized as 128K x 8. It is fabricated using IDT's high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for low-power memory needs. It uses a 6-transistor memory cell.

All input and output signals of the IDT71L024 are LVTTL-compatible and operation is from a single extended-range 3.3V supply. This extended supply range makes the device ideally suited for unregulated battery-powered applications. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71L024 is packaged in a JEDEC standard 32-pin TSOP Type I.

FUNCTIONAL BLOCK DIAGRAM



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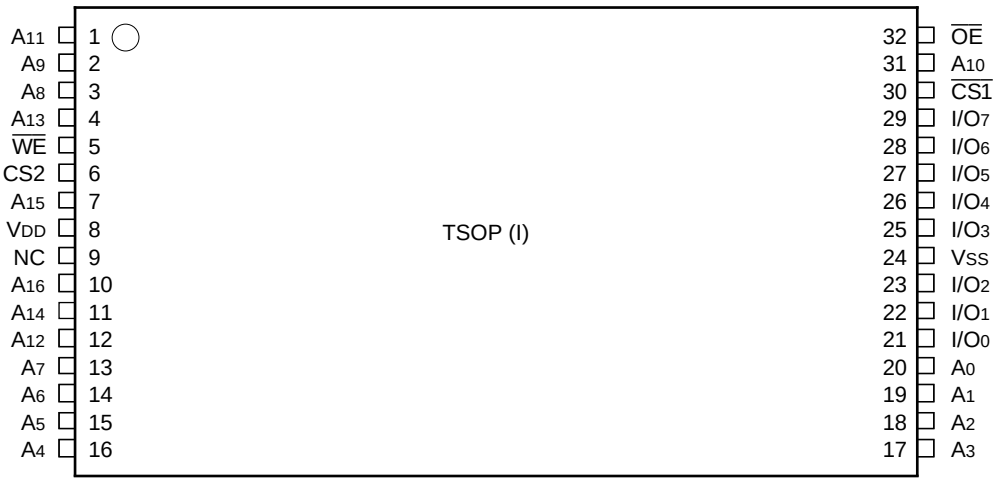
PIN CONFIGURATIONS



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TSOP
TOP VIEW

TRUTH TABLE(1)

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O0-I/O7	Function
H	X	X	X	High-Z	Deselected - Standby
X	L	X	X	High-Z	Deselected - Standby
L	H	L	H	DATAOUT	Read
L	H	X	L	DATAIN	Write
L	H	H	H	High-Z	Outputs Disabled

NOTE: 3778 tbl 02

1.H = V_{IH}, L = V_{IL}, X = Don't care.

PIN DESCRIPTIONS

A0 – A16	Address Inputs	Input
$\overline{CS1}$	Chip Select	Input
CS2	Chip Select	Input
$\overline{WE}$	Write Enable	Input
$\overline{OE}$	Output Enable	Input
I/O0 - I/O7	Data Input/Output	I/O
VDD	Power	Pwr
VSS	Ground	Gnd

3778 tbl 01

CAPACITANCE

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	6	pF
CI/O	I/O Capacitance	VOUT = 3dV	7	pF

NOTE: 3778 tbl 06

1. This parameter is guaranteed by device characterization, but not production tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l. and Ind'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to V_{SS}	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to V_{SS}	–0.5 to V_{DD}+0.5V	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

3778 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. Input, Output,and I/O terminals; 4.6V maximum.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	Vss	V_{DD}
Commercial	0°C to +70°C	0V	2.7V to 3.6V
Industrial	-40°C to +85°C	0V	2.7V to 3.6V

3778 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	2.7	3.0	3.6	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{DD}+0.3(1)	V
V_{IL}	Input Low Voltage	–0.3(2)	—	0.8	V

3778 tbl 05

NOTE:
1. V_{IH} (max.) = V_{DD} + 1.5V for pulse width less than 5ns, once per cycle.
2. V_{IL} (min.) = –1.5V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7V to 3.6V, Commercial and Industrial Temperature Ranges

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = V_{SS} to V_{DD}	—	1	µA
$\|I_{LO}\|$	Output Leakage Current	V_{DD} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{DD}	—	1	µA
V_{OH}	Output High Voltage	I_{OH} = –1mA, V_{DD} = Min.	2.4	—	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA, V_{DD} = Min.	—	0.4	V

3778 tbl 07

DC ELECTRICAL CHARACTERISTICS(1, 2)

V_{DD} = 2.7 to 3.6V, V_{LC} = 0.2V, V_{HC} = V_{DD}–0.2V, Commercial and Industrial Temperature Ranges

Symbol	Parameter	Test Conditions		Typ.(5)	Max.	Unit
I_{CC2}	Dynamic Operating Current	$\overline{CS1}$ = V_{LC}, CS2 = V_{HC}, Outputs Open,	-70 ns	—	25	mA
		V_{DD} = 3.6V, f = f_{MAX}(3)	-100 ns	—	18	
I_{CC}	Static Operating Current	$\overline{CS1}$ = V_{LC}, CS2 = V_{HC}, Outputs Open, $\overline{WE}$ = V_{HC}, V_{DD} = 3.6V, f = 0(4)		—	5	mA
I_{SB1}	Standby Supply Current	$\overline{CS1}$ and CS2 = V_{HC}, or CS2 = V_{LC}, Outputs Open, V_{DD} = 3.6V	-40 to 85°C	—	10	µA
			0 to 70°C	—	5	
			40°C	—	2	
			25°C	—	1	

3778 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. Input low and high voltage levels are 0.2V and VDD-0.2V respectively for all tests.
3. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}).
4. f = 0 means no address input lines are changing .
5. Typical conditions are VDD = 3.0V and specified temperature.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

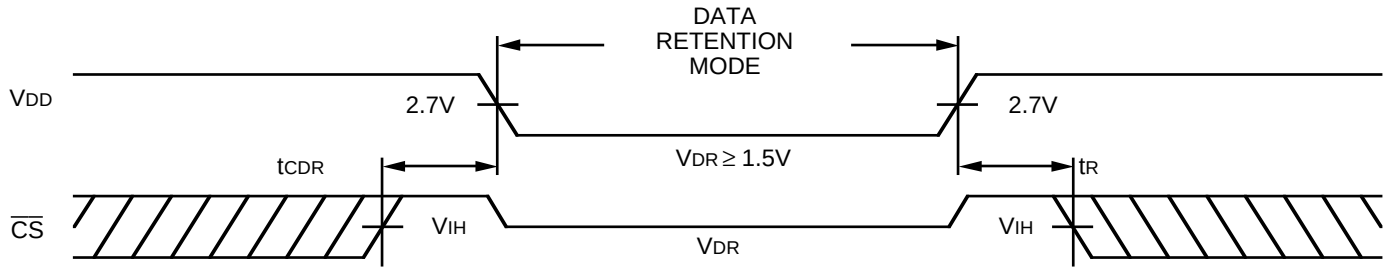
(V_{LC} = 0.2V, V_{HC} = V_{DD} - 0.2V)

Symbol	Parameter	Test Condition	Min.	Typ. [1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	—	1.5	—	—	V
I_{CCDR}	Data Retention Current	1) $\overline{CS1} \geq V_{HC}$ and CS2 ≥ V_{HC} or 2) CS2 ≤ VLC	—	<1	5	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0	—	—	ns
t_R[3]	Operation Recovery Time		t_{RC}[2]	—	—	ns

NOTES:
3778 tbl 09

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{DD} DATA RETENTION WAVEFORM



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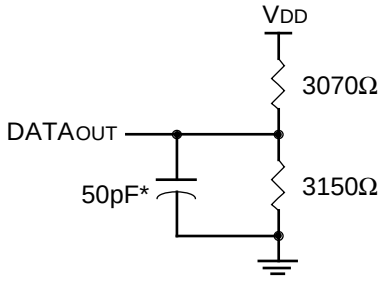
AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1

3778 tbl 10

AC TEST LOAD



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*Including jig and scope capacitance.

Figure 1. AC Test Load

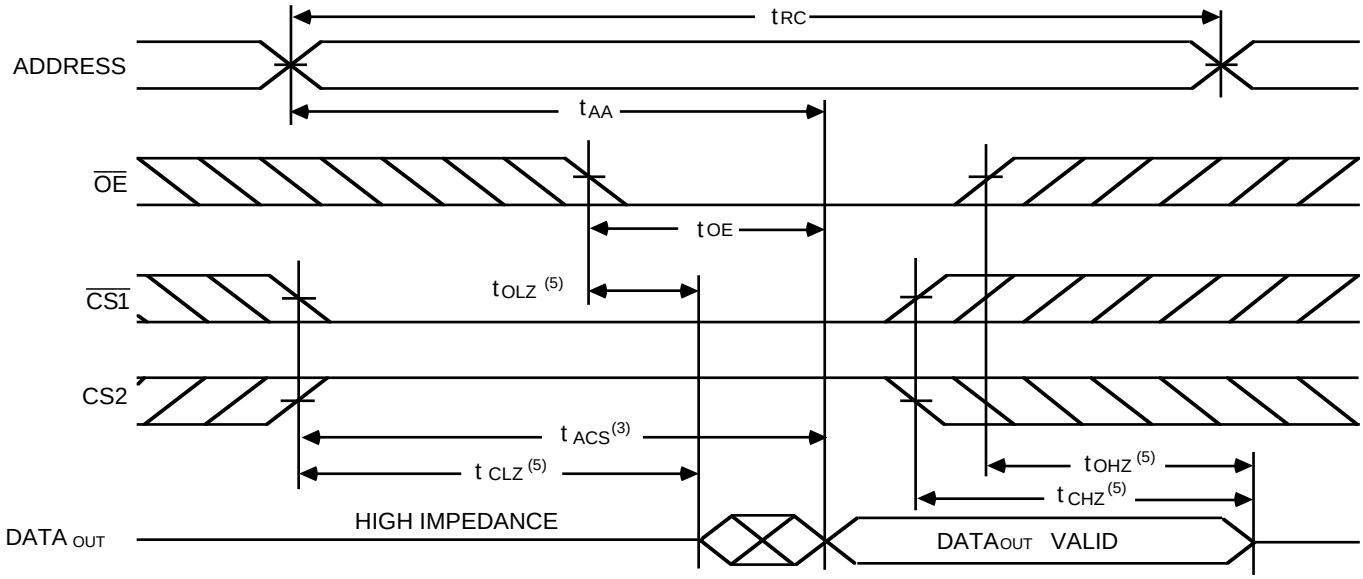
AC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.7 to 3.6V, All Temperature Ranges)

Symbol	Parameter	71L024L70		71L024L100		Units
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	70	—	100	—	ns
t_{AA}	Address Access Time	—	70	—	100	ns
t_{ACS}	Chip Select Access Time	—	70	—	100	ns
t_{CLZ}(1)	Chip Select Low to Output in Low-Z	10	—	10	—	ns
t_{CHZ}(1)	Chip Select High to Output in High-Z	—	25	—	30	ns
t_{OE}	Output Enable Low to Output Valid	—	35	—	50	ns
t_{OLZ}(1)	Output Enable Low to Output in Low-Z	5	—	5	—	ns
t_{OHZ}(1)	Output Enable High to Output in High-Z	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	10	—	15	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	70	—	100	—	ns
t_{AW}	Address Valid to End of Write	65	—	80	—	ns
t_{CW}	Chip Select Low to End of Write	65	—	80	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WR}	Address Hold from End of Write	0	—	0	—	ns
t_{WP}	Write Pulse Width	55	—	70	—	ns
t_{DW}	Data Valid to End of Write	30	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{OW}(1)	Write Enable High to Output in Low-Z	5	—	5	—	ns
t_{WHZ}(1)	Write Enable Low to Output in High-Z	—	25	—	30	ns

NOTE: 3778 tbl 11

1. This parameter is guaranteed by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



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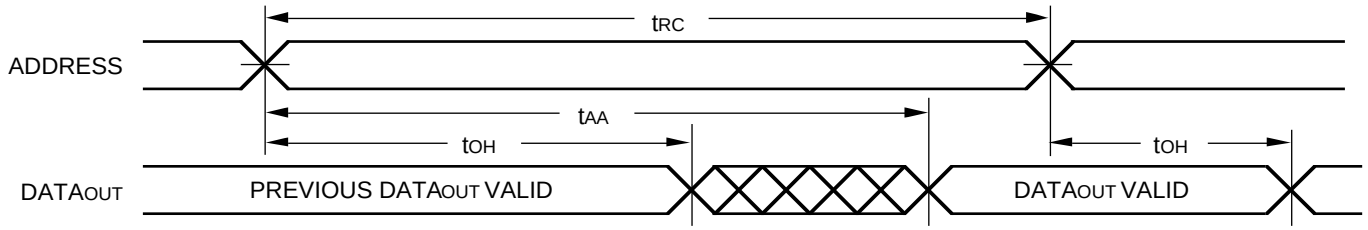
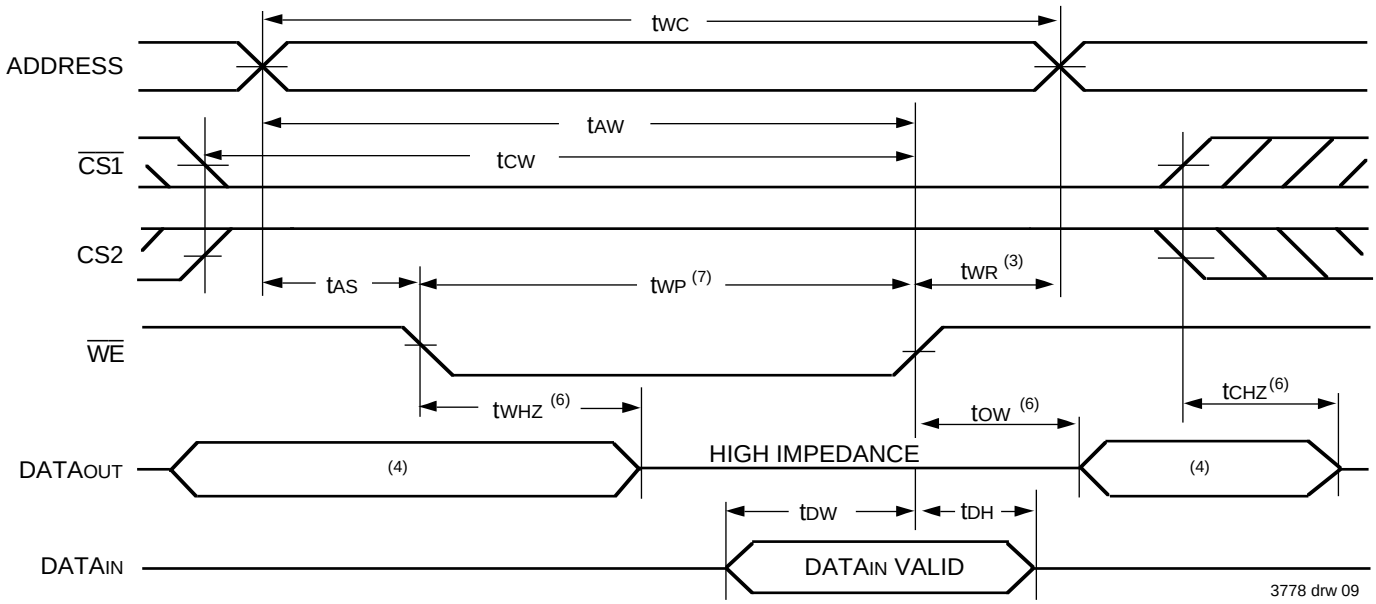
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



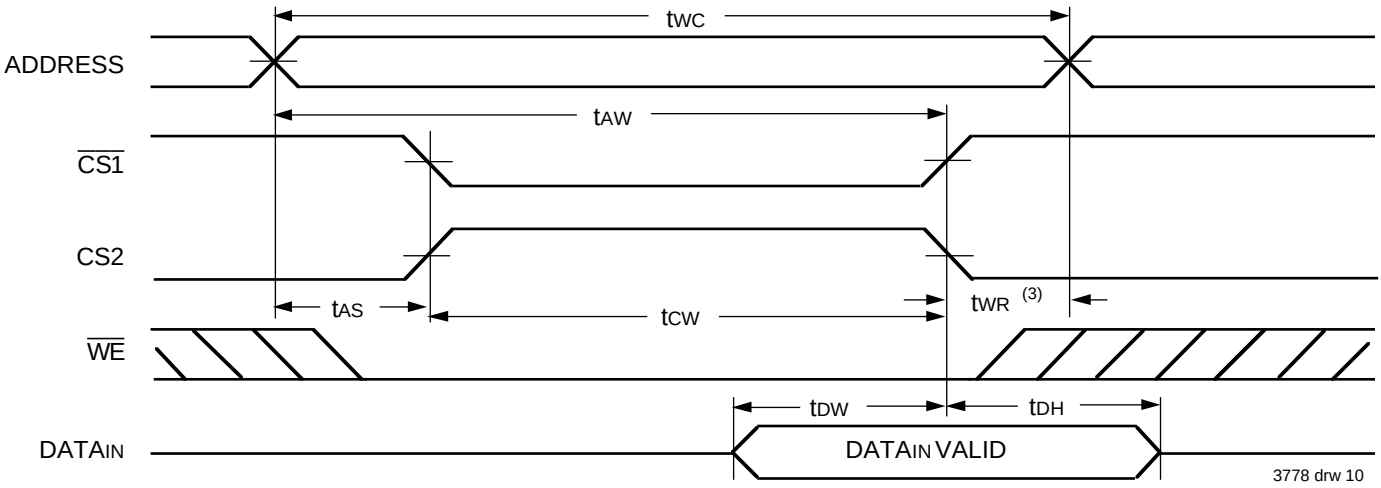
3778 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected; $\overline{CS1}$ is LOW and CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5)

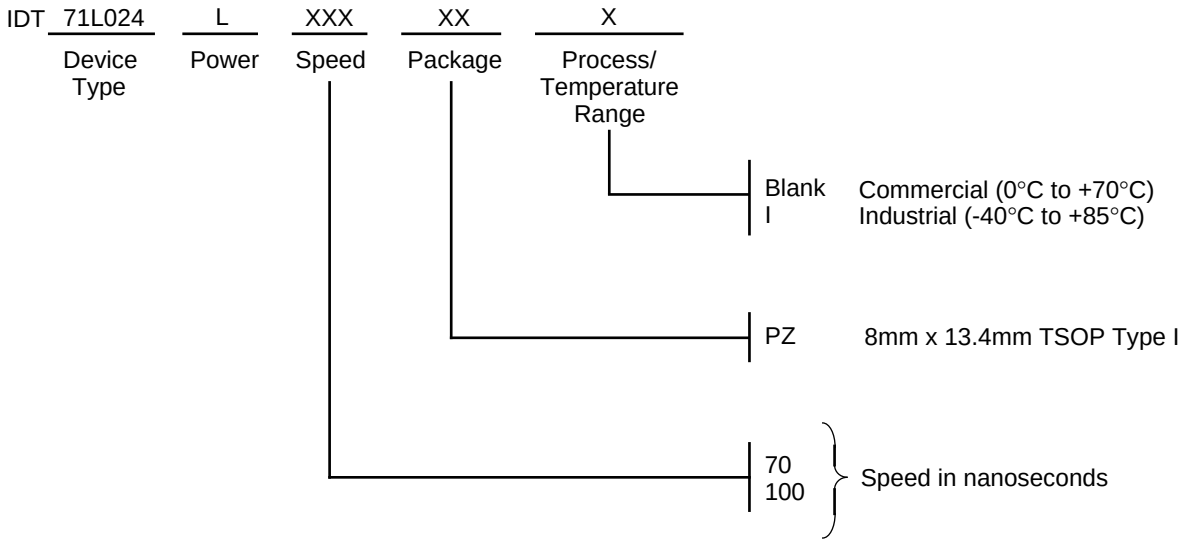


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of either $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS1}$ LOW transition or CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.

ORDERING INFORMATION



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