3.3 VOLT DUAL CMOS SyncFIFO™ DUAL 256 X 9, DUAL 512 X 9, DUAL 1,024 X 9, DUAL 2,048 X 9, DUAL 4,096 X 9 , DUAL 8,192 X 9

IDT72V801
IDT72V811
IDT72V821
IDT72V831
IDT72V841
IDT72V851

FEATURES:

- **The IDT72V801 is equivalent to two IDT72V201 256 x 9 FIFOs**
- **The IDT72V811 is equivalent to two IDT72V211 512 x 9 FIFOs**
- **The IDT72V821 is equivalent to two IDT72V221 1,024 x 9 FIFOs**
- **The IDT72V831 is equivalent to two IDT72V231 2,048 x 9 FIFOs**
- **The IDT72V841 is equivalent to two IDT72V241 4,096 x 9 FIFOs**
- **The IDT72V851 is equivalent to two IDT72V251 8,192 x 9 FIFOs**
- **Offers optimal combination of large capacity, high speed, design flexibility and small footprint**
- **Ideal for prioritization, bidirectional, and width expansion applications**
- **10 ns read/write cycle time**
- **5V input tolerant**
- **Separate control lines and data lines for each FIFO**
- **Separate Empty, Full, programmable Almost-Empty and Almost-Full flags for each FIFO**
- **Enable puts output data lines in high-impedance state**
- **Space-saving 64-pin plastic Thin Quad Flat Pack (TQFP/ STQFP)**
- **Industrial temperature range (–40°C to +85°C) is available**

DESCRIPTION:

The IDT72V801/72V811/72V821/72V831/72V841/72V851/72V851 are dual synchronous (clocked) FIFOs. The device is functionally equivalent to two IDT72V201/72V211/72V221/72V231/72V241/72V251 FIFOs in a single package with all associated control, data, and flag lines assigned to separate pins.

Each of the two FIFOs (designated FIFO A and FIFO B) contained in the IDT72V801/72V811/72V821/72V831/72V841/72V851 has a 9-bit input data port (DA0 - DA8, DB0 - DB8) and a 9-bit output data port (QA0 - QA8, QB0 - QB8). Each input port is controlled by a free-running clock (WCLKA, WCLKB), and two Write Enable pins ($\overline{WENA1}$, WENA2, $\overline{WENB1}$, WENB2). Data is written into each of the two arrays on every rising clock edge of the Write Clock (WCLKA, WCLKB) when the appropriate Write Enable pins are asserted.

The output port of each FIFO bank is controlled by its associated clock pin (RCLKA, RCLKB) and two Read Enable pins ($\overline{RENA1}$, $\overline{RENA2}$, $\overline{RENB1}$, $\overline{RENB2}$). The Read Clock can be tied to the Write Clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An Output Enable pin ($\overline{OEA}$, $\overline{OEB}$) is provided on the read port of each FIFO for three-state output control.

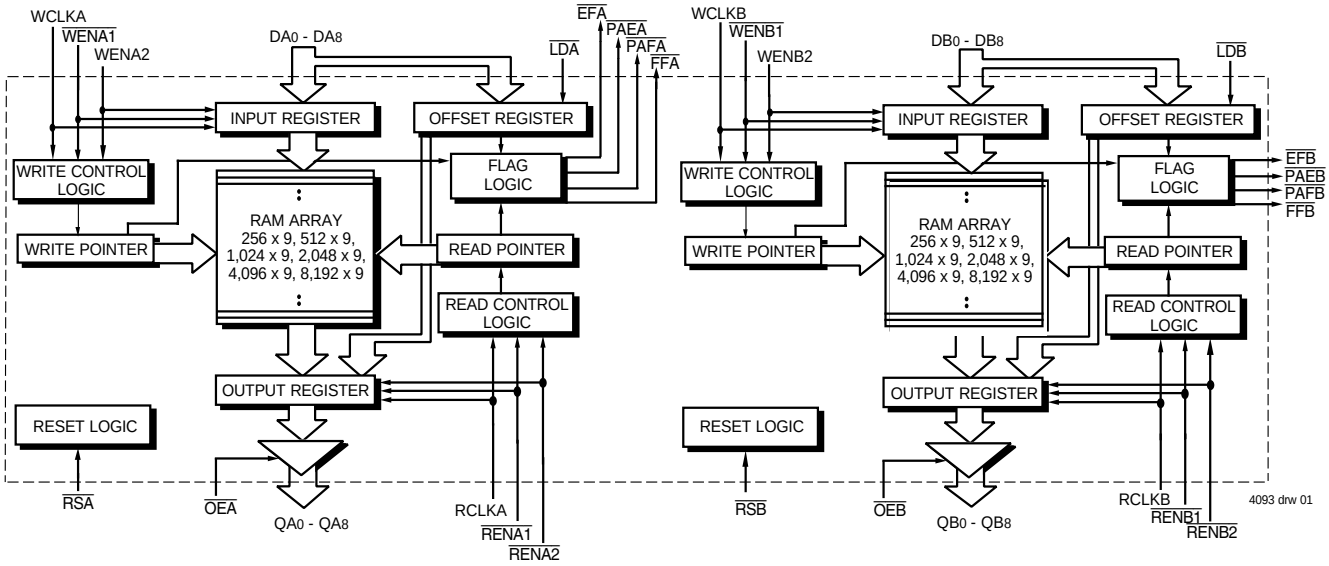
Each of the two FIFOs has two fixed flags, Empty ($\overline{EFA}$, $\overline{EFB}$) and Full ($\overline{FFA}$, $\overline{FFB}$). Two programmable flags, Almost-Empty ($\overline{PAEA}$, $\overline{PAEB}$) and Almost-Full ($\overline{PAFA}$, $\overline{PAFB}$), are provided for each FIFO bank to improve memory utilization. If not programmed, the programmable flags default to Empty+7 for $\overline{PAEA}$ and $\overline{PAEB}$, and Full-7 for $\overline{PAFA}$ and $\overline{PAFB}$.

The IDT72V801/72V811/72V821/72V831/72V841/72V851 architecture lends itself to many flexible configurations such as:

- 2-level priority data buffering
- Bidirectional operation
- Width expansion
- Depth expansion

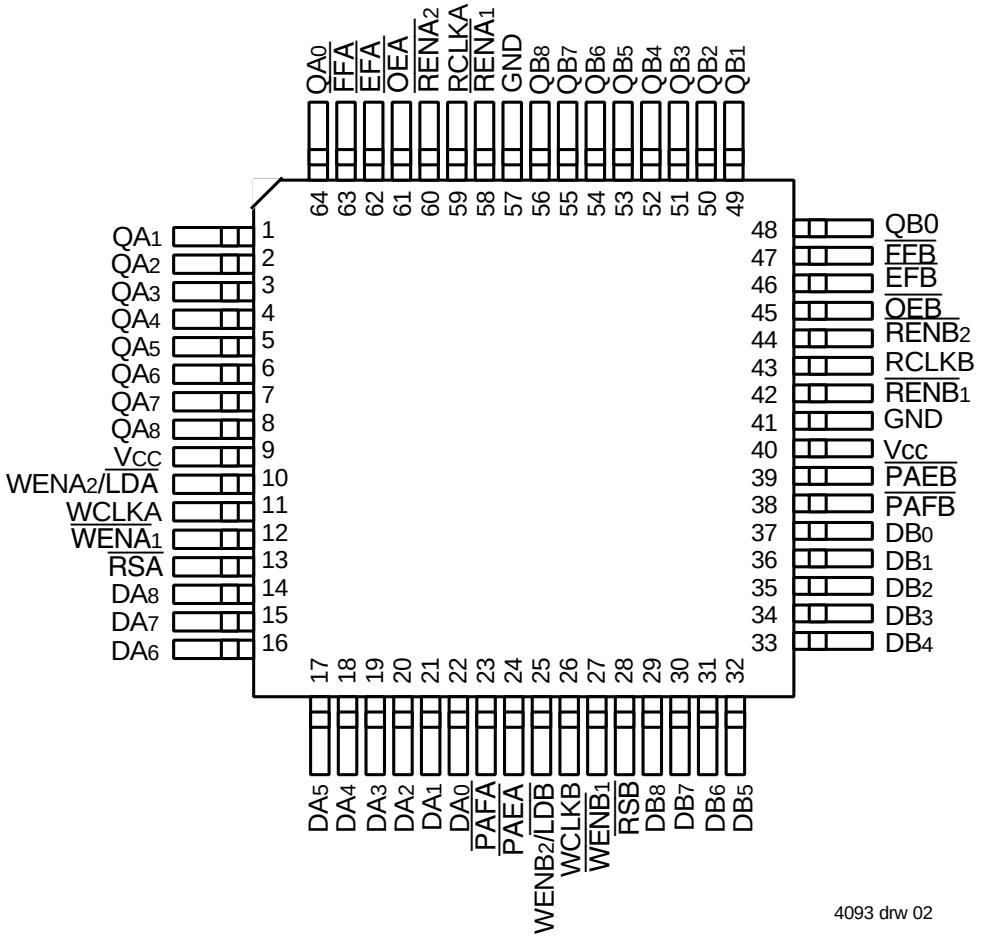
This FIFO is fabricated using IDT's high-performance submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark and the SyncFIFO is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



TQFP (PN64-1, order code: PF)
STQFP (PP64-1, order code: TF)
TOP VIEW

PIN DESCRIPTIONS

The IDT72V801/72V811/72V821/72V831/72V841/72V851's two FIFOs, referred to as FIFO A and FIFO B, are identical in every respect. The following description defines the input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

Symbol	Name I/O		Description
D_{A0}-D_{A8}	A Data Inputs	I	9-bit data inputs to RAM array A.
D_{B0}-D_{B8}	B Data Inputs	I	9-bit data inputs to RAM array B.
$\overline{RSA}$, $\overline{RSB}$	Reset	I	When $\overline{RSA}$ ($\overline{RSB}$) is set LOW, the associated internal read and write pointers of array A (B) are set to the first location; $\overline{FFA}$ ($\overline{FFB}$) and $\overline{PAFA}$ ($\overline{PAFB}$) go HIGH, and $\overline{PAEA}$ ($\overline{PAEB}$) and $\overline{EFA}$ ($\overline{EFB}$) go LOW. After power-up, a reset of both FIFOs A and B is required before an initial WRITE.
WCLKA WCLKB	Write Clock	I	Data is written into the FIFO A (B) on a LOW-to-HIGH transition of WCLKA (WCLKB) when the write enable(s) are asserted.
$\overline{WENA1}$ $\overline{WENB1}$	Write Enable 1	I	If FIFO A (B) is configured to have programmable flags, $\overline{WENA1}$ ($\overline{WENB1}$) is the only write enable pin that can be used. When $\overline{WENA1}$ ($\overline{WENB1}$) is LOW, data A (B) is written into the FIFO on every LOW-to-HIGH transition WCLKA (WCLKB). If the FIFO is configured to have two write enables, $\overline{WENA1}$ ($\overline{WENB1}$) must be LOW and WENA2 (WENB2) must be HIGH to write data into the FIFO. Data will not be written into the FIFO if $\overline{FFA}$ ($\overline{FFB}$) is LOW.
WENA2/$\overline{LDA}$ WENB2/$\overline{LDB}$	Write Enable 2/ Load	I	FIFO A (B) is configured at reset to have either two write enables or programmable flags. If $\overline{LDA}$ ($\overline{LDB}$) is HIGH at reset, this pin operates as a second Write Enable. If WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) is LOW at reset this pin operates as a control to load and read the programmable flag offsets for its respective array. If the FIFO is configured to have two write enables, $\overline{WENA1}$ ($\overline{WENB1}$) must be LOW and WENA2 (WENB2) must be HIGH to write data into FIFO A (B). Data will not be written into FIFO A (B) if $\overline{FFA}$ ($\overline{FFB}$) is LOW. If the FIFO is configured to have programmable flags, $\overline{LDA}$ ($\overline{LDB}$) is held LOW to write or read the programmable flag offsets.
Q_{A0}-Q_{A8}	A Data Outputs	O	9-bit data outputs from RAM array A.
Q_{B0}-Q_{B8}	B Data Outputs	O	9-bit data outputs from RAM array B.
RCLKA RCLKB	Read Clock	I	Data is read from FIFO A (B) on a LOW-to-HIGH transition of RCLKA (RCLKB) when $\overline{RENA1}$($\overline{RENB1}$) and $\overline{RENA2}$ ($\overline{RENB2}$) are asserted.
$\overline{RENA1}$ $\overline{RENB1}$	Read Enable 1	I	When $\overline{RENA1}$ ($\overline{RENB1}$) and $\overline{RENA2}$ ($\overline{RENB2}$) are LOW, data is read from FIFO A (B) on every LOW-to-HIGH transition of RCLKA (RCLKB). Data will not be read from Array A (B) if $\overline{EFA}$ ($\overline{EFB}$) is LOW.
$\overline{RENA2}$ $\overline{RENB2}$	Read Enable 2	I	When $\overline{RENA1}$ ($\overline{RENB1}$) and $\overline{RENA2}$ ($\overline{RENB2}$) are LOW, data is read from the FIFO A (B) on every LOW-to-HIGH transition of RCLKA (RCLKB). Data will not be read from array A (B) if the $\overline{EFA}$ (EFB) is LOW.
$\overline{OEA}$	Output Enable	I	When $\overline{OEA}$ ($\overline{OEB}$) is LOW, outputs D_{A0}-D_{A8} (D_{B0}-D_{B8}) are active. If $\overline{OEA}$ ($\overline{OEB}$) is HIGH, the $\overline{OEB}$ outputs D_{A0}-D_{A8} (D_{B0}-D_{B8}) will be in a high-impedance state.
$\overline{EFA}$ $\overline{EFB}$	Empty Flag	O	When $\overline{EFA}$ ($\overline{EFB}$) is LOW, FIFO A (B) is empty and further data reads from the output are inhibited. When $\overline{EFA}$ ($\overline{EFB}$) is HIGH, FIFO A (B) is not empty. $\overline{EFA}$ ($\overline{EFB}$) is synchronized to RCLKA (RCLKB).
$\overline{PAEA}$ $\overline{PAEB}$	Programmable Almost-Empty Flag	O	When $\overline{PAEA}$ ($\overline{PAEB}$) is LOW, FIFO A (B) is Almost-Empty based on the offset programmed into the appropriate offset register. The default offset at reset is Empty+7. $\overline{PAEA}$ ($\overline{PAEB}$) is synchronized to RCLKA (RCLKB).
$\overline{PAFA}$ $\overline{PAFB}$	Programmable Almost-Full Flag	O	When $\overline{PAFA}$ ($\overline{PAFB}$) is LOW, FIFO A (B) is Almost-Full based on the offset programmed into the appropriate offset register. The default offset at reset is Full-7. $\overline{PAFA}$ ($\overline{PAFB}$) is synchronized to WCLKA (WCLKB).
$\overline{FFA}$ $\overline{FFB}$	Full Flag	O	When $\overline{FFA}$ ($\overline{FFB}$) is LOW, FIFO A (B) is full and further data writes into the input are inhibited. When $\overline{FFA}$ ($\overline{FFB}$) is HIGH, FIFO A (B) is not full. $\overline{FFA}$ ($\overline{FFB}$) is synchronized to WCLKA (WCLKB).
V_{CC}	Power		+3.3V power supply pin.
GND	Ground		0V ground pin.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +5	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ.	Max	Unit
V_{CC}	Supply Voltage(Com'l & Ind'l)	3.0	3.3	3.6	V
GND	Supply Voltage(Com'l & Ind'l)	0	0	—	V
V_{IH}	Input High Voltage (Com'l & Ind'l)	2.0	—	5.0	V
V_{IL}	Input Low Voltage (Com'l & Ind'l)	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C
T_A	Operating Temperature Industrial	-40	—	85	°C

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C; Industrial :V_{CC} = 3.3V ± 0.3V, TA = -40°C to +85°C)

Symbol	Parameter	IDT72V801 IDT72V811 IDT72V821 IDT72V831 IDT72V841 IDT72V851 Commercial and Industrial [1] t_{CLK} = 10, 15, 20 ns Min.	Typ.	Max.	Unit
I_{LI}[2]	Input Leakage Current (Any Input)	–1	—	–1	µA
I_{LO}[3]	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	V
I_{CC1}[4,5,6]	Active Power Supply Current (both FIFOs)	—	—	40	mA
I_{CC2}[3,7]	Standby Current	—	—	10	mA

NOTES:
1. Industrial temperature range product for the 15ns speed grade is available as a standard device.
2. Measurements with $0.4 \le V_{IN} \le V_{CC}$.
3. OEA, OEB $\ge V_{IH}$, $0.4 \le V_{OUT} \le V_{CC}$.
4. Tested with outputs disabled (I_{OUT} = 0).
5. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
6. Typical I_{CC1} = 2[0.17 + 0.48*fs + 0.02*C_L*fs] (in mA).
   These equations are valid under the following conditions:
   V_{CC} = 3.3V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
7. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}[2]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE:
1. With output deselected ($\overline{OEA}$, $\overline{OEB} \ge V_{IH}$).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS(1)

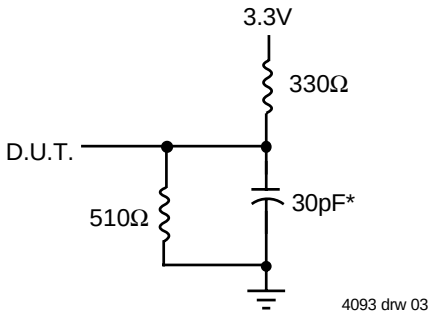
(Commercial: V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C; Industrial: V_{CC} = 3.3V± 0.3V, T_A = -40°C to +85°C)

Symbol	Parameter	Commercial IDT72V801L10 IDT72V811L10 IDT72V821L10 IDT72V831L10 IDT72V841L10 IDT72V851L10		Com'l & Ind'l IDT72V801L15 IDT72V811L15 IDT72V821L15 IDT72V831L15 IDT72V841L15 IDT72V851L15		Commercial IDT72V801L20 IDT72V811L20 IDT72V821L20 IDT72V831L20 IDT72V841L20 IDT72V851L20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Cycle Frequency	—	100	—	66.7	—	50	MHz
tA	Data Access Time	2	6.5	2	10	2	12	ns
tCLK	Clock Cycle Time	10	—	15(1)	—	20	—	ns
tCLKH	Clock High Time	4.5	—	6	—	8	—	ns
tCLKL	Clock Low Time	4.5	—	6	—	8	—	ns
tDS	Data Set-up Time	3	—	4	—	5	—	ns
tDH	Data Hold Time	0.5	—	1	—	1	—	ns
tENS	Enable Set-up Time	3	—	4	—	5	—	ns
tENH	Enable Hold Time	0.5	—	1	—	1	—	ns
tRS	Reset Pulse Width(2)	10	—	15	—	20	—	ns
tRSS	Reset Set-up Time	8	—	10	—	12	—	ns
tRSR	Reset Recovery Time	8	—	10	—	12	—	ns
tRSF	Reset to Flag Time and Output Time	—	10	—	15	—	20	ns
tOLZ	Output Enable to Output in Low-Z(3)	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	6	3	8	3	10	ns
tOHZ	Output Enable to Output in High-Z(3)	3	6	3	8	3	10	ns
tWFF	Write Clock to Full Flag	—	6.5	—	10	—	12	ns
tREF	Read Clock to Empty Flag	—	6.5	—	10	—	12	ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	6.5	—	10	—	12	ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	6.5	—	10	—	12	ns
tSKEW1	Skew Time Between Read Clock and Write Clock for Empty Flag and Full Flag	5	—	6	—	8	—	ns
tSKEW2	Skew Time Between Read Clock and Write Clock for Programmable Almost-Empty Flag and Programmable Almost-Full Flag	14	—	18	—	20	—	ns

NOTES:
1. Industrial temperature range product for the 15ns speed grade is available as a standard device.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

FIFO A and FIFO B are identical in every respect. The following description explains the interaction of input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

INPUTS:

Data In ($D_{A0} - D_{A8}$, $D_{B0} - D_{B8}$) — D_{A0} - D_{A8} are the nine data inputs for memory array A. D_{B0} - D_{B8} are the nine data inputs for memory array B.

CONTROLS:

Reset ($\overline{RSA}$, $\overline{RSB}$) — Reset of FIFO A (B) is accomplished whenever $\overline{RSA}$ ($\overline{RSB}$) input is taken to a LOW state. During reset, the internal read and write pointers associated with the FIFO are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag, $\overline{FFA}$ ($\overline{FFB}$) and Programmable Almost-Full Flag, $\overline{PAFA}$ ($\overline{PAFB}$) will be reset to HIGH after t_{RSF}. The Empty Flag, $\overline{EFA}$ ($\overline{EFB}$) and Programmable Almost-Empty Flag, $\overline{PAEA}$ ($\overline{PAEB}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLKA, WCLKB) — A write cycle to Array A (B) is initiated on the LOW-to-HIGH transition of WCLKA (WCLKB). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of WCLKA (WCLKB). The Full Flag, $\overline{FFA}$ ($\overline{FFB}$) and Programmable Almost-Full Flag, $\overline{PAFA}$ ($\overline{PAFB}$) are synchronized with respect to the LOW-to-HIGH transition of the Write Clock, WCLKA (WCLKB).

The Write and Read clock can be asynchronous or coincident.

Write Enable 1 ($\overline{WENA1}$, $\overline{WENB1}$) — If FIFO A (B) is configured for programmable flags, $\overline{WENA1}$ ($\overline{WENB1}$) is the only enable control pin. In this configuration, when $\overline{WENA1}$ ($\overline{WENB1}$) is LOW, data can be loaded into the input register of RAM Array A (B) on the LOW-to-HIGH transition of every Write Clock, WCLKA (WCLKB). Data is stored in Array A (B) sequentially and independently of any on-going read operation.

In this configuration, when $\overline{WENA1}$ ($\overline{WENB1}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, $\overline{FFA}$ ($\overline{FFB}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the $\overline{FFA}$ ($\overline{FFB}$) will go HIGH after t_{WFF}, allowing a valid write to begin. $\overline{WENA1}$ ($\overline{WENB1}$) is ignored when FIFO A (B) is full.

Read Clock (RCLKA, RCLKB) — Data can be read from Array A (B) on the LOW-to-HIGH transition of RCLKA (RCLKB). The Empty Flag, $\overline{EFA}$ ($\overline{EFB}$) and Programmable Almost-Empty Flag, $\overline{PAEA}$ ($\overline{PAEB}$) are synchronized with respect to the LOW-to-HIGH transition of RCLKA (RCLKB).

The Write and Read Clock can be asynchronous or coincident.

Read Enables ($\overline{RENA1}$, $\overline{RENA2}$, $\overline{RENB1}$, $\overline{RENB2}$) — When both Read Enables, $\overline{RENA1}$, $\overline{RENA2}$ ($\overline{RENB1}$, $\overline{RENB2}$) are LOW, data is read from Array A (B) to the output register on the LOW-to-HIGH transition of the Read Clock, RCLKA (RCLKB).

When either of the two Read Enable, $\overline{RENA1}$, $\overline{RENA2}$ ($\overline{RENB1}$, $\overline{RENB2}$) associated with FIFO A (B) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from FIFO A (B), the Empty Flag, $\overline{EFA}$ ($\overline{EFB}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, $\overline{EFA}$ ($\overline{EFB}$) will go HIGH after t_{REF} and a valid read can begin. The Read Enables, $\overline{RENA1}$, $\overline{RENA2}$ ($\overline{RENB1}$, $\overline{RENB2}$) are ignored when FIFO A (B) is empty.

Output Enable ($\overline{OEA}$, $\overline{OEB}$) — When Output Enable, $\overline{OEA}$ ($\overline{OEB}$) is enabled (LOW), the parallel output buffers of FIFO A (B) receive data from their respective output register. When Output Enable, $\overline{OEA}$ ($\overline{OEB}$) is disabled (HIGH), the QA (QB) output data bus is in a high-impedance state.

Write Enable 2/Load (WENA2/$\overline{LDA}$, WENB2/$\overline{LDB}$) — This is a dual-purpose pin. FIFO A (B) is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) is set HIGH at Reset, $\overline{RSA}$ = LOW ($\overline{RSB}$ = LOW), this pin operates as a second Write Enable pin.

If FIFO A (B) is configured to have two write enables, when Write Enable 1, $\overline{WENA1}$ ($\overline{WENB1}$) is LOW and WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write Clock, WCLKA (WCLKB). Data is stored in the array sequentially and independently of any on-going read operation.

In this configuration, when $\overline{WENA1}$ ($\overline{WENB1}$) is HIGH and/or WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) is LOW, the input register of Array A holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag, $\overline{FFA}$ ($\overline{FFB}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FFA}$ ($\overline{FFB}$) will go HIGH after t_{WFF}, allowing a valid write to begin. $\overline{WENA1}$, ($\overline{WENB1}$) and WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) are ignored when the FIFO is full.

FIFO A (B) is configured to have programmable flags when the WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) is set LOW at Reset, $\overline{RSA}$ = LOW ($\overline{RSB}$ = LOW). Each FIFO

$\overline{LDA}$	$\overline{WENA1}$	WCLKA	OPERATION ON FIFO A
$\overline{LDB}$	$\overline{WENB1}$	WCLKB	OPERATION ON FIFO B
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

NOTE: 4093 tbl 08

1. For the purposes of this table, WENA2 and WENB2 = V_{IH}.
2. The same selection sequence applies to reading from the registers. $\overline{RENA1}$ and $\overline{RENA2}$ ($\overline{RENB1}$ and $\overline{RENB2}$) are enabled and read is performed on the LOW-to-HIGH transition of RCLKA (RCLKB).

Figure 2. Writing to Offset Registers for FIFOs A and B

contains four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

If FIFO A (B) is configured to have programmable flags, when the $\overline{WENA1}$ ($\overline{WENB1}$) and WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) are set LOW, data on the DA (DB) inputs are written into the Empty (Least Significant Bit) Offset register on the first LOW-to-HIGH transition of the WCLKA (WCLKB). Data are written into the Empty (Most Significant Bit) Offset register on the second LOW-to-HIGH transition of WCLKA (WCLKB), into the Full (Least Significant Bit) Offset register on the third transition, and into the Full (Most Significant Bit) Offset register on the fourth transition. The fifth transition of WCLKA (WCLKB) again writes to the Empty (Least Significant Bit) Offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing $\overline{LDA}$ ($\overline{LDB}$) HIGH, FIFO A (B) is returned to normal read/write operation. When $\overline{LDA}$ ($\overline{LDB}$) is set LOW, and $\overline{WENA1}$ ($\overline{WENB1}$) is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the QA (QB) outputs when WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) is set LOW and both Read Enables $\overline{RENA1}$, $\overline{RENA2}$ ($\overline{RENB1}$, $\overline{RENB2}$) are set LOW. Data can be read on the LOW-to-HIGH transition of the Read Clock RCLKA (RCLKB).

A read and write should not be performed simultaneously to the offset registers.

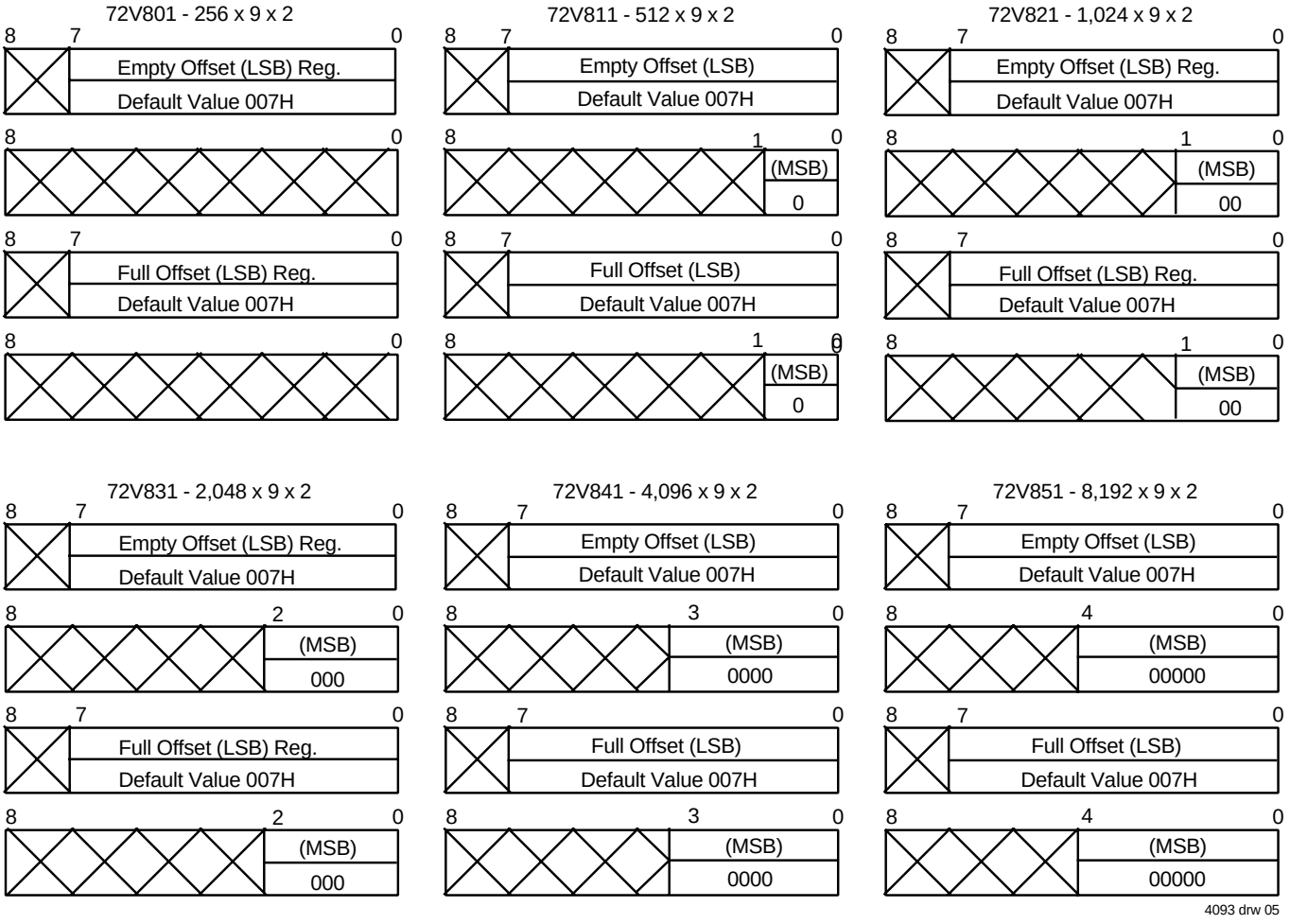


Figure 3. Offset Register Formats and Default Values for the A and B FIFOs

OUTPUTS:

Full Flag ($\overline{FFA}$, $\overline{FFB}$) — $\overline{FFA}$ ($\overline{FFB}$) will go LOW, inhibiting further write operations, when Array A (B) is full. If no reads are performed after reset, $\overline{FFA}$ ($\overline{FFB}$) will go LOW after 256 writes to the IDT72V801's FIFO A (B), 512 writes to the IDT72V811's FIFO A (B), 1,024 writes to the IDT72V821's FIFO A (B), 2,048 writes to the IDT72V831's FIFO A (B), 4,096 writes to the IDT72V841's FIFO A (B), or 8,192 writes to the IDT72V851's FIFO A (B).

$\overline{FFA}$ ($\overline{FFB}$) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock WCLKA (WCLKB).

Empty Flag ($\overline{EFA}$, $\overline{EFB}$) — $\overline{EFA}$ ($\overline{EFB}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that Array A (B) is empty.

$\overline{EFA}$ ($\overline{EFB}$) is synchronized with respect to the LOW-to-HIGH transition of the Read Clock RCLKA (RCLKB).

Programmable Almost–Full Flag ($\overline{PAFA}$, $\overline{PAFB}$) — $\overline{PAFA}$ ($\overline{PAFB}$) will go LOW when the amount of data in Array A (B) reaches the Almost-Full condition. If no reads are performed after reset, $\overline{PAFA}$ ($\overline{PAFB}$) will go LOW after (256-m) writes to the IDT72V801's FIFO A (B), (512-m) writes to the IDT72V811's FIFO A (B), (1,024-m) writes to the IDT72V821's FIFO A (B), (2,048-m) writes to the IDT72V831's FIFO A (B), (4,096-m) writes to the IDT72V841's FIFO A (B), or (8,1912-m) writes to the IDT72V851's FIFO A (B).

$\overline{FFA}$ ($\overline{FFB}$) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock WCLKA (WCLKB). The offset "m" is defined in the Full Offset Registers.

If there is no Full offset specified, $\overline{PAFA}$ ($\overline{PAFB}$) will go LOW at Full-7 words.

$\overline{PAFA}$ ($\overline{PAFB}$) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock WCLKA (WCLKB).

Programmable Almost–Empty Flag ($\overline{PAEA}$, $\overline{PAEB}$) — $\overline{PAEA}$ ($\overline{PAEB}$) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty Offset Registers. If no reads are performed after reset, $\overline{PAEA}$ ($\overline{PAEB}$) will go HIGH after "n+1" writes to FIFO A (B).

If there is no Empty offset specified, $\overline{PAEA}$ ($\overline{PAEB}$) will go LOW at Empty+7 words.

$\overline{PAEA}$ ($\overline{PAEB}$) is synchronized with respect to the LOW-to-HIGH transition of the Read Clock RCLKA (RCLKB).

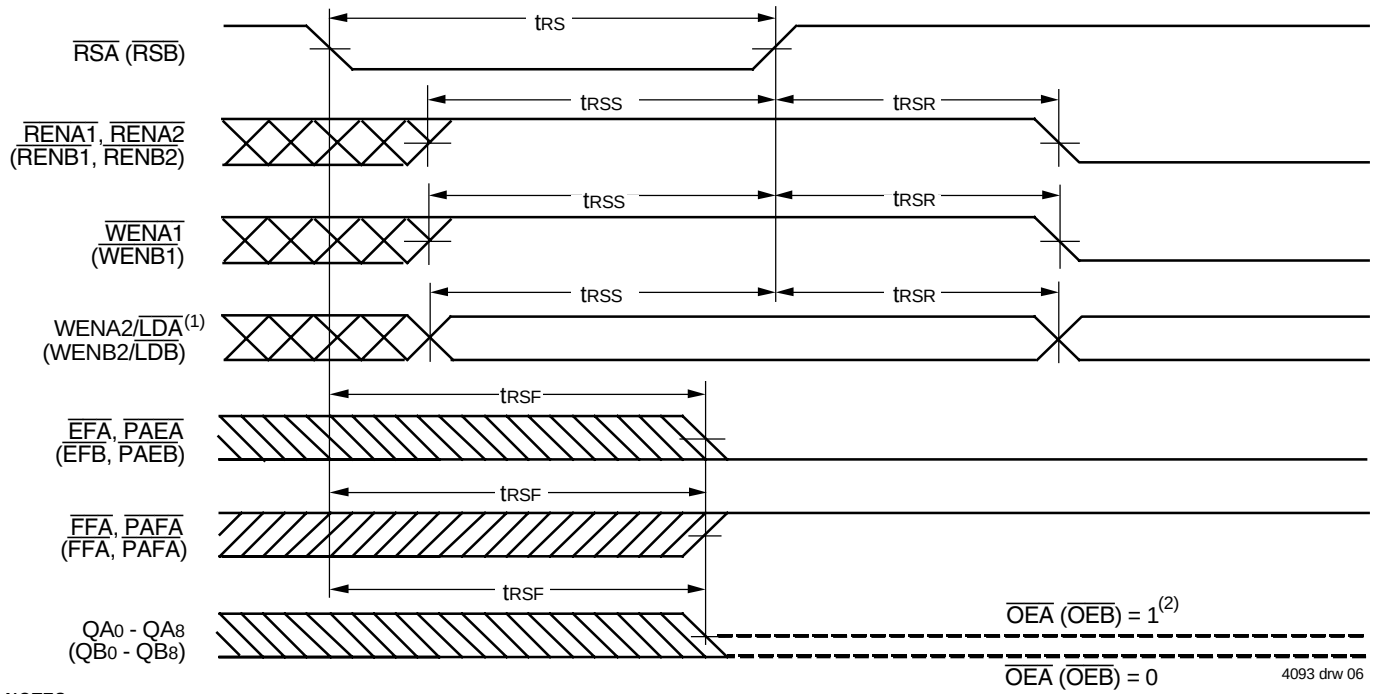
Data Outputs ($QA_0 – QA_8$, $QB_0 – QB_8$) — QA_0 - QA_8 are the nine data outputs for memory array A, QB_0 - QB_8 are the nine data outputs for memory array B.

TABLE 1: STATUS FLAGS FOR A AND B FIFOS

NUMBER OF WORDS IN ARRAY A			$\overline{FFA}$	$\overline{PAFA}$	$\overline{PAEA}$	$\overline{EFA}$
NUMBER OF WORDS IN ARRAY B			$\overline{FFB}$	$\overline{PAFB}$	$\overline{PAEB}$	$\overline{EFB}$
IDT72V801	IDT72V811	IDT72V821				
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	(n+1) to (1,024-(m+1))	H	H	H	H
(256-m)[2] to 255	(512-m)[2] to 511	(1,024-m)[2] to 1,023	H	L	H	H
256	512	1,024	L	L	H	H

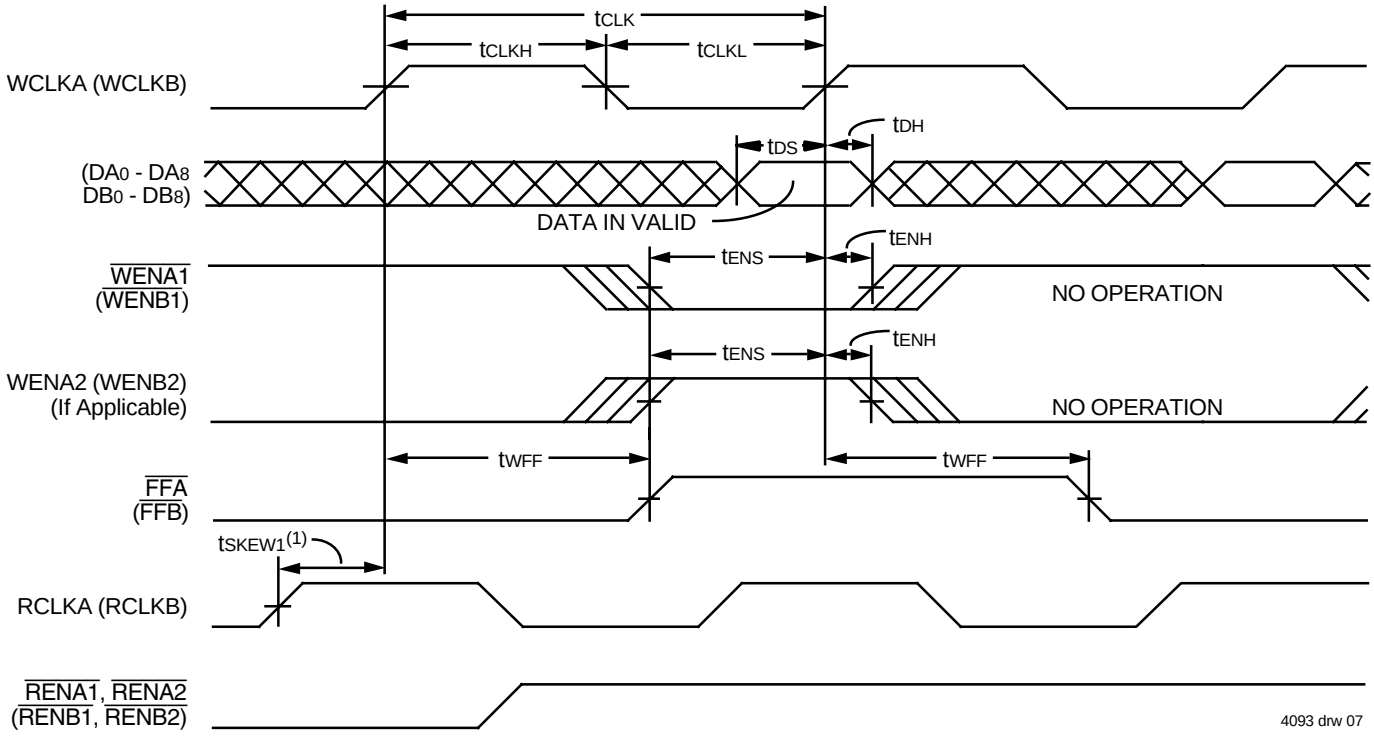
NUMBER OF WORDS IN ARRAY A			$\overline{FFA}$	$\overline{PAFA}$	$\overline{PAEA}$	$\overline{EFA}$
NUMBER OF WORDS IN ARRAY B			$\overline{FFB}$	$\overline{PAFB}$	$\overline{PAEB}$	$\overline{EFB}$
IDT72V831	IDT72V841	IDT72V851				
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (2,048-(m+1))	(n+1) to (4,096-(m+1))	(n+1) to (8,192-(m+1))	H	H	H	H
(2,048-m)[2] to 2,047	(4,096-m)[2] to 4,095	(8,192-m)[2] to 8,191	H	L	H	H
2,048	4,096	8,192	L	L	H	H

NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)



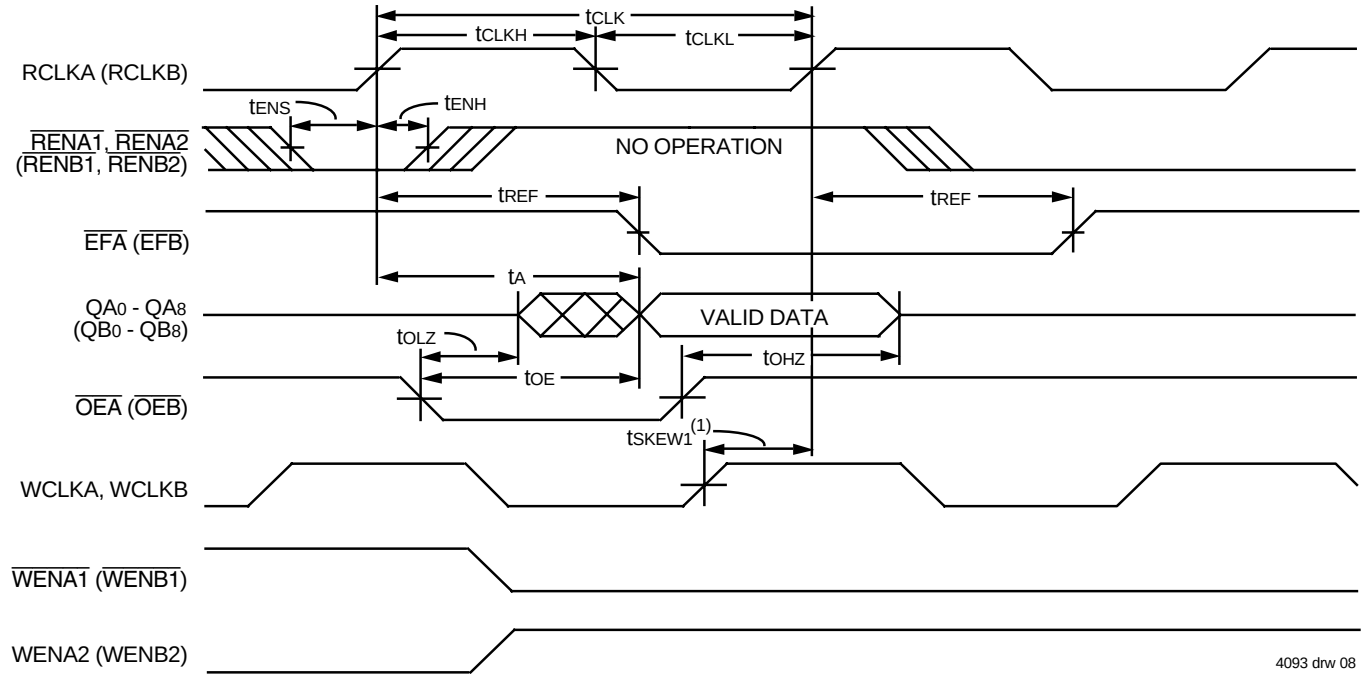
NOTES:
1. Holding WENA2/LDA (WENB2/LDB) HIGH during reset will make the pin act as a second Write Enable pin. Holding WENA2/LDA (WENB2/LDB) LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, QA_0 - QA_8 (QB_0 - QB_8) will be LOW if OEA (OEB) = 0 and tri-state if OEA (OEB) = 1.
3. The clocks RCLKA, WCLKA (RCLKB, WCLKB) can be free-running during reset.

Figure 4. Reset Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for FFA (FFB) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW1}, then FFA (FFB) may not change state until the next WCLKA (WCLKB) edge.

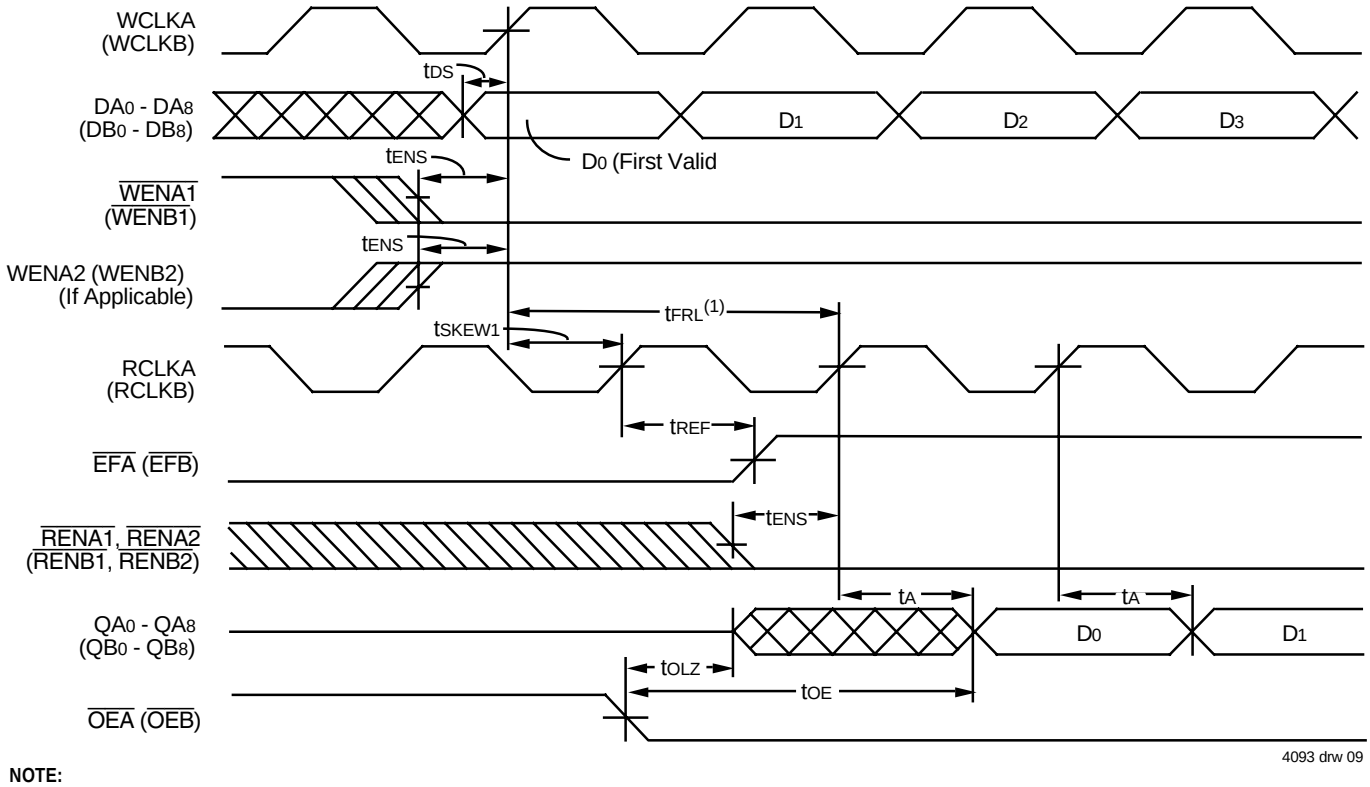
Figure 5. Write Cycle Timing



NOTE:

1. t_{SKEW1} is the minimum time between a rising WCLKA (WCLKB) edge and a rising RCLKA (RCLKB) edge for $\overline{EFA}$ ($\overline{EFB}$) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW1}, then $\overline{EFA}$ ($\overline{EFB}$) may not change state until the next RCLKA (RCLKB) edge.

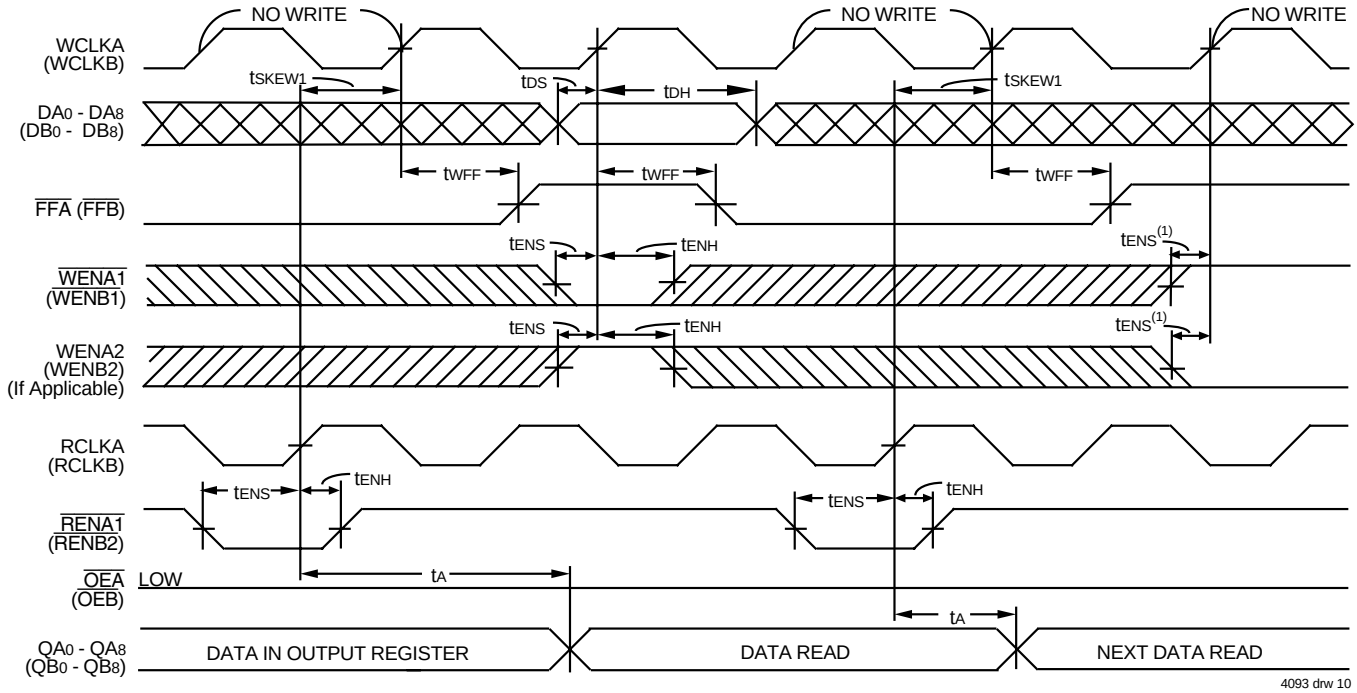
Figure 6. Read Cycle Timing



NOTE:

1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EFA}$, $\overline{EFB}$ = LOW).

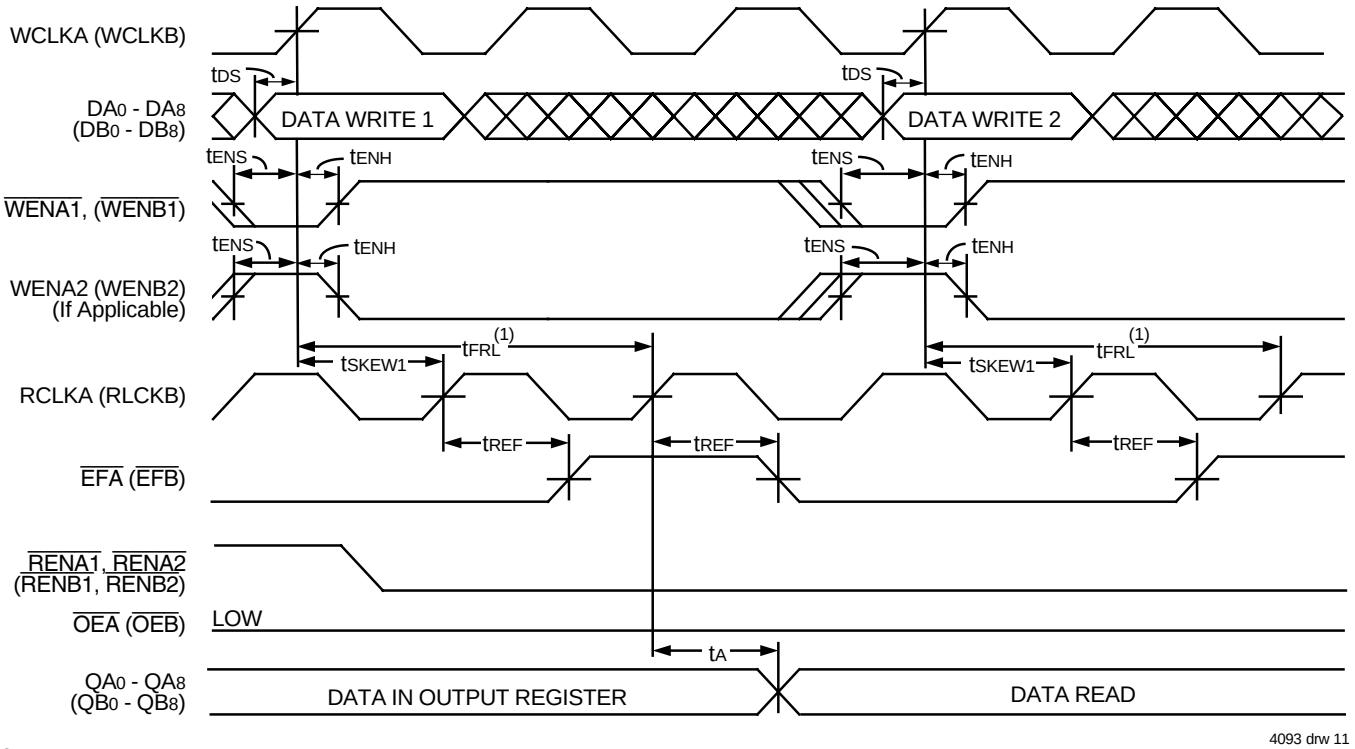
Figure 7. First Data Word Latency Timing



4093 drw 10

NOTE:
1. Only one of the two Write Enable inputs, $\overline{WEN1}$ or $\overline{WEN2}$, needs to go inactive to inhibit writes to the FIFO.

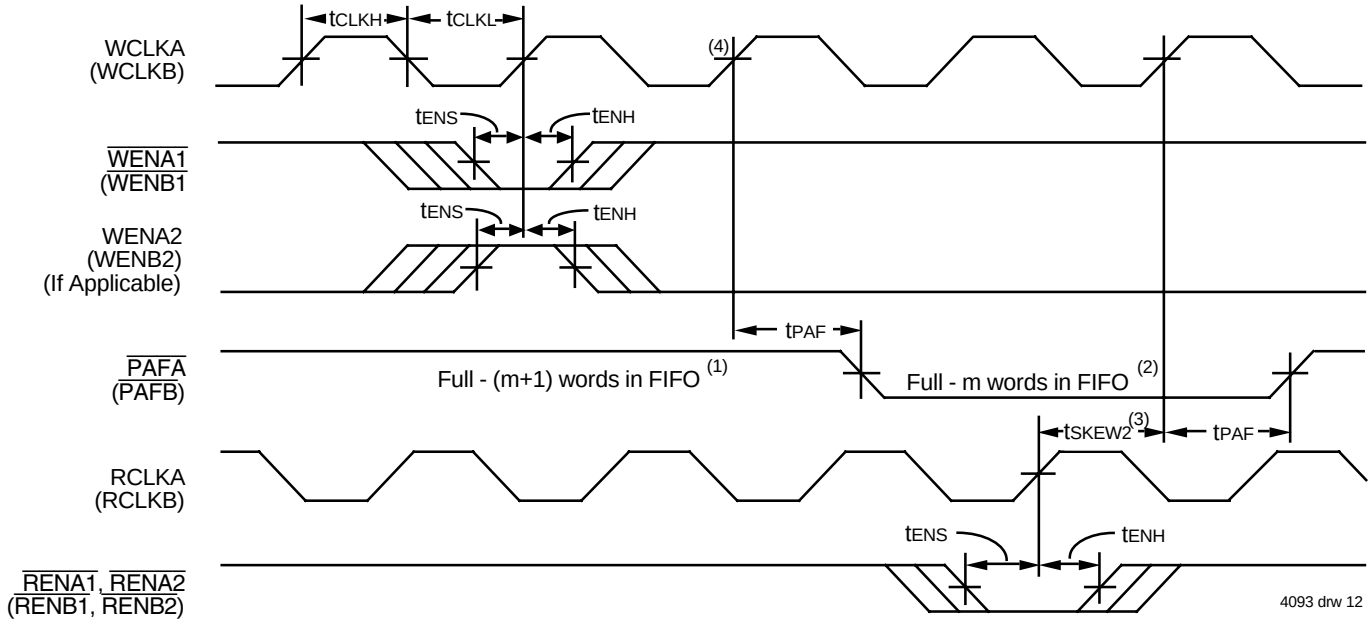
Figure 8. Full Flag Timing



4093 drw 11

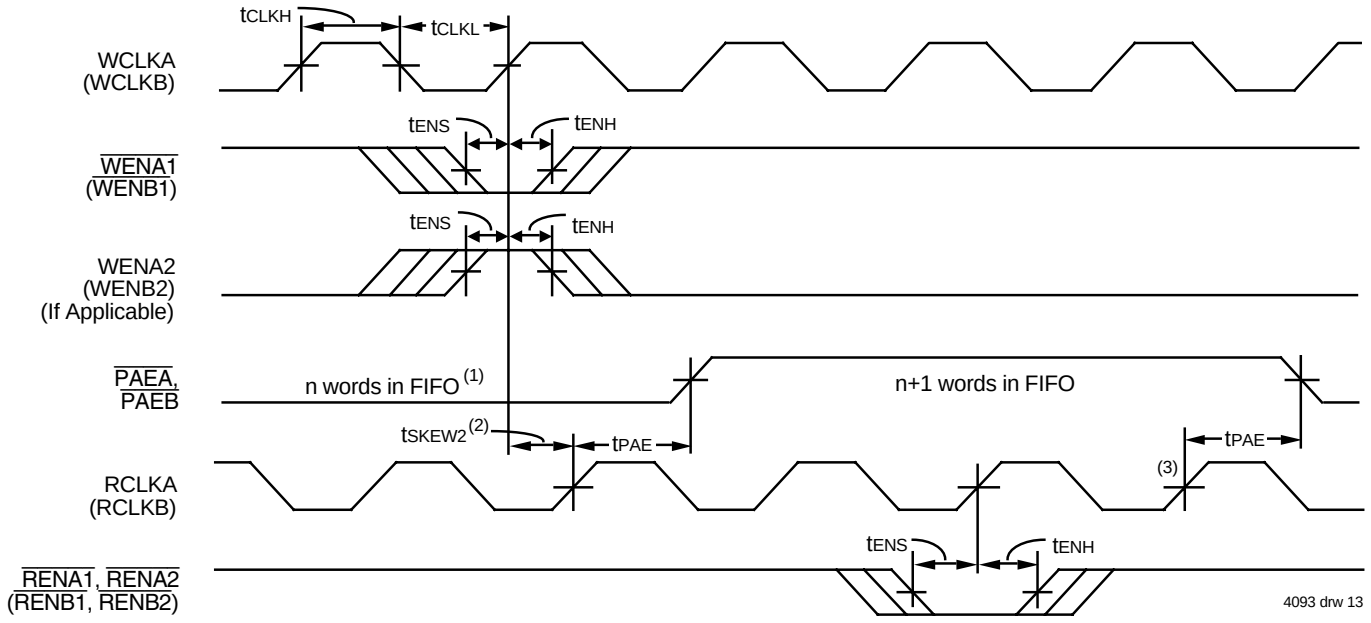
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EFA}$, $\overline{EFB}$ = LOW).

Figure 9. Empty Flag Timing



NOTES:
1. m = PAF offset.
2. (256-m) words for the IDT72V801, (512-m) words the IDT72V811, (1,024-m) words for the IDT72V821, (2,048-m) words for the IDT72V831, (4,096-m) words for the IDT72V841, or (8,192-m) words for the IDT72V851.
3. t_{SKEW2} is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for PAFA (PAFB) to change during that clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW2}, then PAFA (PAFB) may not change state until the next WCLKA (WCLKB) rising edge.
4. If a write is performed on this rising edge of the Write Clock, there will be Full - (m-1) words in FIFO A (B) when PAFA (PAFB) goes LOW.

Figure 10. Programmable Full Flag Timing



NOTES:
1. n = PAE offset.
2. t_{SKEW2} is the minimum time between a rising WCLKA (WCLKB) edge and a rising RCLKA (RCLKB) edge for PAEA (PAEB) to change during that clock cycle. If the time between the rising edge of WCLKA (WCLKB) and the rising edge of RCLKA (RCLKB) is less than t_{SKEW2}, then PAEA (PAEB) may not change state until the next RCLKA (RCLKB) rising edge.
3. If a read is performed on this rising edge of the Read Clock, there will be Empty + (n-1) words in FIFO A (B) when PAEA (PAEB) goes LOW.

Figure 11. Programmable Empty Flag Timing

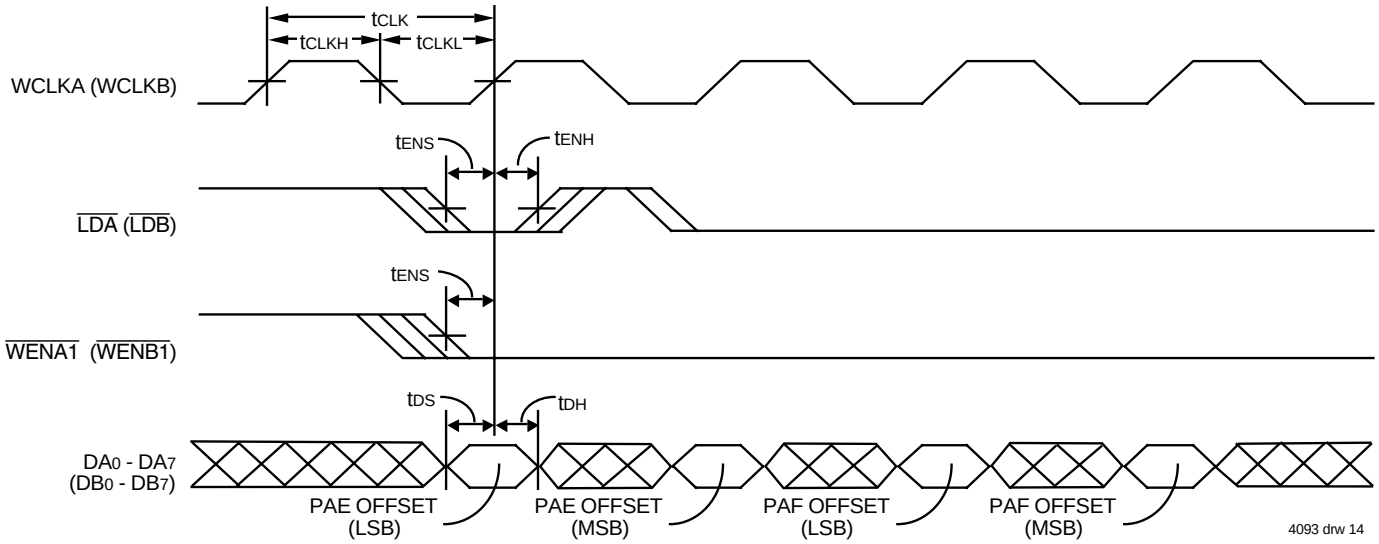


Figure 12. Write Offset Register Timing

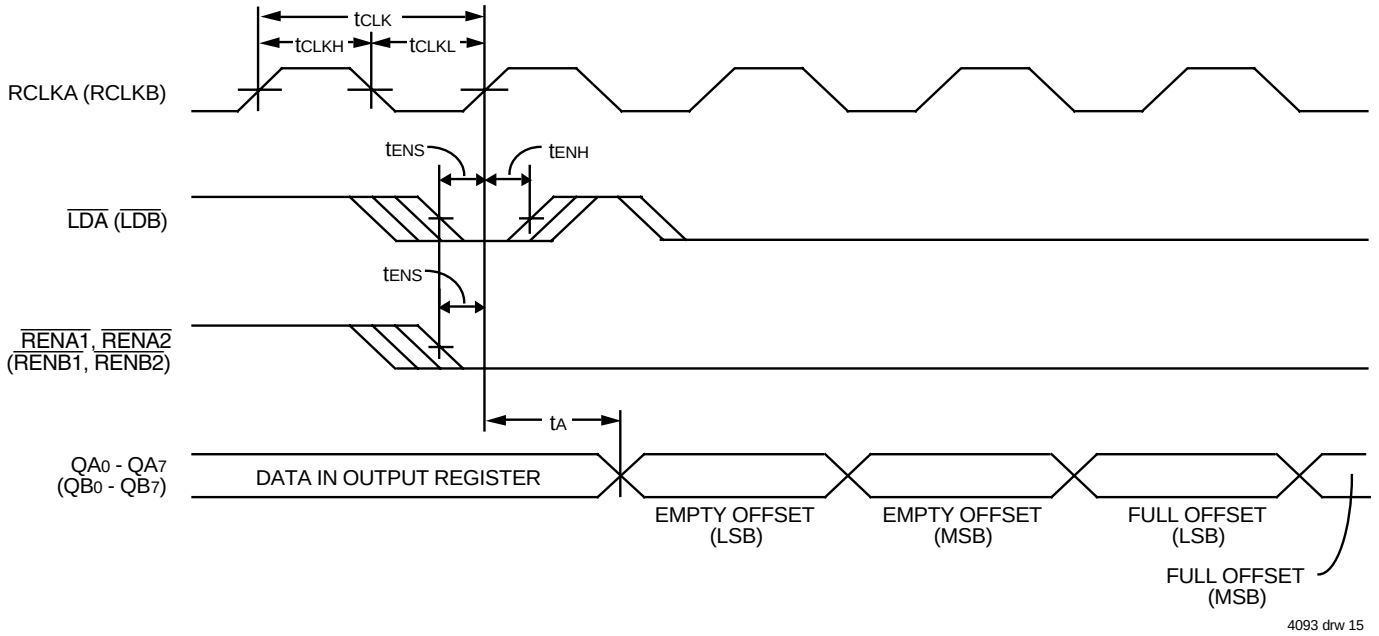


Figure 13. Read Offset Register Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION — When FIFO A (B) is in a Single Device Configuration, the Read Enable 2 $\overline{RENA2}$ ($\overline{RENB2}$) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

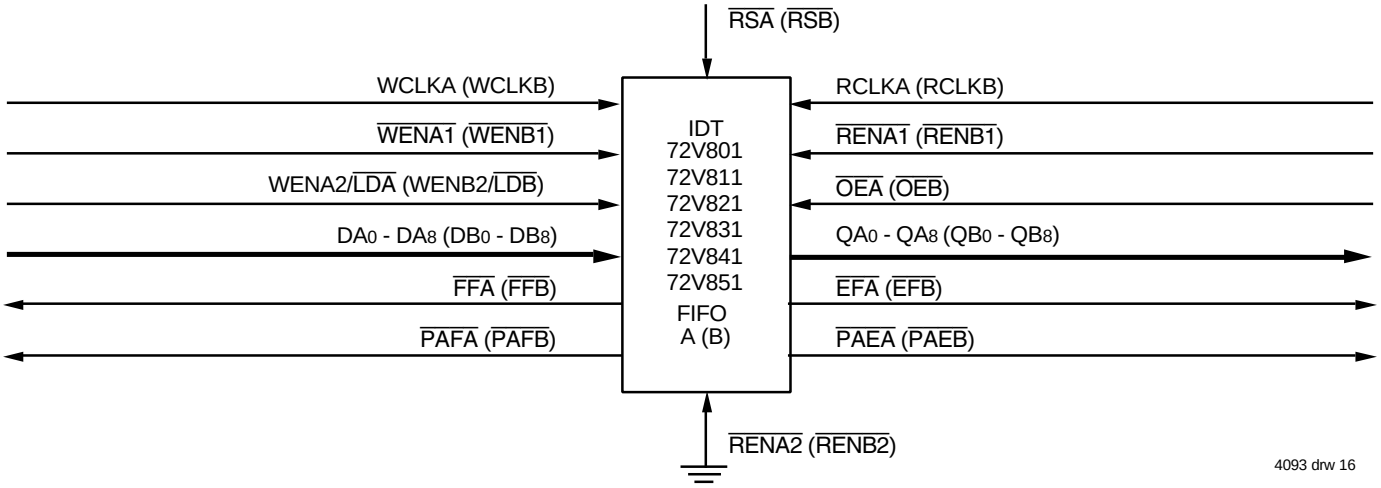


Figure 14. Block Diagram of One of the IDT72V801/72V811/72V821/72V831/72V841/72V851's two FIFOs configured as a single device

WIDTH EXPANSION CONFIGURATION — Word width may be increased simply by connecting the corresponding input control signals of FIFOs A and B. A composite flag should be created for each of the end-point status flags ($\overline{EFA}$ and $\overline{EFB}$, also $\overline{FFA}$ and $\overline{FFB}$). The partial status flags $\overline{PAEA}$, $\overline{PAFB}$, $\overline{PAEA}$ and $\overline{PAFB}$ can be detected from any one device. Figure 15 demonstrates an 18-bit word width using the two FIFOs contained in one IDT72V801/72V811/72V821/72V831/72V841/72V851. Any word width can be attained by adding additional IDT72V801/72V811/72V821/72V831/72V841/72V851s.

When these devices are in a Width Expansion Configuration, the Read Enable 2 ($\overline{RENA2}$ and $\overline{RENB2}$) control inputs can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load (WENA2/$\overline{LDA}$, WENB2/$\overline{LDB}$) pins are set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

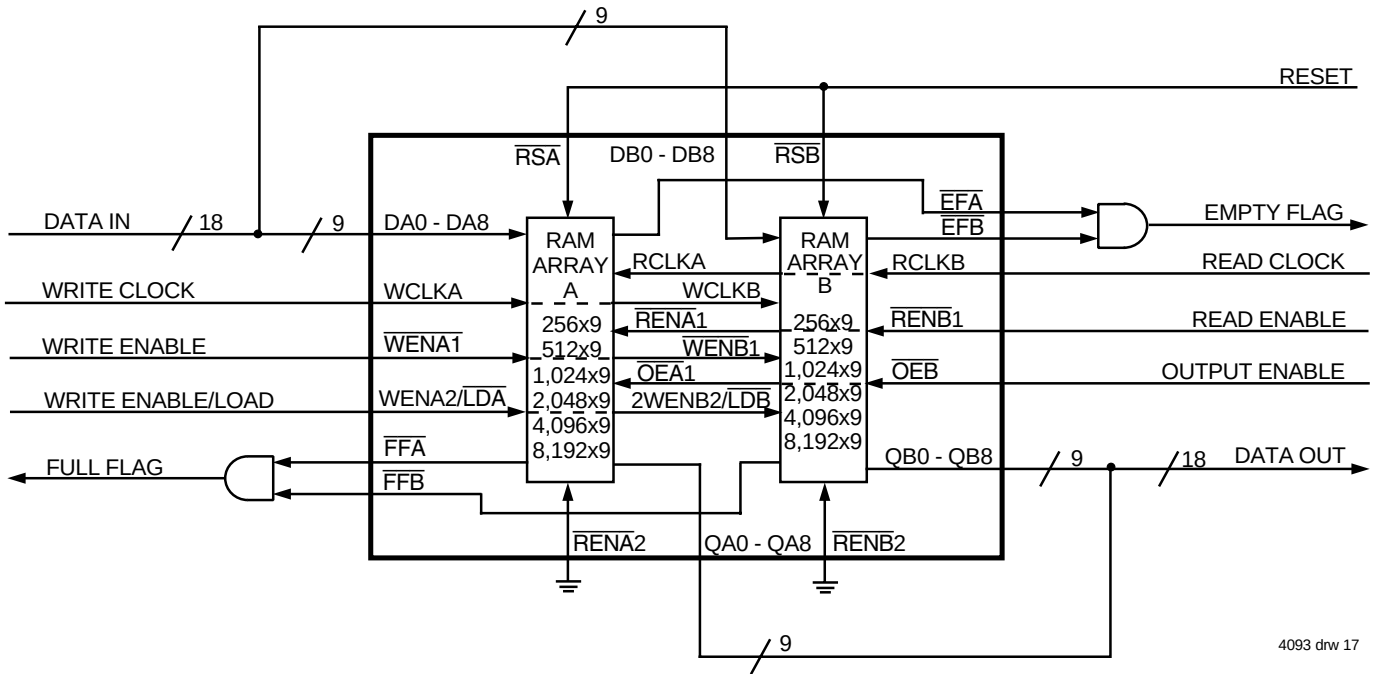


Figure 15. Block diagram of the two FIFOs contained in one IDT72V801/72V811/72V821/72V831/72V841/72V851 configured for an 18-bit width-expansion

TWO PRIORITY DATA BUFFER CONFIGURATION

The two FIFOs contained in the IDT72V801/72V811/72V821/72V831/72V841/72V851 can be used to prioritize two different types of data shared on a system bus. When writing from the bus to the FIFO, control logic sorts the intermixed data according to type, sending one kind to FIFO A and the other kind to FIFO B. Then, at the outputs, each data type is transferred to its appropriate destination. Additional IDT72V801/72V811/72V821/72V831/72V841/72V851s permit more than two priority levels. Priority buffering is particularly useful in network applications.

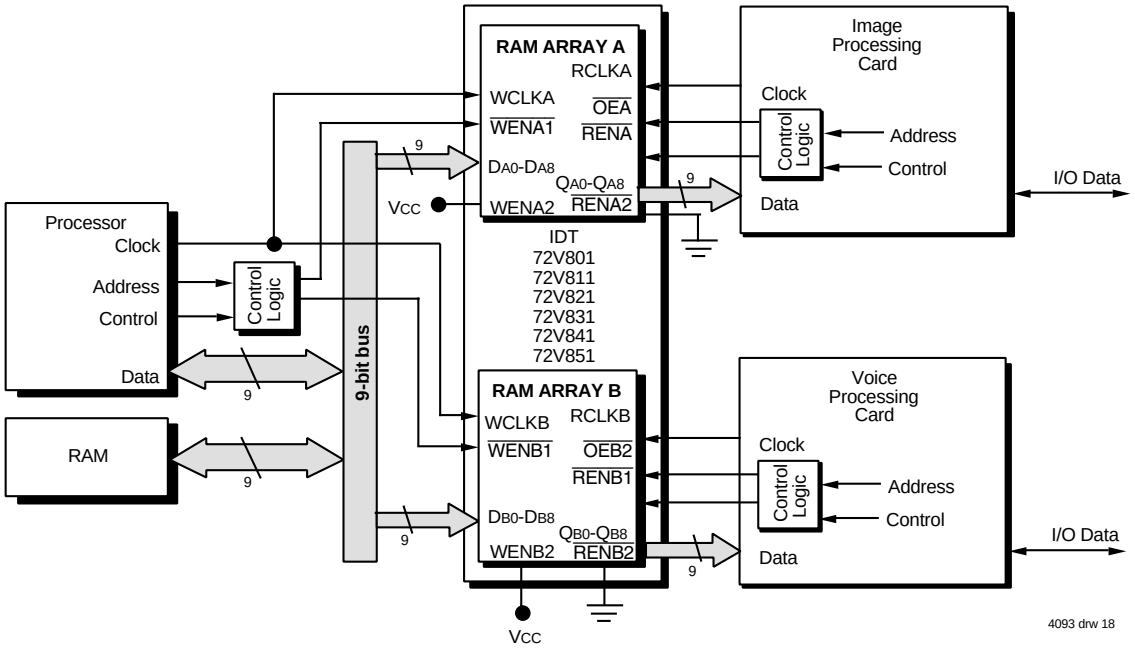


Figure 16. Block Diagram of Two Priority Configuration

BIDIRECTIONAL CONFIGURATION

The two FIFOs of the IDT72V801/72V811/72V821/72V831/72V841/72V851 can be used to buffer data flow in two directions. In the example that follows, a processor can write data to a peripheral controller via FIFO A, and, in turn, the peripheral controller can write the processor via FIFO B.

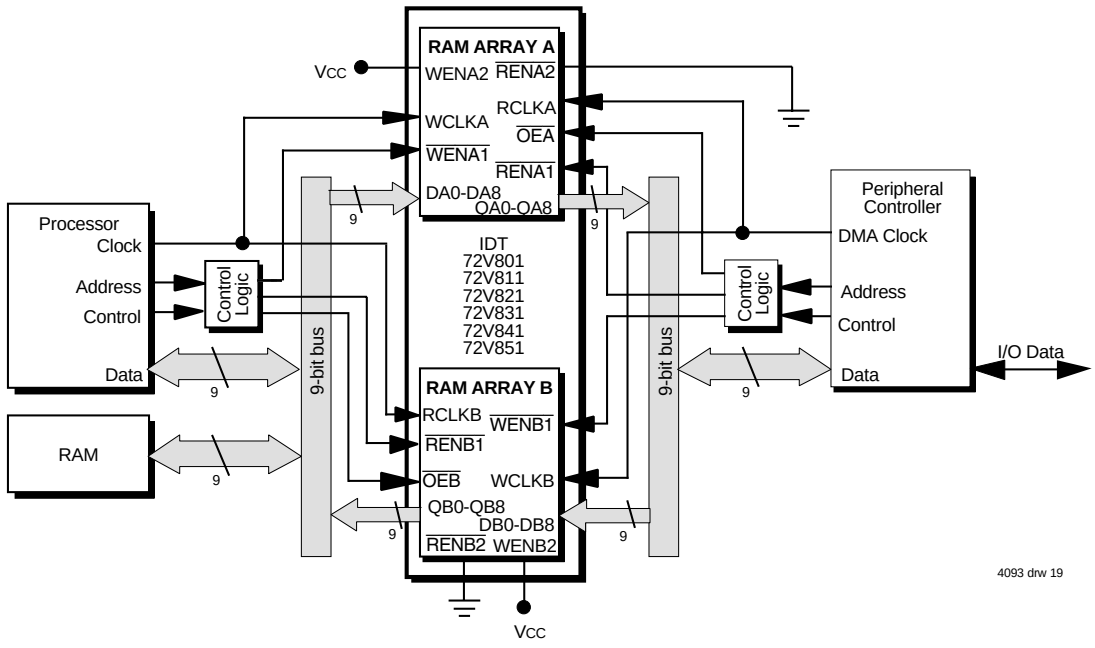


Figure 17. Block Diagram of Bidirectional Configuration

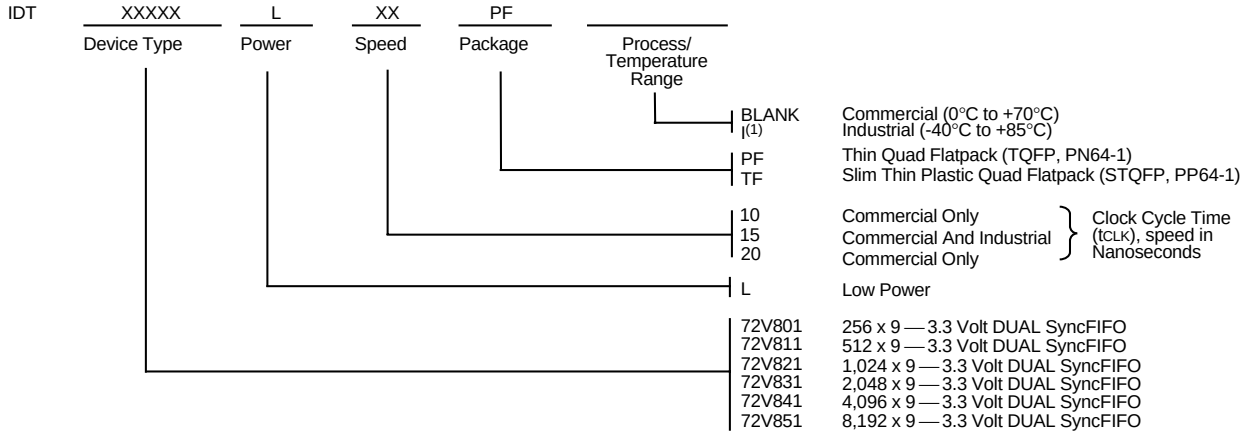
DEPTH EXPANSION — These FIFOs can be adapted to applications that require greater than 256/512/1,024/2,048/4,096/8,192 words. The existence of double enable pins on the read and write ports allow depth expansion. The Write Enable 2/Load (WENA2, WENB2) pins are used as a second write enables in a depth expansion configuration, thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner.

The IDT72V801/72V811/72V821/72V831/72V841/72V851 operates in the Depth Expansion configuration when the following conditions are met:

1. WENA2/$\overline{LDA}$ and WENB2/$\overline{LDB}$ pins are held HIGH during Reset so that these pins operate as second Write Enables.
2. External logic is used to control the flow of data.

Please see the Application Note "DEPTH EXPANSION OF IDT'S SYNCHRONOUS FIFOs USING THE RING COUNTER APPROACH" for details of this configuration.

ORDERING INFORMATION



NOTE:
1. Industrial temperature range product for the 15ns speed grade is available as a standard device.

DATASHEET DOCUMENT HISTORY

04/24/2001 pgs. 4, 5 and 16

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for TECH SUPPORT:
(408) 330-1753
FIFOhelp@idt.com
PF Pkg: www.idt.com/docs/PSC4036.pdf
TF Pkg: www.idt.com/docs/PSC4046.pdf