2N4856A, 2N4857A, 2N4858A, 2N4859A, 2N4860A, 2N4861A

N-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at T_A = 25°C

	2N4856A, 2N4857A, 2N4858A	2N4859A, 2N4860A, 2N4861A
Reverse Gate Source Voltage	– 40 V	– 30 V
Reverse Gate Drain Voltage	– 40 V	– 30 V
Continuous Device Dissipation	1.8 W	1.8 W
Continuous Forward Gate Current	50 mA	50 mA
Power Derating	10 mA/°C	10 mA/°C

At 25°C free air temperature:		2N4856A 2N4859A		2N4857A 2N4860A		2N4858A 2N4861A		Process NJ132		
Static Electrical Characteristics		Min	Max	Min	Max	Min	Max	Unit	Test Conditions	
Gate Source Breakdown Voltage **2N4856A, 2N4857A, 2N4858A**	$V_{(BR)GSS}$		– 40		– 40		– 40	V	I_G = – 1 µA, V_{DS} = ØV	
Gate Source Breakdown Voltage **2N4859A, 2N4860A, 2N4861A**	$V_{(BR)GSS}$		– 30		– 30		– 30	V	I_G = – 1 µA, V_{DS} = ØV	
Gate Reverse Current **2N4856A, 2N4857A, 2N4858A**	I_{GSS}		– 250		– 250		– 250	pA	V_{GS} = – 20V, V_{DS} = ØV	
			– 500		– 500		– 500	nA	V_{GS} = – 20V, V_{DS} = ØV	T_A = 150°C
Gate Reverse Current **2N4859A, 2N4860A, 2N4861A**	I_{GSS}		– 250		– 250		– 250	pA	V_{GS} = – 15V, V_{DS} = ØV	
			– 500		– 500		– 500	nA	V_{GS} = – 15V, V_{DS} = ØV	T_A = 150°C
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	– 4	– 10	– 2	– 6	– 0.8	– 4	V	V_{DS} = 15V, I_D = 0.5 nA	
Drain Saturation Current (Pulsed)	I_{DSS}	50		20	100	8	80	mA	V_{DS} = 15V, V_{GS} = ØV	
Drain Cutoff Current	$I_{D(OFF)}$		250		250		250	pA	V_{DS} = 15V, V_{GS} = – 10V	
			500		500		500	nA	V_{DS} = 15V, V_{GS} = – 10V	T_A = 150°C
Drain Source ON Voltage	$V_{DS(ON)}$		0.75 (20)		0.5 (10)		0.5 (5)	V (mA)	V_{GS} = ØV, I_D = ( )	
Dynamic Electrical Characteristics										
Common Source ON Resistance	$r_{ds(on)}$		25		40		60	Ω	V_{GS} = ØV, I_D = Ø A	f = 1 kHz
Common Source Input Capacitance	C_{iss}		10		10		10	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Common Source Reverse Transfer Capacitance	C_{rss}		4		3.5		3.5	pF	V_{DS} = ØV, V_{GS} = – 10V	f = 1 MHz
Switching Characteristics										
Turn ON Delay Time	$t_{d(on)}$		5 (20) [–10]		6 (10) [– 6]		8 (5) [– 4]	ns (mA) [V]	V_{DD} = 10V, V_{GS} = ØV $I_{D(ON)}$ = ( ) $V_{GS(OFF)}$ = [ ] **(2N4856A, 2N4859A)** R_L = 464Ω **(2N4857A, 2N4860A)** R_L = 953Ω **(2N4858A, 2N486A1)** R_L = 1910Ω	
Rise Time	t_r		3 (20) [–10]		4 (10) [– 6]		8 (5) [– 4]	ns (mA) [V]		
Turn OFF Delay Time	$t_{d(off)}$		25 (20) [–10]		40 (10) [– 6]		80 (5) [– 4]	ns (mA) [V]		

TO-18 Package
See Section G for Outline Dimensions

Pin Configuration
1 Source, 2 Drain, 3 Gate & Case

Surface Mount
SMP4856A, SMP4857A, SMP4858A, SMP4859A, SMP4860A, SMP4861A

InterFET Corporation
1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375

www.interfet.com