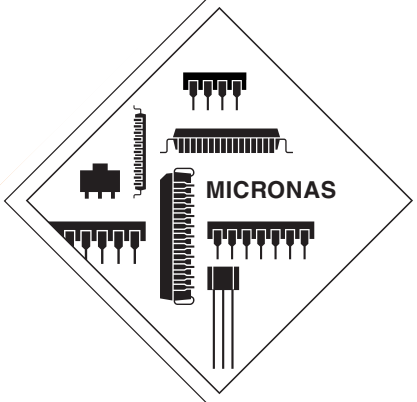

ADVANCE INFORMATION

MAS 3504D
G.729 Annex A
Voice Codec

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MICRONAS

Contents

Contents, continued

G.729 Annex A Voice Codec

1. Introduction

The MAS 3504D is a single-chip codec for use in memory-based voice recording and playback applications. Due to embedded memories, the embedded DC/DC up-converter, and the very low power consumption, the MAS 3504D is ideally suited for portable electronics.

The MAS 3504D implements a voice encoder and decoder that is compliant to the ITU Standard G.729 Annex A. This standard works on 8 kHz, 16 bit, mono audio data that is compressed to 1 bit per audio sample. One second of compressed audio data uses 1000 bytes of memory.

1.1. Features

- Single-chip G.729 decoder
- G.729 Annex A encoder
- ITU compliance tests passed
- Parallel input and parallel output of coded bitstream data
- Input audio data read from an I^2S bus (in various formats)
- Output audio data delivered via an I^2S bus (in various formats)
- Digital volume / mute
- Low power dissipation (150 mW for encoder, 80 mW for decoder @ 3.3 V)
- Supply voltage range: 1.0 V to 3.6 V due to built-in DC/DC converter (1-cell battery operation)
- Adjustable power supply supervision
- Power-off function
- Additional functionality achievable via download software (ADPCM encoder/decoder)

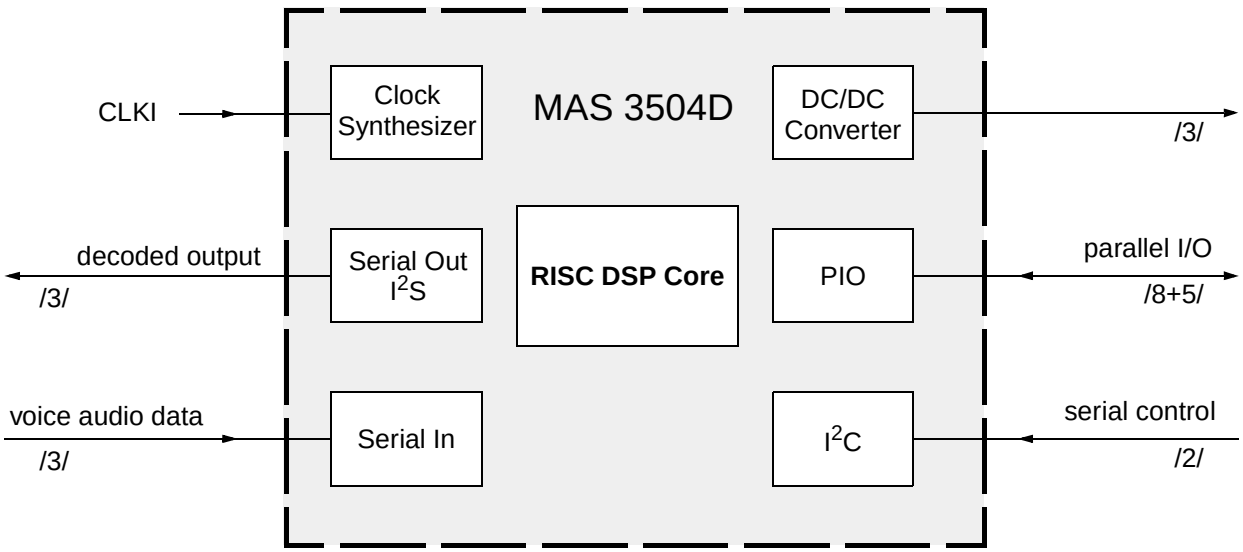


Fig. 1–1: MAS 3504D block diagram

1.2. Application Overview

The MAS 3504D can be applied in two major environments: as standalone decoder or as encoder/decoder combination. For decoding only mode, the DAC 3550A fits perfectly to the requirements of the MAS 3504D. It is a high-quality multi sample rate DAC (8 kHz ... 50 kHz) with internal crystal oscillator, which is only needed for generating the decoder Clock, and integrated stereo headphone amplifier plus 2 stereo inputs.

1.2.1. Decoder Mode

In a memory-based voice playback environment, the decoding is started with a command from a controller. Then the MAS 3504D continuously requests frames of G.729 data every 10 ms via the parallel (PIO) interface.

A delayed response of the host to the request signal (max. 20 milliseconds) will be tolerated by the MAS 3504D as long as the input buffer does not run empty. A PC might use its DMA capabilities to transfer the data in the background to the MAS 3504D without interfering with its foreground processes.

The source of the bit stream may be a memory (e.g. ROM, Flash) or PC peripherals, such as CD-ROM drive, a hard disk or a floppy disk drive.

1.2.2. Encoder Mode

For encoding a support routine must be downloaded to the MAS 3504D via I^2C. After the encoder is started, it begins to encode the incomming audio data and writes the coded datastream to the parallel (PIO) interface.

A delayed response of the host to the data available signal (max. 20 milliseconds) will be tolerated by the MAS 3504D as long as the output buffer does not overrun.

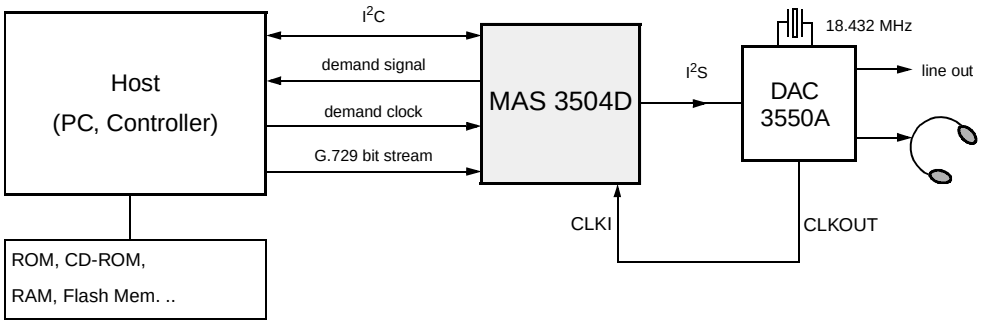


Fig. 1–2: Block diagram of a MAS 3504D, decoding a stored bit stream in a decoding only application

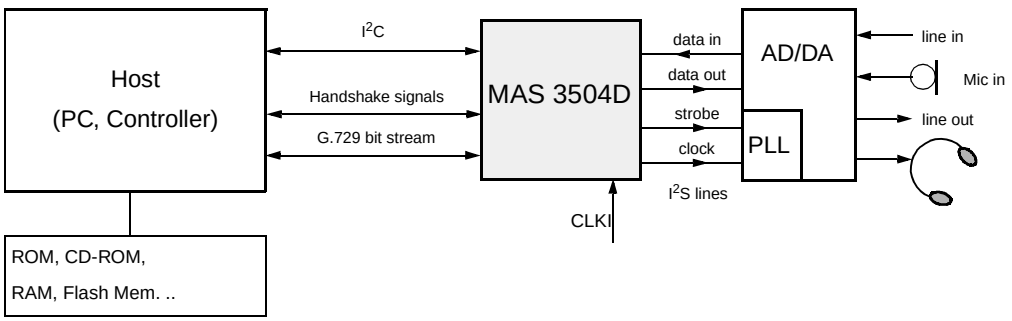


Fig. 1–3: Block diagram of a MAS 3504D in an encoding/decoding application

2. Functional Description of the MAS 3504D

2.1. DSP Core

The hardware of the MAS 3504D consists of a high performance Digital Signal Processor and appropriate interfaces. The processor works with a memory word length of 20 bits and an extended range of 32 bits in its accumulators. The instruction set of the DSP is highly optimized for audio data compression and decompression. Thus, only very small areas of internal RAM and ROM are required. All data input and output actions are based on a ‘non cycle stealing’ background DMA that does not cause any computational overhead.

2.2. Firmware (Internal Program ROM)

The firmware fully contains a G.729 voice decoder. With an additional support routine the IC is extended to a G.729 Annex A encoder.

The G.729 standard compresses 8 kHz/16 bit mono voice data in frames of 80 samples to 10 bytes each, what results in a compressed bitstream of 1 bit/sample. The encoding according to Annex A has reduced complexity, but is fully compatible to the initial G.729 standard. Therefore the MAS 3504D can decode bitstreams that were encoded by other G.729 encoders and it can encode bitstreams that can be decoded with other G.729 decoders.

2.2.1. G.729 Encoder

For encoding operation the MAS 3504D has to be prepared by downloading an additional routine to support the encoder. After starting the encoder, 80 audio samples are continously read via the serial input interface. Each audio block of 80 samples is encoded to a G.729 data frame consisting of 10 bytes which is sent via the parallel interface. It is possible to monitor the input audio samples also directly via the serial output interface.

2.2.2. G.729 Decoder

The MAS 3504D expects a sequence of valid G.729 frames (10 bytes each) as input. The compressed data is sent via the parallel interface. Each frame is decoded to 80 audio samples, modified by the volume/mute control and sent out via the serial output interface.

2.3. Program Download Feature

The overall function of the MAS 3504D can be altered by downloading up to 1 kWord program code into the internal RAM and by executing this code instead of the ROM code. During this time, G.729 processing is not possible.

The code must be downloaded by the ‘write to memory’ command (see Section 3.3.) into an area of internal RAM. A ‘run’ command starts the operation.

Micronas provides modules for encoding and decoding audio data with ADPCM.

Detailed information about downloading is provided in combination with the MAS 3504D software development package from Micronas.

2.4. Clock Management

The MAS 3504D should be driven by a single clock at a frequency of 18.432 MHz.

The CLKI signal acts as a reference for the embedded clock synthesizer that generates the internal system clock.

2.5. Power Supply Concept

The MAS 3504D offers an embedded controlled DC/DC converter and voltage monitoring circuits for battery based power supply concepts. It works as an up-converter. The application circuit for the DC/DC converter is shown in Fig. 2–1.

2.5.1. Internal Voltage Monitor

An internal voltage monitor compares the input voltage at the VSENS pin with an internal reference value that is adjustable via I^2C bus. The PUP output pin becomes inactive when the voltage at the VSENS pin drops below the programmed value of the reference voltage.

It is important that the WSEN must not be activated before the PUP is generated. The PUP signal thresholds are listed in Table 3–8.

2.5.2. DC/DC Converter

The DC/DC converter of the MAS 3504D is used to generate a fixed power supply voltage even if the chip is powered by battery cells in portable applications. The DC/DC converter is designed for the application of 1 or 2 batteries or NiCd cells. The DC/DC converter is switched on by activating the DCEN pin. Its output power is sufficient for other ICs as well.

A 22 µH inductor is required for the application. The important specification item is the inductor saturation current rating, which should be greater than 2.5 times the DC load current. The DC resistance of the inductor is important for efficiency. The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR), as the product of the inductor current variation and the ESR determines the high-frequency amplitude seen on the output voltage. The Schottky diode should have a low voltage drop V_D for a high overall efficiency of the DC/DC converter. The current rating of the diode should also be greater than 2.5 times the DC output current. The VSENS pin is always connected to the output voltage at the low ESR capacitor.

2.5.3. Stand-by Functions

The digital part of the MAS 3504D and the DC/DC converter are turned on by setting WSEN. If only the DC/DC converter should work, it can remain active bysetting DCEN alone to supply other parts of the application even if the audio decoding part of the MAS 3504D is not being used. The WSEN power-up pin of the digital part should be handled by the controller.

Please pay attention to the fact, that the I^2C interface is working only if the processor is powered up (WSEN = 1).

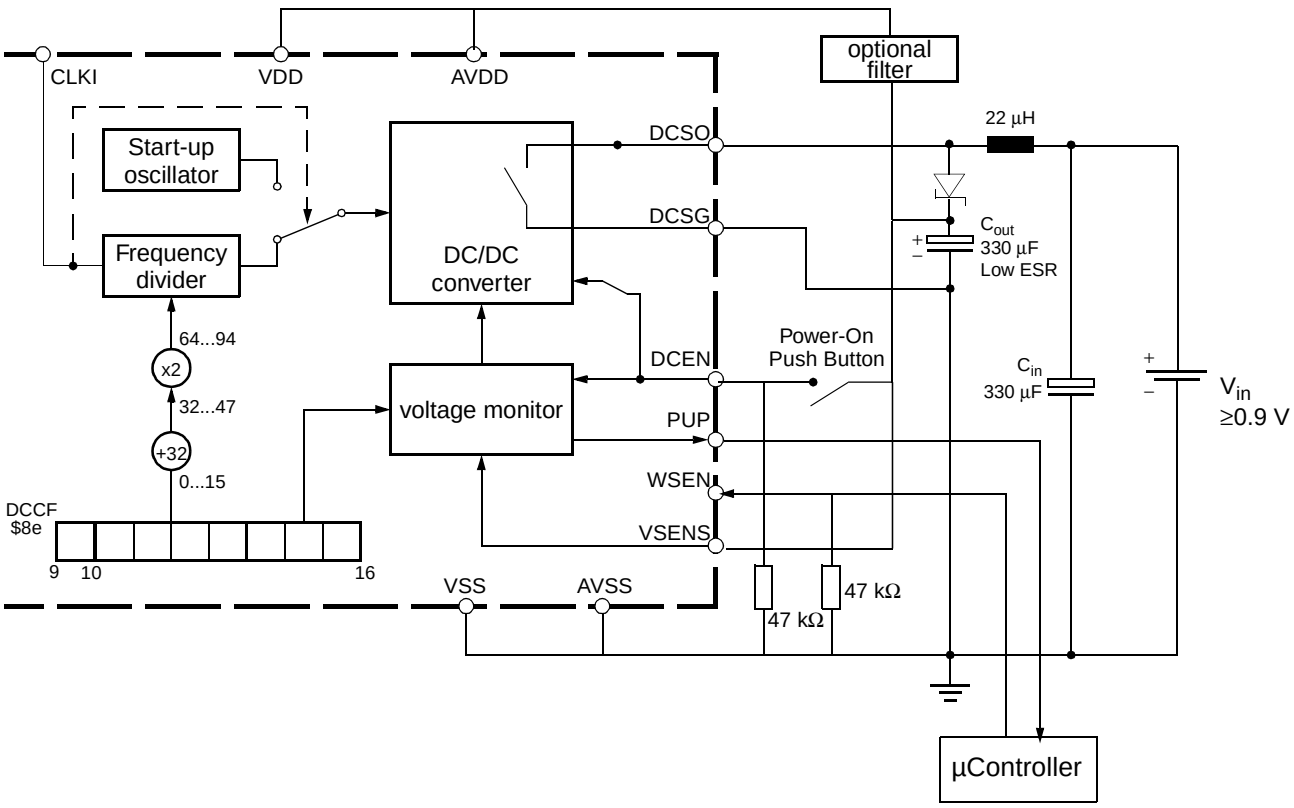


Fig. 2–1: DC/DC converter application circuit

2.5.4. Start-up Sequence

The DC/DC converter operates at a minimum input voltage of 0.9 V. In case WSEN is active, the MAS 3504D is in the DSP operation mode. The start-up script should be as follows:

1. in the power-off state DCEN and WSEN are inactive

2. set DCEN to > 0.9 V

3. hold DCEN until controller operates, detects if *PUP* is high, and sets WSEN to high.

Please also refer to Figure 2–2.

Note: Connecting DCEN directly to VDD leads to unexpected states of the DCCF register.

The PUP signal should be read out by the system controller and used to set WSEN.

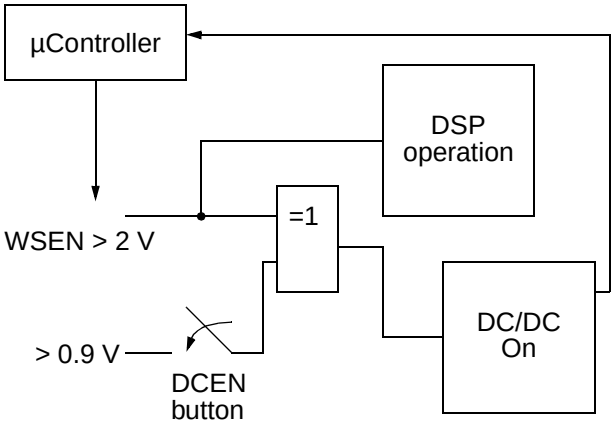


Fig. 2–2: DC/DC startup

2.6. Interfaces

The MAS 3504D uses an I^2C control interface, a parallel I/O interface (PIO) for G.729- or ADPCM-data, a digital audio input interface (SDI) for audio data input and a digital audio output interface (SDO) for the decoded audio data (I^2S or similar).

The G.729 bit stream generated by an encoder is aligned in frames of 10 bytes. The parallel data required from the G.729 decoder must be sent in byte-swapped order related to the standard specification. The G.729 encoder also sends the encoded bit stream byte-swapped to the PIO interface.

2.6.1. Parallel Input Output Interface (PIO)

The parallel interface of the MAS 3504D consists of the lines PI0...PI4, PI8, PI12...PI19, and several control lines.

2.6.2. Parallel Data Output

In encoding mode, PIO lines PI12...PI19 are switched to the MAS 3504D data output which hence will be an 8-bit parallel output port with MSB first (at position PI19) for the G.729 bit stream data.

The data is transfered in bursts of 10 bytes (1 frame) each 10 ms. If the transmission of headers is enabled, there is an additional 10 byte burst before each sequence of 50 frames.

Handshaking for PIO output mode is accomplished through the $\overline{RTW}$, $\overline{PCS}$, and PI12..PI19 signal lines (see Fig. 2–3). The PR line has to be set to high level.

$\overline{RTW}$ will go low as soon as a byte is available in the output buffer and will stay low until a byte has been read. Reading of a byte is performed with a $\overline{PCS}$ pulse. Data is latched out from the MAS 3504D on the falling edge of $\overline{PCS}$ and removed from the bus on the rising edge of $\overline{PCS}$.

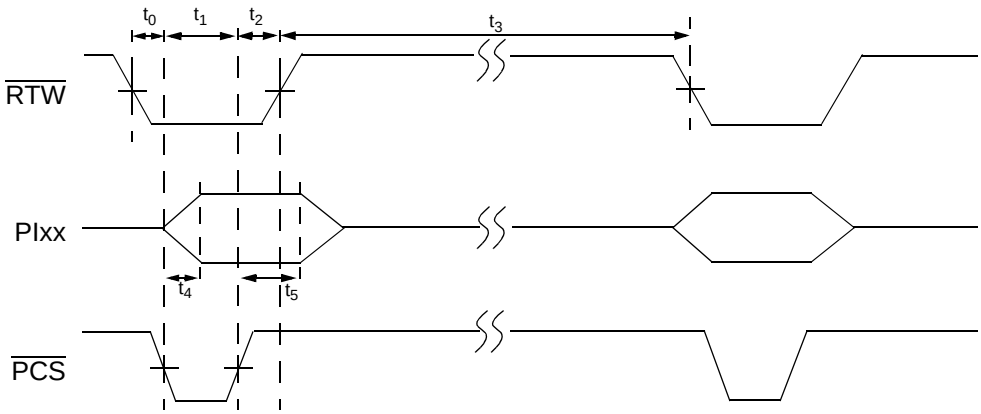


Fig. 2–3: Parallel Data Output (PIO) Timing

Table 2–1: PIO Output Mode Timing[1)]

Symbol	Pin	Min.	Max.	Unit
t_0	$\overline{RTW}$, $\overline{PCS}$	0.010	1800	µs
t_1	PCS	0.330		µs
t_2	$\overline{PCS}$, $\overline{RTW}$	0.010		µs
t_3	$\overline{RTW}$	0.330	10000	µs
t_4	PI	0.330		µs
t_5	PI	0.081		µs

1) see Figure 2–3

2.6.3. Parallel Data Input

In decoding mode, PIO lines PI12...PI19 are switched to the MAS 3504D data input which hence will be an 8-bit parallel input port with MSB first (at position PI19) for the G.729 bit stream data. In order to write data to this parallel port, a special handshake protocol has to be used by the controller (see Fig. 2–4).

2.6.3.1. DMA Handshake Protocol

The data transfer can be started after the $\overline{EOD}$ pin of the MAS 3504D is set to high. After verifying this, the controller indicates the transmission of data by activating the PR line. The MAS 3504D responds by setting the $\overline{RTR}$ line to the low level. The MAS 3504D reads the data PI[19:12] after the rising edge of the PR. The next data word write operation will again be initialized by setting the PR line via the controller. Please refer to Figure 2–4 and Table 2–2 for the exact timing.

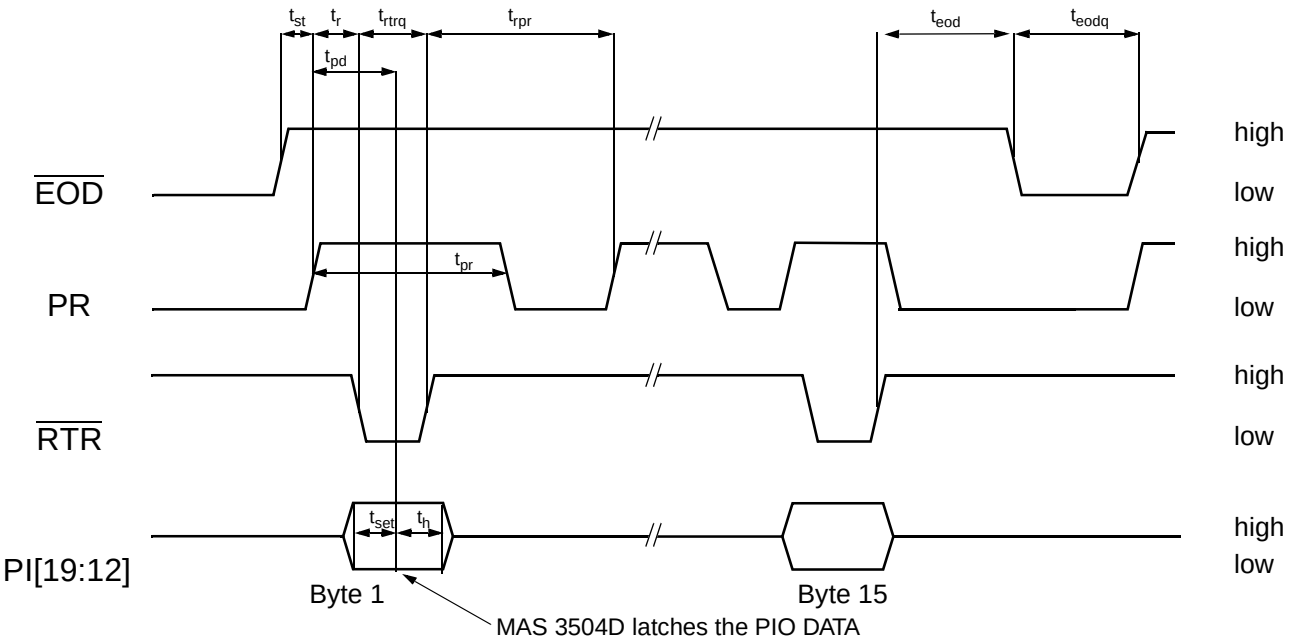


Fig. 2–4: Handshake protocol for writing G.729 data to the PIO-DMA

2.6.3.2. End of DMA Transfer

The above procedure will be repeated until the MAS 3504D sets the $\overline{EOD}$ signal to “0”, which indicates that the transfer of one data block has been executed. Subsequently, the controller should set PR to “0”, wait until $\overline{EOD}$ rises again, and then repeat the procedure (see Section 2.6.3.1.) to send the next block of data. The DMA buffer is 10 bytes long (one frame).

The recommended PIO DMA conditions and the characteristics of the PIO timing are given in Table 2–2.

Table 2–2: PIO DMA Timing

Symbol	PIO Pin	Min.	Max.	Unit
t_{st}	PR, $\overline{EOD}$	0.010	2000	µs
t_r	PR, $\overline{RTR}$	40	160	ns
t_{pd}	PR, PI[19:12]	120	480	ns
t_{set}	PI[19:12]	160	no limit	ns
t_h	PI[19:12]	160	no limit	ns
t_{rtrq}	$\overline{RTR}$	200	30000	ns
t_{pr}	PR	120	no limit	ns
t_{rpr}	PR, $\overline{RTR}$	40	no limit	ns
t_{eod}	PR, $\overline{EOD}$	40	160	ns
t_{eodq}	EOD	0	500	µs

2.6.4. Audio Input Interface (SDI)

The A/D interface is a standard I^2S interface (16/32 bit, stereo). This input is used for G.729 recording mode and must be slaved to the D/A output clock and word-strobe signals.

The interface is configurable by software to work in different modes. It is possible to choose:

– inverted or noninverted word strobe (SOI),

– no delay or delay of data related to word strobe

– inverted or noninverted I^2S-Clock (SOC).

For further details see Section 3.5.4.

2.6.5. Audio Output Interface (SDO)

The audio output interface of the MAS 3504D is a standard I^2S interface. As the G.729 standard is only working on mono signals, the same signal is written to both output channels (left and right).

The interface is configurable by software to work in different modes. It is possible to choose:

– 16 or 32 bit/sample modes,

– inverted or noninverted word strobe (*SOI*),

– no delay or delay of data related to word strobe

– inverted or noninverted I^2S-clock (*SOC*).

For further details see Section 3.5.4.

2.6.5.1. Example 1:16 Bits/Sample (I^2S Compatible Data Format)

A schematic timing diagram of the SDO interface in 16 bit/sample mode with delayed data by 1 clock cycle is shown in Fig. 2–5.

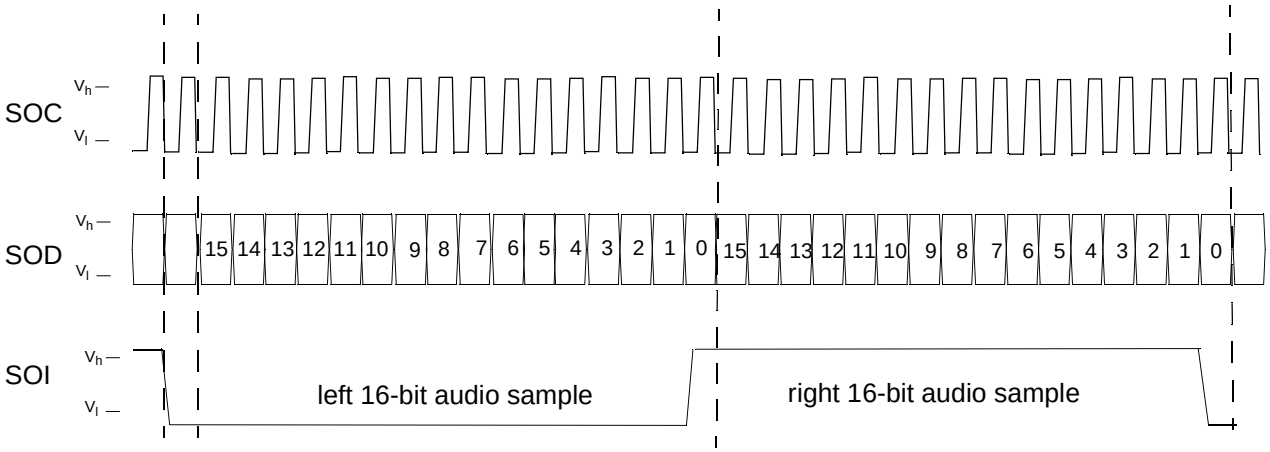


Fig. 2–5: Schematic timing of the SDO interface in 16bit/sample mode

2.6.5.2. Example 2:32 Bit/Sample (Inverted SOI)

If the serial output generates 32 bits per audio sample, only the first 20 bits will carry valid audio data. The 12 trailing bits are set to zero by default (see Fig. 2–6).

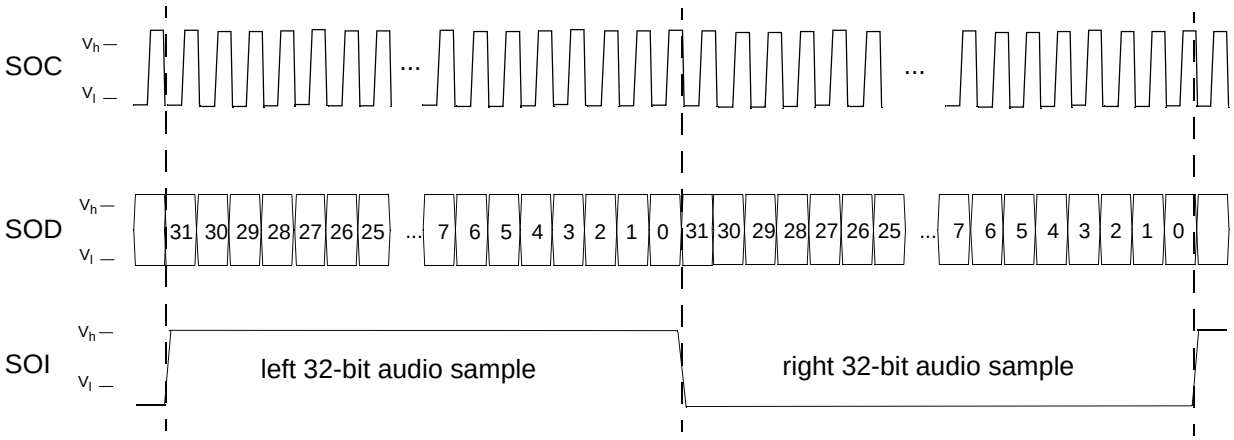


Fig. 2–6: Schematic timing of the SDO interface in 32 bit/sample mode

3. Control Interfaces

3.1. I²C Bus Interface

3.1.1. Device and Subaddresses

The MAS 3504D is controlled via the I²C bus slave interface.

The IC is selected by transmitting the MAS 3504D device addresses. (see Table 3–1).

Writing is done by sending the device write address, ($3a) followed by the subaddress byte ($68) and two or more bytes of data. Reading is done by sending the write device address ($3a), followed by the subaddress byte ($69). Without sending a stop condition, reading of the addressed data is completed by sending the device read address ($3b) and reading n-bytes of data.

By means of the RESET bit in the CONTROL register,the MAS 3504D can be reset by the controller.

Due to the internal architecture of the MAS 3504D, the IC cannot react immediately to an I²C request. The typical response time is about 0.5 ms. If the MAS 3504D cannot accept another complete byte of data, it will hold the clock line I2C_CL LOW to force the transmitter into a wait state. The maximum wait period of the MAS 3504D during normal operation mode is less than 4 ms.

Table 3–1: I²C Bus Device Addresses

MAS 3504D device address	Write	Read
MAS_I2C_ADR	$3a	$3b

Table 3–2: Control Register (Subaddress: $6a)

Name	Subaddress	Bit : 8	Bit : 0-7, 9-15
CONTROL	$6a	1 : Reset 0 : normal	0

Table 3–3: I²C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL_MAS	0000 0000	$6a	Write	control subaddress (see Table 3–2)
WR_MAS	0110 1000	$68	Write	write subaddress
RD_MAS	0110 1001	$69	Write	read subaddress

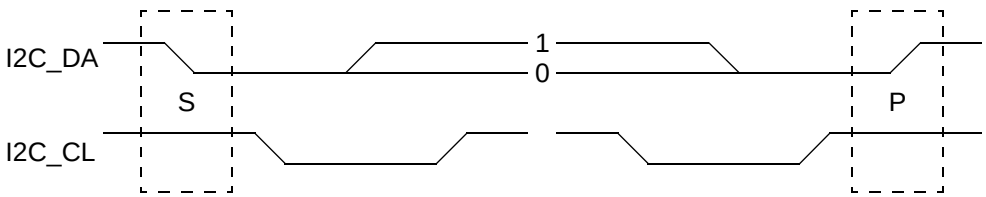


Fig. 3–1: I²C bus protocol (MSB first; data must be stable while clock is high)

Note: S = I²C-Bus Start Condition from master
P = I²C-Bus Stop Condition from master
A = Acknowledge-Bit: LOW on I2C_DA from slave or master
N = Not Acknowledge-Bit: HIGH on I2C_DA from master to indicate ‘End of Read’

Wait = I²C-Clock line is held low, while the MAS 3504D is processing the I²C command. This waiting time is max. 1 ms

3.2. Command Structure

The I^2C control of the MAS 3504D is done completely via the I^2C data register by using a special command syntax. The commands are executed by the MAS 3504D during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. These I^2C commands allow the controller to access internal states, RAM contents, internal hardware control registers, and to download software modules. The command structure allows sophisticated control of the MAS 3504D. The registers of the MAS 3504D are either general purpose, e.g. for program flow control, or specialized registers that directly affect hardware blocks. The unrestricted access to these registers allows the system controller to overrule the firmware configuration.

The MAS 3504D firmware scans the I^2C interface periodically and checks for pending or new commands. Table 3–4 shows the basic controller commands that are available by the MAS 3504D.

3.2.1. Conventions for the Command Description

The description of the various controller commands uses the following formalism:

– A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.

– Data values in nibbles are always shown in hexadecimal notation indicated by a preceding $.

– A hexadecimal 20-bit number *d* is written, e.g. as d = $17c63, its five nibbles are
d0 = $3, d1 = $6, d2 = $c, d3 = $7, and d4 = $1.

– **Abbreviations** used in the following descriptions:
a address
d data value
n count value
o offset value
r register number
x don't care

– **Variables** used in the following descriptions:
dev_write $3a
dev_read $3b
data_write $68
data_read $69

Table 3–4: Basic Controller Commands

Code	Command	Comment
$0 $1	run	Start execution of an internal program. (Run 0 means freeze operating system.)
$9	write register	An internal register of the MAS 3504D can be written directly to by the controller.
$a $b	write to memory	A block of the DSP memory can be written to by the controller. This feature may be used to download alternate programs.
$d	read register	The controller can read an internal register of the MAS 3504D.
$e $f	read memory	A block of the DSP memory can be read by the controller.

3.3. Detailed MAS 3504D Command Syntax

3.3.1. Run

S	dev_write	A	data_write	A	a3,a2	A	a1,a0	A	P

The *'run'* command causes the start of a program part at address **a** = (a3, a2, a1, a0). The nibble a3 is restricted to **$0** or **$1** which also acts as command selector. Run with address **a = $0** will suspend the encoding/decoding function and only I^2C commands are evaluated. This freezing is required if alternative software is downloaded into the internal RAM of the MAS 3504D. Detailed information about downloading is provided in combination with a MAS 3504D software development package or together with MAS 3504D software modules available from Micronas.

Example: 'run' at address $1 (start of G.729 decoder) has the following I^2C protocol:

<$3a><$68><$00><$01>

3.3.2. Write Register

S	dev_write	A	data_write	A	**$9**, r1	A	r0, d0	A	
					d4, d3	A	d2, d1	A	P

The controller writes the 20-bit value (**d** = d4, d3, d2, d1, d0) into the MAS 3504D register (**r** = r1,r0). In contrast to memory cells, registers are always addressed individually, and they may also interact with built-in hardware blocks. A list of registers is given in Section 3.5.

Example: G.729 decoding is started by writing the value 1 into the register with the number $fd:

<$3a><$68><$9f><$d1><$00><$00>

3.3.3. Write D0 Memory

S	dev_write	A	data_write	A	**$A**, $0	A	$0,$0	
				A	**n3,n2**	A	n1,n0	
				A	a3,a2	A	a1,a0	
				A	**d3,d2**	A	d1,d0	
				A	$0,$0	A	$0,d4	
				....repeat for n data values....				
				A	**d3,d2**	A	d1,d0	
				A	$0,$0	A	$0,d4	A P

n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The MAS 3504D has 2 memory areas of 2048 words each called D0 and D1 memory. For both memory areas, read and write commands are provided.

Example: writing one word to address d0:$0321 has the following I^2C protocol:

```
<$3a><$68><$a0><$00> (write D0 memory)
<$00><$01>           (1 word to write)
<$03><$21>           (start address)
<$23><$45>           (value = $12345)
<$00><$01>
```

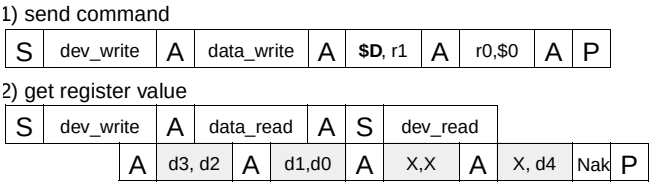
3.3.4. Write D1 Memory

S	dev_write	A	data_write	A	**$B**, $0	A	$0,$0	
				A	**n3,n2**	A	n1,n0	
				A	a3,a2	A	a1,a0	
				A	**d3,d2**	A	d1,d0	
				A	$0,$0	A	$0,d4	
				....repeat for n data values....				
				A	**d3,d2**	A	d1,d0	
				A	$0,$0	A	$0,d4	A P

n3..n0: number of words to be transmitted
a3..a0: start address in MASD memory
d4..d0: data value

For further details, see 'write D0 memory' command.

3.3.5. Read Register



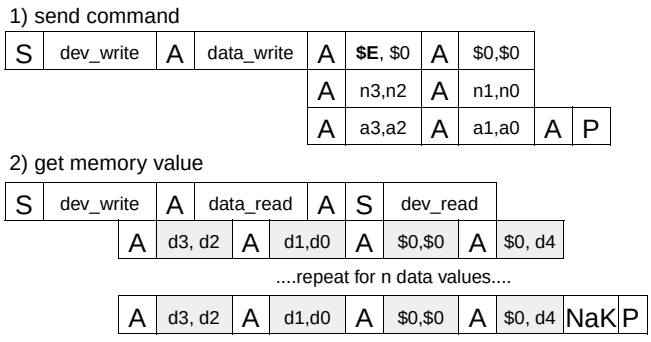
r1, r0: register **r**
d3...d0: data value in **r**
X: don't care

The MAS 3504D has an address space of 256 registers. Some of the registers (**r** = r1, r0 in the figure above) are direct control inputs for various hardware blocks, others do control the internal program flow. In the next section, those registers that are of any interest with respect to the G.729 codec are described in detail.

Example:
Read the content of the PIO data register ($c8):

<$3a><$68><$dc><$80>
<$3a><$69><$3b>
now read:
<d3,d2><d1,d0><x,x><x,d4>

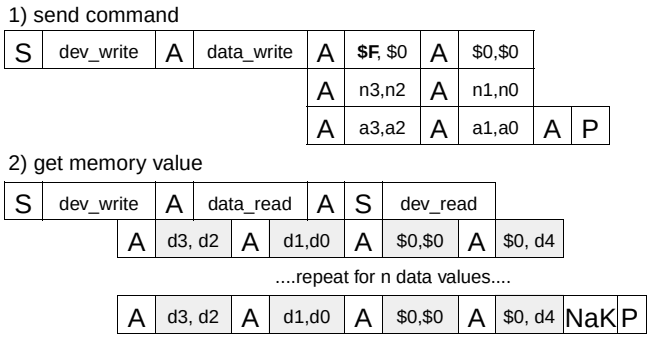
3.3.6. Read D0 Memory



n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The 'read D0 memory' command is provided to get information from memory cells of the MAS 3504D. It gives the controller access to all memory cells of the internal D0 memory. Direct access to memory cells is an advanced feature of the DSP. It is intended for users of the MASC software development kit.

3.3.7. Read D1 Memory



n3..n0: number of words
a3..a0: start address in MASD memory
d4..d0: data value

The 'read D1 memory' command is provided to get information from memory cells of the MAS 3504D. It gives the controller access to all memory cells of the internal D1 memory.

3.4. Version Number

Table 3–5 shows where the chip identification and the name of the software is located.

Table 3–5: MAS 3504D Version

Addr.	Content	Example Value	
D1:$ff6	name of MAS 3504D version	0x03504	3504
D1:$ff9	description: "G.729a CODEC"	0x0472e	G.
D1:$ffa		0x03732	72
D1:$ffb		0x03961	9a
D1:$ffc		0x02043	C
D1:$ffd		0x04f44	OD
D1:$ffe		0x04543	EC
D1:$fff		0x02020	

3.5. Register Table

In Table 3–6, the internal registers for controlling the MAS 3504D are listed. They are accessible by ‘register read/write’ I^2C commands (see Section 3.3.). For a more detailed register usage (see Table 3–8).

Important note! Writing into undocumented registers or read-only registers is always possible, but it is highly recommended not to do so. It may damage the function of the firmware and may even lead to a complete system crash of the decoder operation which can only be restored by a reset.

3.5.1. DC/DC Converter (Reg. $8e)

The DCCF Register controls both the internal voltage monitor and the DC/DC converter. Between output voltage of the DC/DC converter and the internal voltage monitor threshold an offset exists which is shown in Table 3–8. Please pay attention to the fact, that I^2C protocol is working only if the processor works (WSEN = 1).However, the setting for the DCCF register will remain active if the DCEN and WSEN lines are deasserted.

The DC/DC converter may generate interference noise that could be unacceptable for some applications. Thus the oscillator frequency may be adjusted in 32 steps in order to allow the system controller to select a base frequency that does not interfere with an other application.

The CLKI input provides the base clock f_{CLKI} for the frequency divider whose output is made symmetrical with an additional divider by two. The divider quotient is determined by the content of the DCCF register. This register allows 32 settings generating a DC/DC converter clock frequency f_{dc} between:

$$f_{SW} = \frac{f_{CLKI}}{2 \cdot (m+n)}\Bigg|_{n \in \{0,15\},\, m \in \{32,16\}} \qquad \text{(EQ 1)}$$

3.5.2. User Control (Reg. $fd)

The UserControl register is used to switch between basic operation modes. On startup, after a software reset or a “run 1” command it is set to $0. The MAS 3504D sets the control registers to default values, switches off all interfaces (except I^2C) and waits for a change in UserControl.

Table 3–6: Command Register Table

Address (hex)	Mode	Function	Default (hex)	Name
8e	w	DC/DC operation control	8000	DCCF
fd	w	Operation mode selection	0	UserControl
fc	w	Output volume	7ffff	Volume
74	w	Serial interface wordlength	0	Wordlength
e1	w	Configuration of the I^2S audio input interface	4	InputConfig
61	w	Configuration of the I^2S audio output interface	4000	OutputConfig
fa	w	Special operation options	0	HWControl

3.5.2.1. Data Transmission Format

The codec is working on a page basis. That means, that encoding and decoding is performed in blocks of 50 G.729 frames, whereas each frame consists of 10 bytes in byteswapped order (see Fig. 3–2). Therefore most changes to the UserControl register become effective when processing of a page is finished. The pages are optionally preceeded by 10 byte header frames (see Table 3–7).

Table 3–7: Content of Page Header

Byte	1	2	3	4	5	6	7	8	9	10
Value	$64	$6d	$72	$31	$64	$61	$74	$61	$f4	$01

Switching from encoding to decoding mode or vice versa directly is not allowed. Instead the controller has to send a stop request to the MAS 3504D (writing $0 to UserControl). Then the controller has to keep on sending data in decoding mode or receive data in encoding mode until the current page of 50 frames is finished. After this run out time, the encoding or decoding can be started again.

3.5.2.2. Encoder Operation

To enable the G.729 encoder mode, a special routine has to be downloaded to the MAS 3504D IC first. This has to be done with an I^2C download before the encoder is started the first time. If the encoder is started without downloading the routine, the behaviour of the IC is unpredictable.

To switch to encoder operation mode, UserControl has to be set to $3. Then 50 frames are encoded and sent via the PIO interface. This is repeated until the UserControl register is changed. If the transmission of headers is enabled, each page of 50 frames is preceeded by a header frame as shown in Table 3–7.

To switch off the encoder, UserControl has to be set to $0. Then the encoding and sending of frames continues until the end of the current page and the operation mode is set to stop.

3.5.2.3. Decoder Operation

The routines for the G.729 decoder mode are completely located in the MAS 3504D firmware. So there is no need to download the encoder routine in a decode only application.

To switch to decoder operation mode, UserControl has to be set to $1. For decoding with slow speed, set UserControl to $11. For decoding with fast speed, set UserControl to $21. Then the decoder is requesting several frames via the PIO interface to fill its internal buffer. If enough data is available, 50 frames are decoded. This is repeated until the UserControl register is changed. If the transmission of headers is enabled, a header frame (as shown in Table 3–7) has to be sent before each page of 50 frames.

To switch off the decoder, UserControl has to be set to $0. Then the decoding of frames continues until the end of the current page and the operation mode is set to stop.

3.5.2.4. Pause and Mute

If the pause bit is set, the processing continues until the current page is finished and then en-/decoding is paused. The pause mode lasts until the pause bit is cleared again or the mode is set to 0.

If the mute bit is set, the output is muted immediately.

Note that the other bits of the UserControl register have to stay on their old values when switching to pause mode.

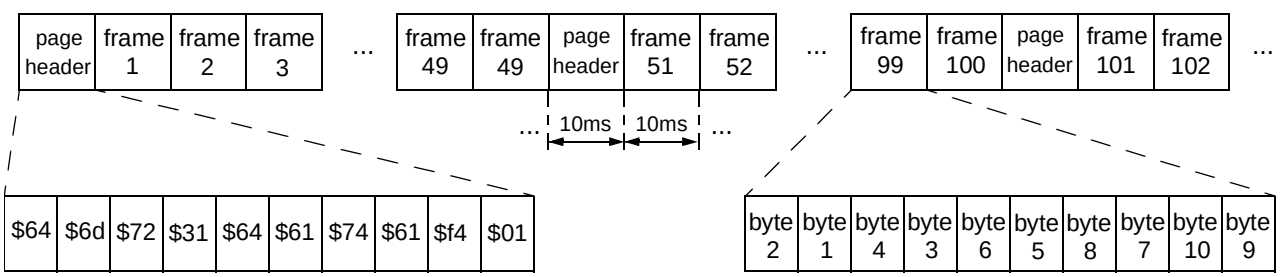


Fig. 3–2: Schematic timing of the data transmission with preceeding header

3.5.3. Volume Control (Reg. $fc)

Volume control is implemented in the MAS 3504D. It allows to adjust the output volume linear from $0 (silence) to $7ffff (original volume).

3.5.4. Interface Control

All the interface control registers have to be written before the encoder or decoder is started by writing to the UserControl register. Otherwise they have no effect until the operation mode is changed.

3.5.4.1. Wordlength Control (Reg. $74)

A value of $0 sets wordlength on SDI and SDO interfaces to 32 bit. $1 sets wordlength to 16 bit.

3.5.4.2. Input Configuration (Reg. $61)

The content of this register is set on startup by the firmware. Additional to the Wordlength setting for the serial interfaces, some other settings can be made.

3.5.4.3. Output Configuration (Reg. $e1)

The content of this register is set on startup by the firmware. Additional to the Wordlength setting for the serial interfaces, some other settings can be made.

3.5.5. Hardware Control (Reg. $fa)

The HWControl register is used to set special operation options.

If the page headers bit is 0, a header frame is transfered in front of each page of 50 data frames. If the header bit is 1, all the frames are G.729 data frames.

Bits 2 and 1 are used to select input channels for encoding. If both bits are set to 0, the left and right channel are added to get the mono input signal. If only one of this bits is 1, only the corresponding channel is used as input.

Table 3–8: Detailed Register Usage

Address (hex)	Mode	Function	Default (hex)	Name
61	w	Configuration of the I^2S audio input interface bit[19:12] not used, set to 0 bit[11] additional delay of data related to word strobe 0 no delay 1 1 bit delay bit[10:6] not used, set to 0 bit[5] input word strobe signal 0 standard timing 1 inverted timing bit[4:3] not used, set to 0 bit[2] input clock signal 0 standard timing 1 inverted timing bit[1:0] not used, set to 0	4	InputConfig
74	w	Serial output interface wordlength bit[19:1] not used, set to 0 bit[0] wordlength 0 32 bit/sample 1 16 bit/sample	0	Wordlength

Table 3–8: Detailed Register Usage

Address (hex)	Mode	Function	Default (hex)	Name
8e	w	DC/DC operation control bit[19:17] not used, set to 0 bit[16:14,9] output voltage / internal voltage monitor (PUP signal becomes inactive when output is below the monitoring voltage) 111,0: output voltage 3,5 V; internal voltage monitor 3,3 110,0: 3,4; 3,2 101,0: 3,3; 3,1 100,0: 3,2; 3,0 011,0: 3,1; 2,9 010,0: 3,0; 2,8 001,0: 2,9; 2,7 000,0: 2,8; 2,6 111,1: 2,7; 2,5 110,1: 2,6; 2,4 101,1: 2,5; 2,3 100,1: 2,4; 2,2 011,1: 2,3; 2,1 010,1: 2,2; 2,0 001,1: 2,1; 1,9 000,1: 2,0; 1,8 bit[13:10,8] DC/DC-converter switching frequency f_{SW} [kHz] bit[13:10] / bit[8]=0 / bit[8]=1 1111: 196; 297 1110: 200; 307 1101: 204; 317 1100: 209; 329 1011: 214; 341 1010: 219; 354 1001: 224; 368 1000: 230; 384 0111: 236; 400 0110: 242; 418 0101: 249; 438 0100: 256; 460 0011: 263; 485 0010: 271; 512 0001: 279; 542 0000: 288; 576 bit[7:0] not used, set to 0	8000	DCCF

Table 3–8: Detailed Register Usage

Address (hex)	Mode	Function	Default (hex)	Name
e1	w	Configuration of the I^2S audio output interface bit[19:15] not used, set to 0 bit[14] output clock signal 0 standard timing 1 inverted timing bit[13:12] not used, set to 0 bit[11] additional delay of data related to word strobe 0 no delay 1 1 bit delay bit[10:6] not used, set to 0 bit[5] output word strobe signal 0 standard timing 1 inverted timing bit[4:0] not used, set to 0	4000	OutputConfig
fa	w	Special operation options bit[19:3] not used, set to 0 bit[2:1] input channel matrixing 00 add left/right channel 01 input only from right channel 10 input only from left channel 11 not allowed bit[0] page headers 0 enable 1 disable	0	HWControl
fc	w	Output volume bit[19:0] linear volume level	7ffff	Volume
fd	w	Operation mode selection bit[19:6] not used, set to 0 bit[5:4] decoding speed 00 8 kHz (normal) 01 6 kHz (slow) 10 12 kHz (fast) 11 not allowed bit[3] mute audio output 0 disable 1 enable bit[2] pause encoder/decoder 0 disable 1 enable bit[1:0] mode 00 idle 01 decode 10 not allowed 11 encode	0	UserControl

4. Specifications

4.1. Outline Dimensions

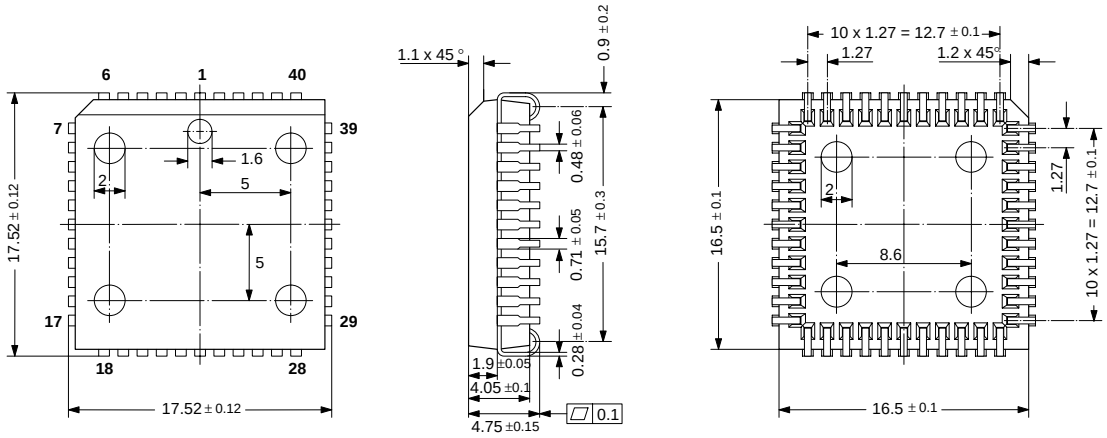


Fig. 4–1:
44-Pin Plastic Leaded Chip Carrier Package
(PLCC44)
Weight approximately 2.5 g
Dimensions in mm

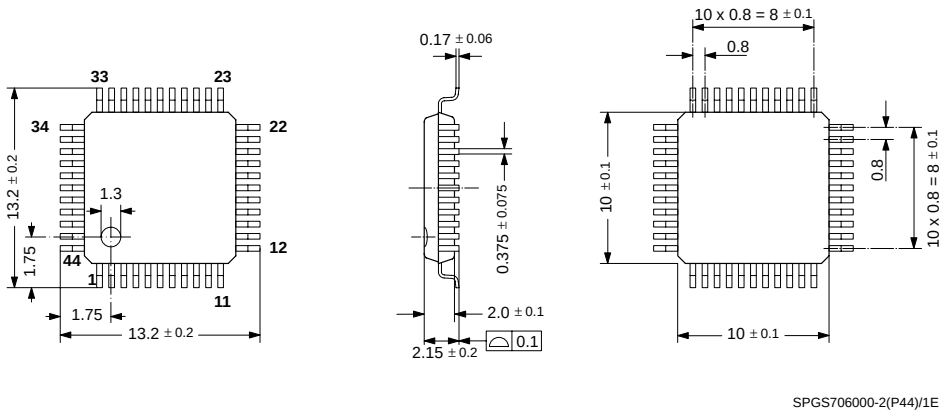


Fig. 4–2:
44-Pin Plastic Quad Flat Package
(PMQFP44)
Weight approximately 0.4 g
Dimensions in mm

Note: Start pin and orientation of pin numbering is different for PLCC and PMQFP packages!

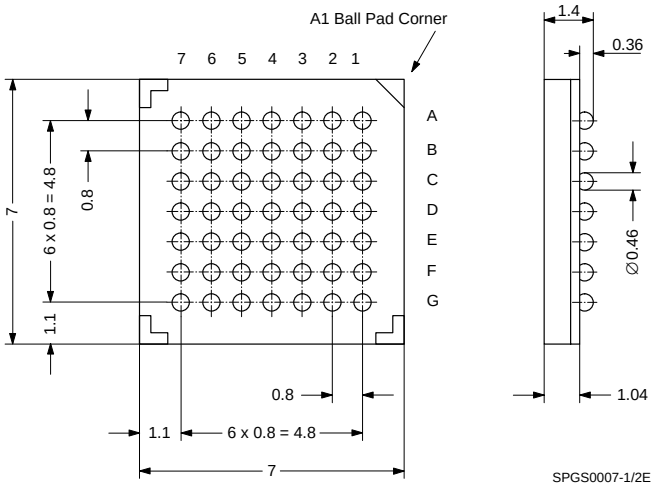


Fig. 4–3:
49-Ball Plastic Grid Array
(PBGA49)
Weight approximately 0.13 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC not connected, leave vacant
LV If not used, leave vacant
X obligatory, pin must be connected as described in application information

VDD connect to positive supply
VSS connect to ground

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin No. PBGA 49-ball	Pin Name Test Alias in ()	Type	Connection (If not used)	Short Description
1	6	C3	TE	IN	VSS	Test Enable
2	5	C2	$\overline{\text{POR}}$	IN	X	Reset, Active Low
3	4	B1	I2CC	IN/OUT	X	I^2C Clock Line
4	3	D2	I2CD	IN/OUT	X	I^2C Data Line
5	2	C1	VDD	SUPPLY	X	Positive Supply for Digital Parts
6	1	D1	VSS	SUPPLY	X	Ground Supply for Digital Parts
7	44	E2	DCEN	IN	VSS	Enable DC/DC Converter
8	43	E1	$\overline{\text{EOD}}$	OUT	LV	PIO End of DMA, Active Low
9	42	F2	$\overline{\text{RTR}}$	OUT	LV	PIO Ready to Read, Active Low
10	41	F1	$\overline{\text{RTW}}$	OUT	LV	PIO Ready to Write, Active Low
11	40	G1	DCSG	SUPPLY	VSS	DC Converter Transistor Ground
12	39	E3	DCSO	OUT	VSS	DC Converter Transistor Open Drain
13	38	F3	VSENS	IN	VDD	DC Converter Voltage Sense
14	37	G2	PR	IN	X	PIO-DMA Request or Read/$\overline{\text{Write}}$

Pin No.			Pin Name	Type	Connection	Short Description
PMQFP 44-pin	PLCC 44-pin	PBGA 49-ball	Test Alias in ()		(If not used)	
15	36	F4	$\overline{PCS}$	IN	X	PIO Chip Select, Active Low
16	35	G3	PI19	IN/OUT	LV	PIO Data [19] data bit [7], MSB
17	34	E4	PI18	IN/OUT	LV	PIO Data [18] data bit [6]
18	33	G4	PI17	IN/OUT	LV	PIO Data [17] data bit [5]
19	32	F5	PI16	IN/OUT	LV	PIO Data [16] data bit [4]
20	31	G5	PI15	IN/OUT	LV	PIO Data [15] data bit [3]
21	30	F6	PI14	IN/OUT	LV	PIO Data [14] data bit [2]
22	29	G6	PI13	IN/OUT	LV	PIO Data [13] data bit [1]
23	28	E5	PI12	IN/OUT	LV	PIO Data [12] data bit [0]
24	27	E6	SOD (PI11)	OUT	LV	Serial Output Data
25	26	F7	SOI (PI10)	OUT	LV	Serial Output Frame Identification
26	25	D6	SOC (PI9)	OUT	LV	Serial Output Clock
27	24	E7	PI8	IN	LV	Not used
28	23	D7	XVDD	SUPPLY	X	Positive Supply of Output Buffers
29	22	C6	XVSS	SUPPLY	X	Ground of Output Buffers
30	21	C7	SID (PI7)	IN	VSS	Serial Input Data
31	20	B6	SII (PI6)	IN	VSS	Serial Input Frame Identification
32	19	B7	SIC (PI5)	IN	VSS	Serial Input Clock
33	18	A7	PI4	IN	LV	Not used
34	17	B5	PI3	IN	LV	Not used
35	16	A6	PI2	IN	LV	Not used
36	15	B4	PI1	IN	LV	Not used
37	14	A5	PI0	IN	LV	Not used
38	13	C4	CLKO	OUT	LV	Not used
39	12	A4	PUP	OUT	LV	Power Up (status of voltage supervision)
40	11	B3	WSEN	IN	X	Enable DSP and Start DC/DC Converter
41	10	A3	WRDY	OUT	LV	If WSEN = 0: valid clock input at CLKI If WSEN = 1: clock synthesizer PLL locked
42	9	B2	AVDD	SUPPLY	VDD	Supply for Analog Circuits
43	8	A2	CLKI	IN	X	Clock Input
44	7	A1	AVSS	SUPPLY	VSS	Ground Supply for Analog Circuits

4.2.1. Pin Descriptions

4.2.1.1. Power Supply Pins

Connection of all power supply pins is mandatory for the function of the MAS 3504D.

VDD **SUPPLY**
VSS **SUPPLY**

The VDD/VSS pair is internally connected with all digital modules of the MAS 3504D.

XVDD **SUPPLY**
XVSS **SUPPLY**

The XVDD/XVSS pins are internally connected with the pin output buffers.

AVDD **SUPPLY**
AVSS **SUPPLY**

The AVDD/AVSS pair is connected internally with the analog blocks of the MAS 3504D, i.e. clock synthesizer and supply voltage supervision circuits.

4.2.1.2. DC/DC Converter Pins

DCEN **IN**

The DCEN input signal enables the DC/DC converter operation.

DCSG **SUPPLY**

The 'DC converter Signal Ground' pin is used as a basepoint for the internal switching transistor of the DC/DC converter. It must always be connected to ground.

DCSO **OUT**

DCSO is an open drain output and should be connected with external circuitry (inductor/diode) to start the DC/DC converter. When the DC/DC converter is not used, it has to be connected to VSS.

VSENS **IN**

The VSENS pin is the input for the DC/DC converter feedback loop. It must be connected directly with the Schottky diode and the capacitor as shown in Fig. 2–1. When the DC/DC converter is not used, it has to be connected to VDD.

4.2.1.3. Control Lines

I2CC **SCL** **IN/OUT**
I2CD **SDA** **IN/OUT**

Standard I^2C control lines. Normally there are Pullup-resistors tied from each line to VDD.

4.2.1.4. Parallel Interface Lines

4.2.1.4.1. PIO Handshake Lines

'PIO handshake lines' are used in operation mode. PIO-DMA mode is used in input mode and µP mode in output mode.

$\overline{\text{PCS}}$ **IN**

The 'PIO chip select' is driven from microcontroller to activate data output from MAS 3504D to the bus. Data is output to the bus on the falling edge of $\overline{\text{PCS}}$ and is removed on the rising edge of $\overline{\text{PCS}}$.

PR **IN**

The 'PIO request' must be set to '1' to validate data output from MAS 3504D.

$\overline{\text{RTR}}$ **OUT**

'Ready to read' is driven from the MAS 3504D in PIO/DMA input mode.

$\overline{\text{RTW}}$ **OUT**

'Ready to write' is driven from MAS 3504D to indicate that data is available in PIO output mode.

$\overline{\text{EOD}}$ **OUT**

'End of DMA' is supported by the built-in firmware in PIO-DMA input mode.

4.2.1.4.2. PIO Data Lines

PI19...PI12 **PARALLEL DATA** **OUT/IN**

These pins are used to send or receive compressed data.

4.2.1.5. Voltage Supervision And Other Functions

CLKI **IN**

This is the clock input of the MAS 3504D. CLKI should be a buffered output of a crystal oscillator. Standard clock frequency is 18.432 MHz.

CLKO **OUT**

This pin has no function.

PUP **OUT**

The PUP output indicates that the power supply voltage exceeds its minimal level (software adjustable).

WSEN **IN**

WSEN enables DSP operation and switches on the DC/DC-converter.

WRDY **OUT**

WRDY has two functions depending on the state of the WSEN signal.

If WSEN = ’0’, it indicates that a valid clock has been recognized at the CLKI clock input.

If WSEN = ’1’, the WRDY output will be set to ‘0’ until the internal clock synthesizer has locked to the incoming audio data stream, and thus, the CLKO clock output signal is valid.

4.2.1.6. Serial Input Interface

SID **IN**
SII **IN**
SIC **IN**

Data, Frame Indication, and Clock line of the serial input interface. The SII indicates whether the left or the right audio sample is transmitted.

4.2.1.7. Serial Output Interface

SOD **OUT**
SOI **OUT**
SOC **OUT**

Data, Frame Indication, and Clock line of the serial output interface. The SOI indicates whether the left or the right audio sample is transmitted.

4.2.1.8. Miscellaneous

$\overline{\text{POR}}$ **IN**

The Power On Reset pin is used to reset the digital parts of the MAS 3504D. $\overline{\text{POR}}$ is a low active signal.

TE **IN**

The TE pin is for production test only and must be connected with VSS in all applications.

4.2.2. Pin Configurations

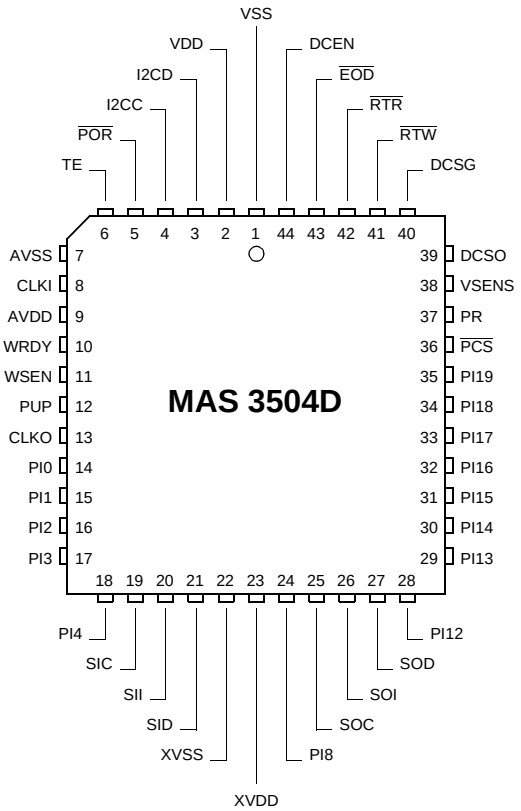


Fig. 4–4: 44-pin PLCC package

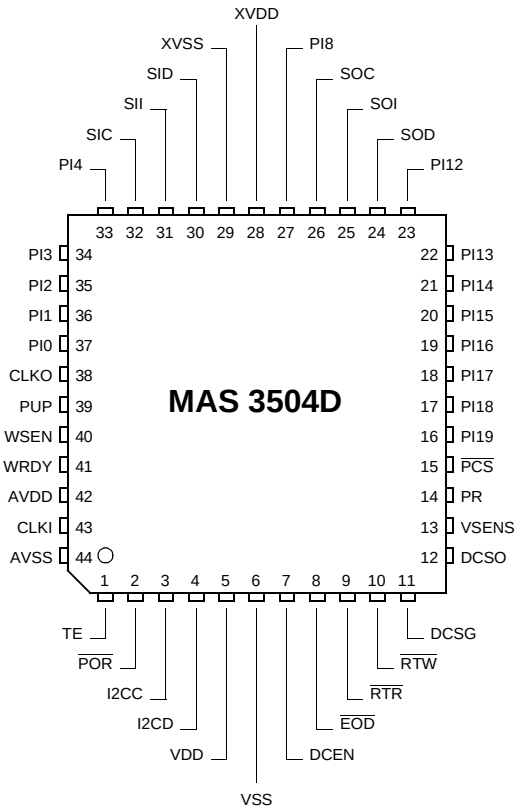


Fig. 4–5: 44-pin PMQFP package

4.2.3. Internal Pin Circuits

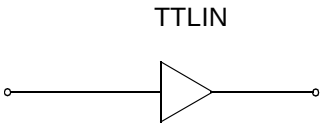


Fig. 4–6: Input pins $\overline{PCS}$, PR

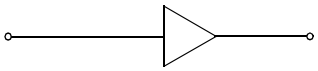


Fig. 4–7: Input pin TE, DCEN

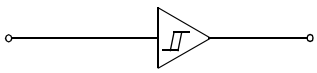


Fig. 4–8: Input pins WSEN, $\overline{POR}$

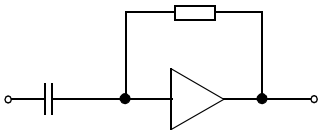


Fig. 4–9: Input pin CLKI

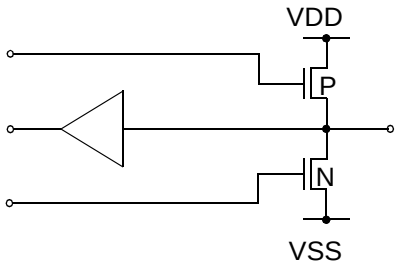


Fig. 4–10: Input/Output pins PI0...PI4, PI8, SOC, SOI, SOD, PI12...PI19

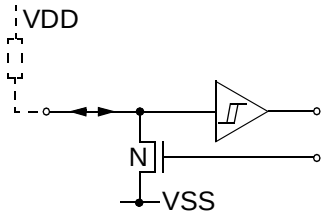


Fig. 4–11: Input/Output pins I2CC, I2CD

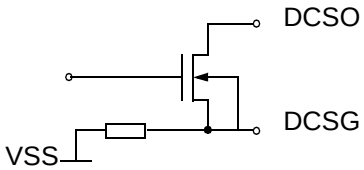


Fig. 4–12: Input/Output pins DCSO, DCSG

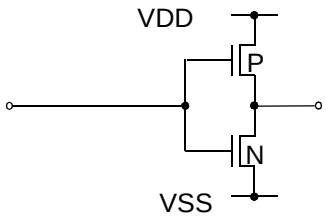


Fig. 4–13: Output pins WRDY, $\overline{RTW}$, $\overline{EOD}$, $\overline{RTR}$, CLKO, PUP

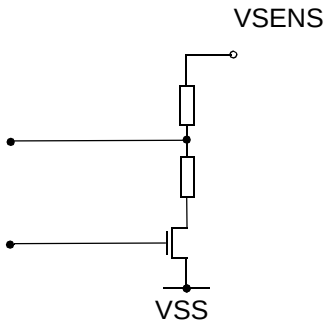


Fig. 4–14: Input pin VSENS

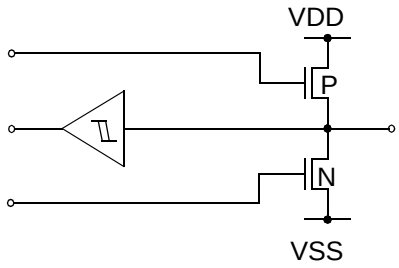


Fig. 4–15: Input/Output pins SIC, SII, SID

4.2.4. Electrical Characteristics

4.2.4.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		–30	85	°C
T_S	Storage Temperature		–40	125	°C
P_{MAX}	Power dissipation for all packages	VDD, XVDD, AVDD		400	mW
V_{SUP}	Supply voltage	VDD, XVDD, AVDD		5.5	V
V_{Idig}	Input voltage, all digital inputs		–0.3	V_{SUP} +0.3	V
I_{Idig}	Input current, all digital inputs		–20	+20	mA
I_{Out}	Current, all digital outputs			0.5	A
I_{OutDC}	Current	DCSO		1.5	A

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.2.4.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient temperature range		–30		85	°C
V_{SUP}	Supply voltage for G.729 decoder operation and download software	VDD, XVDD, AVDD	2.7	3.0	3.6	V
	Supply voltage for G.729 encoder operation		3.0	3.3	3.6	V
Reference Frequency Generation						
CLK_F	Clock Frequency	CLKI		18.432		MHz
CLK_{I_V}	Clock Input Voltage		0		V_{SUP}	V
CLK_{Amp}	Clock Amplitude		0.5			V_{pp}
Levels						
I_{IL27}	Input Low Voltage @V_{SUP} = 2.7 V ... 3.6 V	POR I2CC, I2CD, DCEN, WSEN			0.4	V
I_{IH36}	Input High Voltage @V_{SUP} = 2.7 V ... 3.6 V		1.8			V
I_{IH33}	Input High Voltage @V_{SUP} = 2.7 V ... 3.3 V		1.7			V
I_{IH30}	Input High Voltage @V_{SUP} = 2.7 V ... 3.0 V		1.6			V
I_{ILD}	Input Low Voltage	PI<I>[1], SII, SIC, SID, PR, PCS, TE,			0.4	V
I_{IHD}	Input High Voltage		V_{SUP}– 0.5			V
T_{rf}	Rise / Fall time of digital inputs	PI<I>, SII, SIC, SID, PR, PCS, CLKI			10	ns
D_{cycle}	Duty cycle of clock inputs	SIC, CLKI	40	50	60	%
DC-DC converter external circuitry						
C_1	Blocking Capacitor (25 mΩ ESR)[2]	VSENS, DCSG		330		µF
V_F	Schottky Diode Forward voltage[3]	DCSO, VSENS	0.35		0.45	V
L	Inductance of Ferrite ring core coil[4] (50 mΩ),VAC 616/103	DCSO		20		µH

[1] i = 0 to 4, 8 , 12 to 19
[2] Sanyo Oscon 6SA330M
(distributed by Endrich Bauelemente, D-72202 Nagold-Iselshausen, www.endrich.com)
[3] ZETEX ZMCS1000
(distributed by ZETEX, D-81673 München, europe.sales@zetex.com), standard Schottky 1N5817
[4] C8 R/4L, SDS0604 (distributed by Endrich Bauelemente, s.a.), VAC 616/103

4.2.4.3. Characteristics

at T_A = –30 to 85 °C, V_{SUP} = 3.0 to 3.6 V, typ. values at T_A = 27 °C, V_{SUP} = 3.3 V, CLK_F = 18.432 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage							
I_{SUP}	Current Consumption	VDD, XVDD, AVDD		46		mA	3.3 V, G.729 encoding
				25		mA	3.3 V, G.729 decoding
				15		mA	3.3 V, waiting mode
Digital Outputs and Inputs							
V_{DOL}	Output Low Voltage	PI<I>[1], SOI, SOC, SOD, $\overline{EOD}$, $\overline{RTR}$, $\overline{RTW}$, WRDY, PUP, CLKO			0.3	V	@ I_{LOAD} = 6 mA
V_{DOH}	Output High Voltage		V_{SUP}-0.3			V	@ I_{LOAD} = 6 mA
C_{DIGL}	Input Capacitance	PI<I>, SII, SIC, SID, PR, PCS, CLKI			7	pF	
I_{DLeak}	Digital Input Leakage Current		–1		1	µA	0 V < V_{pin} < V_{SUP}

[1] i = 0 to 4, 8 , 12 to 19

4.2.4.3.1. I²C Characteristics

at T_A = –30 to 85 °C, V_{SUP} =3.0 to 3.6 V, typ. values at T_A = 27 °C, V_{SUP} = 3.3 V, CLK_F = 18.432 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R_{ON}	Output Resistance	I2CC, I2CD			60	Ω	I_{LOAD} = 5 mA, V_{SUP} = 2.7 V
f_{I2C}	I²C Bus Frequency	I2CC			400	kHz	
t_{I2C1}	I²C START Condition Setup Time	I2CC, I2CD	300			ns	
t_{I2C2}	I²C STOP Condition Setup Time	I2CC, I2CD	300			ns	
t_{I2C3}	I²C Clock Low Pulse Time	I2CC	1250			ns	
t_{I2C4}	I²C Clock High Pulse Time	I2CC	1250			ns	
t_{I2C5}	I²C Data Hold Time before Rising Edge of Clock	I2CC	80			ns	
t_{I2C6}	I²C Data Hold Time after Falling Edge of Clock	I2CC	80			ns	
V_{I2COL}	I²C Output Low Voltage	I2CC, I2CD			0.3	V	I_{LOAD} = 5 mA
I_{I2COH}	I²C Output High Leakage Current	I2CC, I2CD			1	uA	V_{I2CH} = 3.6 V
t_{I2COL1}	I²C Data Output Hold Time after Falling Edge of Clock	I2CC, I2CD	20			ns	
t_{I2COL2}	I²C Data Output Setup Time before Rising Edge of Clock	I2CC, I2CD	250			ns	f_{I2C} = 400 kHz

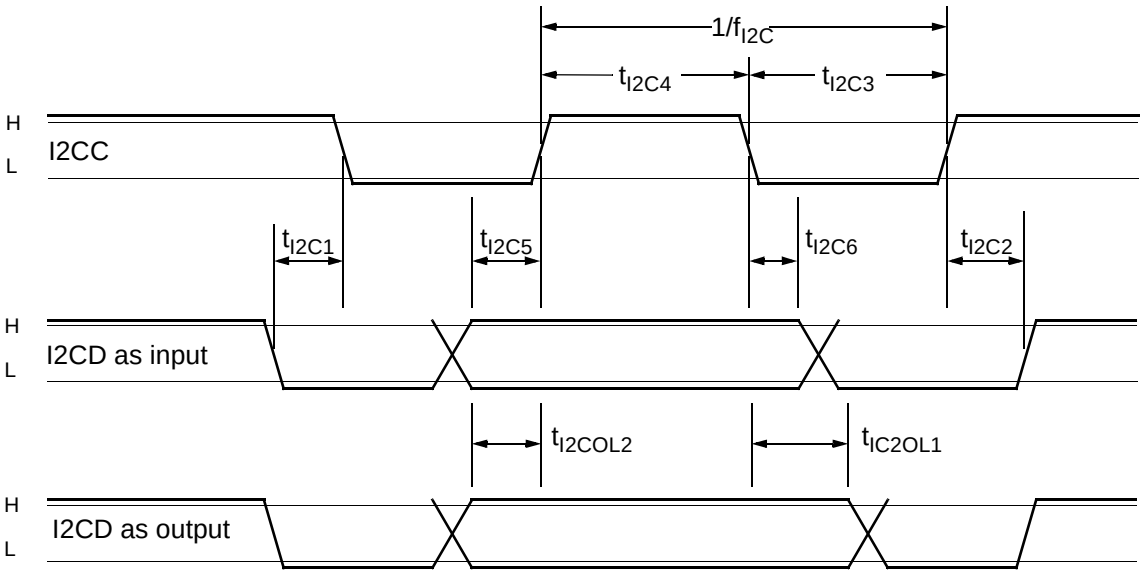


Fig. 4–16: I²C timing diagram

4.2.4.3.2. I^2S Bus Characteristics – SDI

at T_A = –30 to 85 °C, V_{SUP} = 3.0 to 3.6 V, typ. values at T_A = 27 °C, V_{SUP} = 3.3 V, CLK_F = 18.432 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SICLK}	I^2S Clock Input Period	SIC	960			ns	
t_{SIIDS}	I^2S Data SetupTime before Falling Edge of Clock	SIC, SID	50		t_{SICLK}-100	ns	
t_{SIIDH}	I^2S Data Hold Time	SID	50			ns	
t_{bw}	Burst Wait Time	SIC, SID	480				

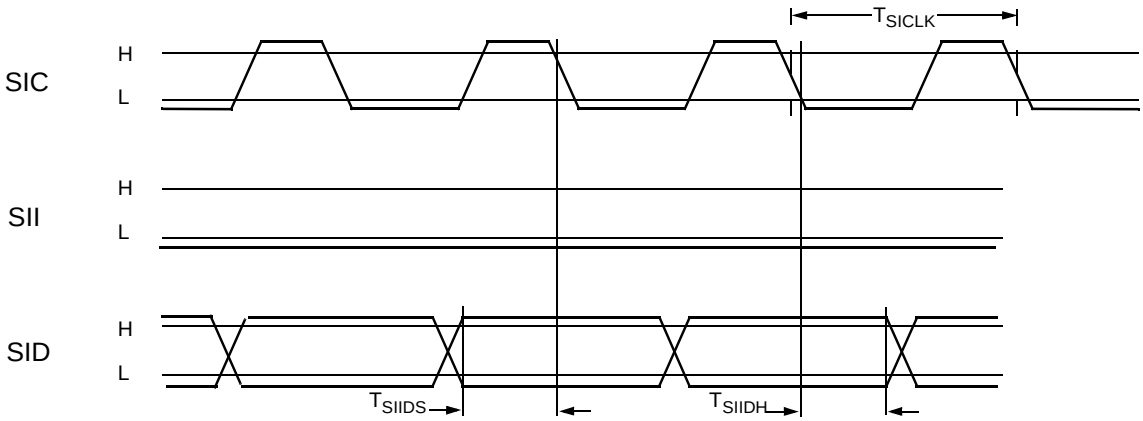


Fig. 4–17: Serial input

4.2.4.3.3. I^2S Characteristics – SDO

at T_A = –30 to 85 °C, V_{SUP} = 3.0 to 3.6 V, typ. values at T_A = 27 °C, V_{SUP} = 3.3 V, CLK_F = 18.432 MHz, duty cycle = 50 %

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SOCLK}	I^2S Clock Output Period	SOC		1953		ns	8 kHz stereo 32 bit/sample
t_{SOISS}	I^2S Wordstrobe Hold Time after Falling Edge of Clock	SOC, SOI	10		t_{SOCLK}/2	ns	
t_{SOODC}	I^2S Data Hold Time after Falling Edge of Clock	SOC, SOD	10		t_{SOCLK}/2	ns	

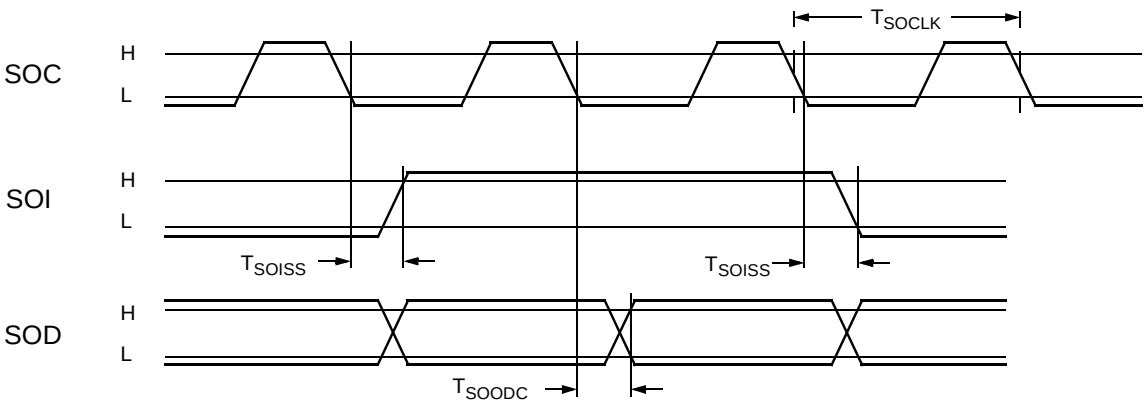


Fig. 4–18: Serial output SOI

4.2.4.4. DC/DC Converter Characteristics

at T_A = –30 to 85 °C, V_{SUP} = 3.0 V, CLK_F = 14.725 MHz, f_{sw} = 230 kHz, typ. values at T_A = +27 °C
Note: The following characterizations were made with voltage and clock input that is not usable for G.729 applications.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IN1}	Minimum Start-Up Input Voltage			0.9	1.0	V	I_{LOAD} = 0 mA DCCF = $08000 (Reset)
V_{IN2}	Minimum Operating Voltage			0.6	0.8	V	I_{LOAD} = 55 mA, DCCF = $08000 (Reset)
				1.3	1.8	V	I_{LOAD} = 250 mA, DCCF = $08000 (Reset)
V_{OUT}	Output Voltage		2.0 [1)]		3.5	V	(see Section 4.2.4.5.)
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line Regulation			1		%	V_{IN} = 1.0...3.0 V, I_{LOAD} = 55mA
$dV_{OUT}/dI_{LOAD}/V_{OUT}$	Load Regulation			0.6		%	V_{IN} = 1.2 V, I_{LOAD} = 0...55 mA, f_{SW} = 230 kHz
$dV_{OUT}/dI_{LOAD}/V_{OUT}$	Load Regulation			1.2		%	V_{IN} = 1.2 V, I_{LOAD} = 0...55 mA, f_{SW} = 165 kHz
h_{max}	Maximum Efficiency			90		%	
I_{SUPPLY}	Supply Current			1.1	5	mA	V_{IN} = 3.0 V, I_{LOAD} = 0, includ. switch current
$I_{L,MAX}$	Inductor Current Limit	DCSO, DCSG		1.0	1.4	A	
R_{ON}	Switch On-Resistance	DCSO, DCSG		0.2	0.4	Ω	T_j = 25 °C
I_{LEAK}	Switch Leakage Current	DCSO, DCSG		0.1	1	µA	T_j = 25 °C
f_{SW}	Switch Frequency	DCSO, DCSG	156	230	230	kHz	Depending on DCCF
t_{START}	Start Up Time to PUP-Enable	DCEN, PUP		8		ms	V_{IN} = 1.0 V, I_{LOAD} = 1 mA, PUPLIM = 010 (Reset)
$V_{STARTTRAN}$	Start-Up to Normal Mode Transition Voltage	VSENSE		1.9		V	

[1)] see Section 4.2.4.2.

All measurements are made with a C8 R/4L 20 µH, 25 mΩ ferrite ring-core coil, Zetex ZLMCS1000 Schottky diode, and Sanyo/Oscon 6SA330M 330 µF, 25 mΩ ESR capacitors at input and output (see Section 4.2.4. on page 28).

4.2.4.5. Typical Performance Characteristics

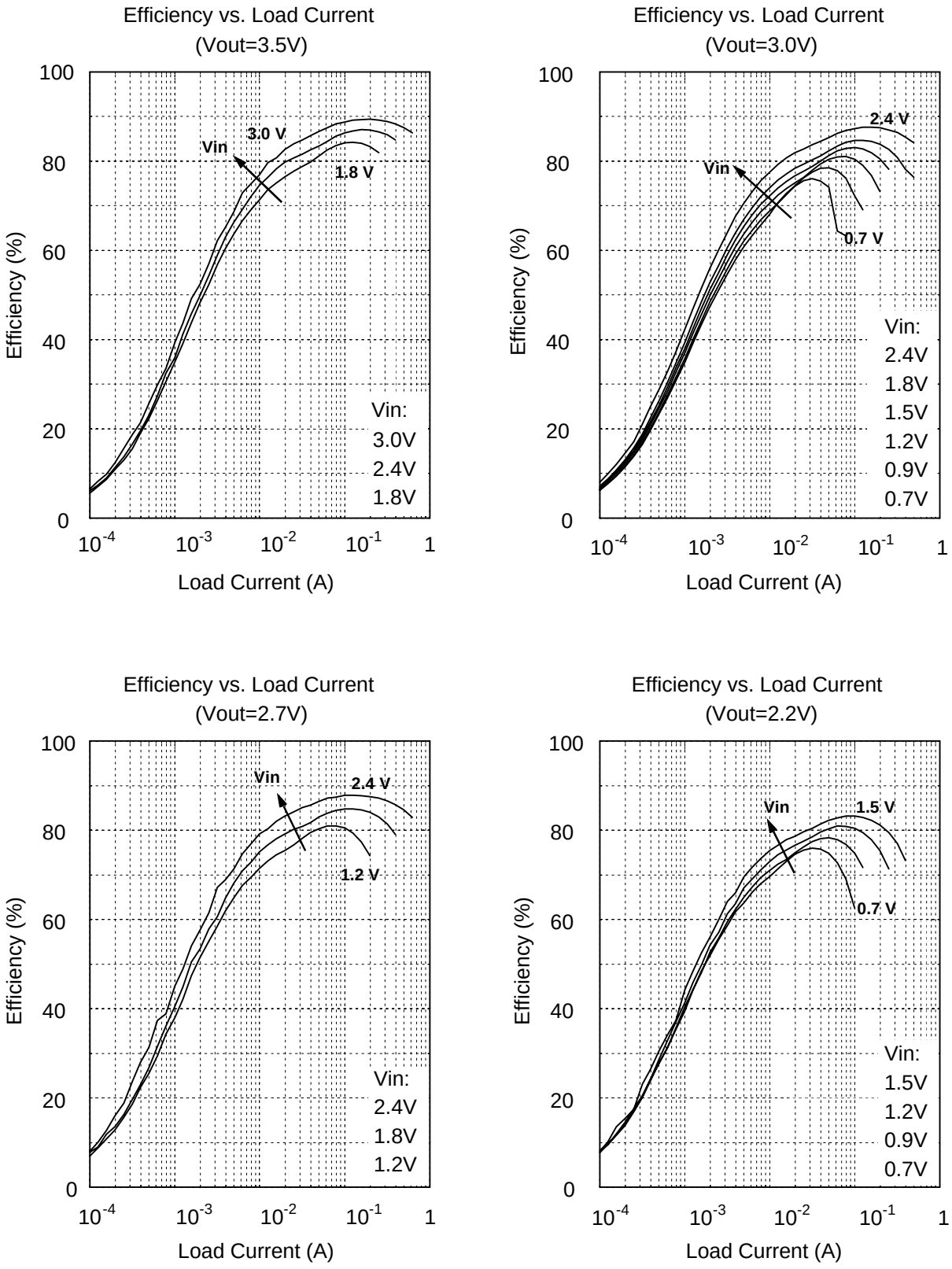


Fig. 4–19: Efficiency vs. Load Current

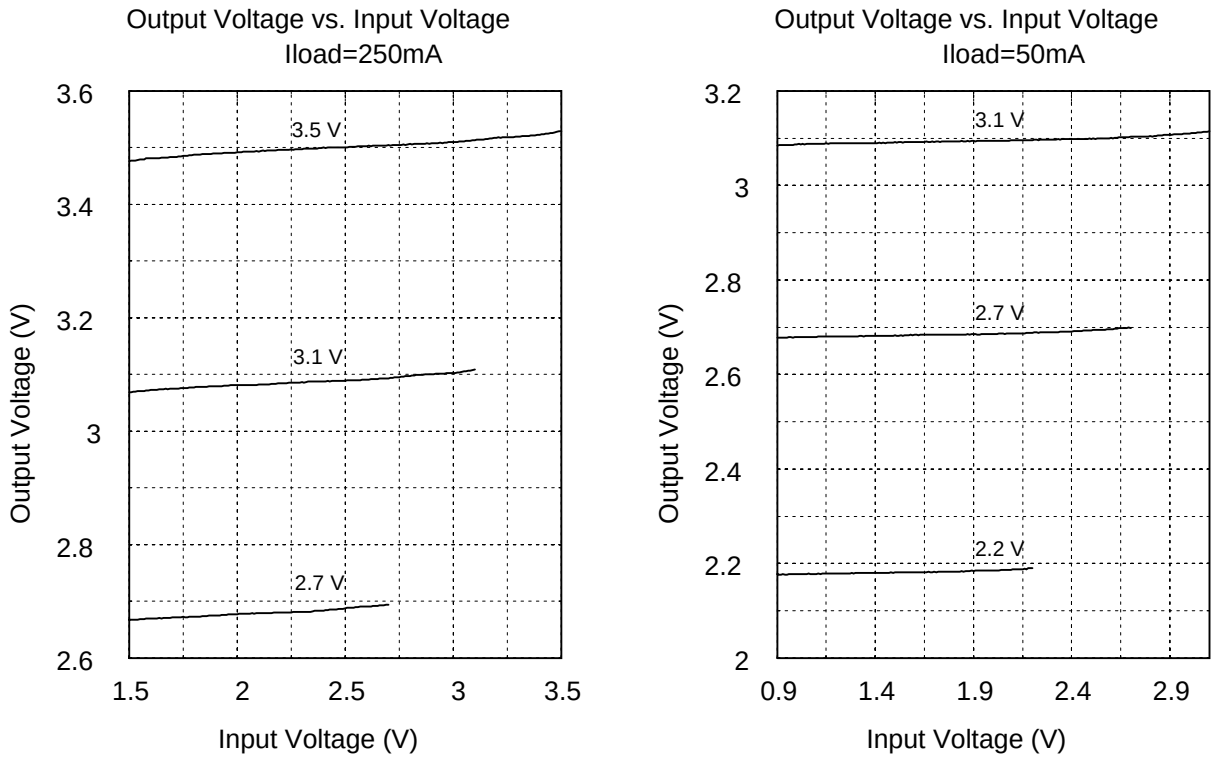


Fig. 4–20: Output Voltage vs. Input Voltage

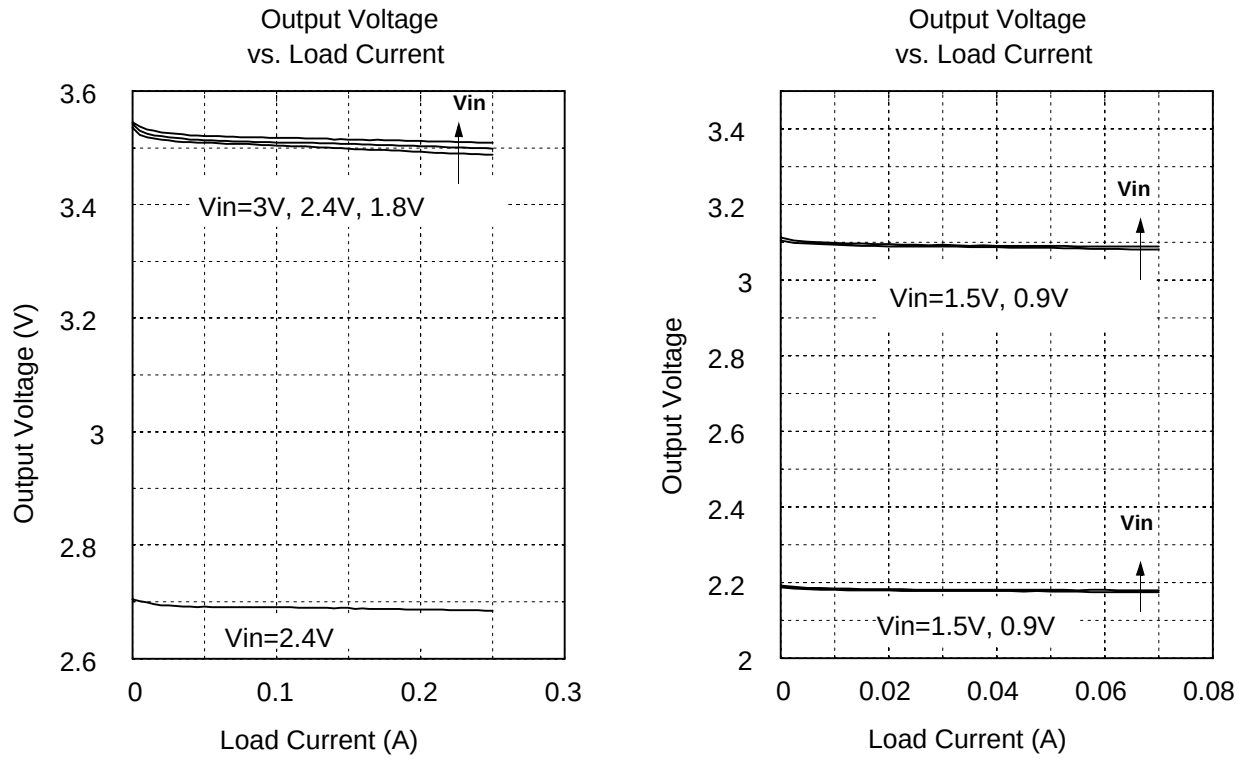


Fig. 4–21: Output Voltage vs. Load Current

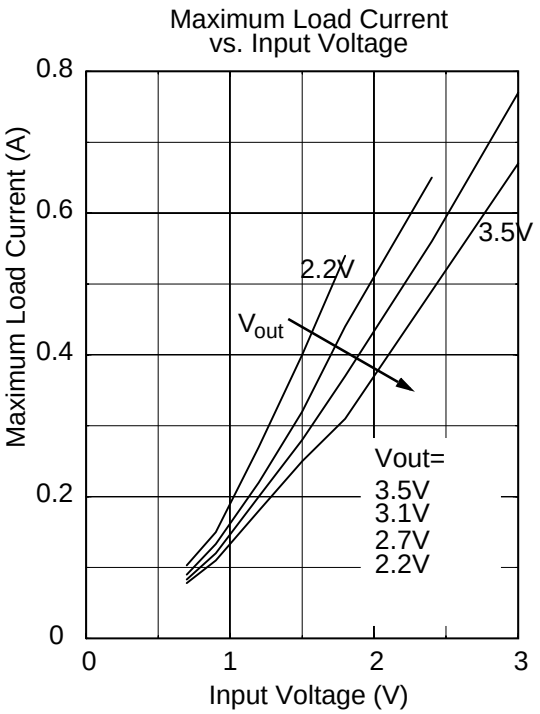


Fig. 4–22: Maximum Load Current vs. Input Voltage

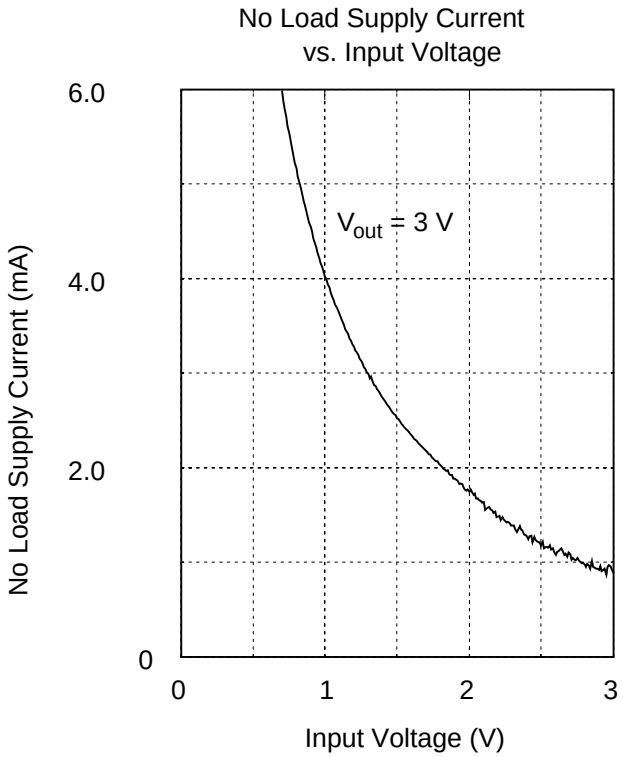
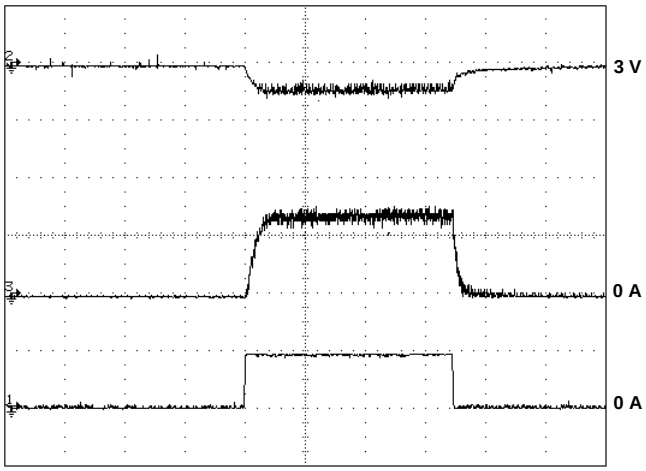


Fig. 4–23: No Load Supply Current vs. Input Voltage

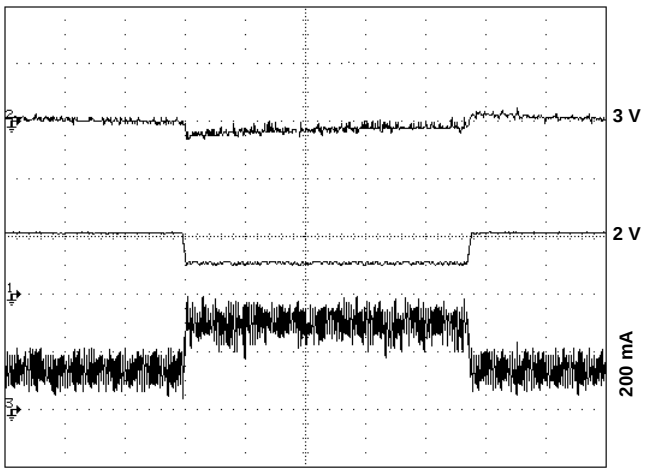


500.00 µs/Div

V_{in} = 1.2 V; V_{out} = 3 V

1	Load Current	200.0 mA/Div
2	Output Voltage	100.0 mV/Div / AC-coupled
3	Inductor Current	500.0 mA/Div

Fig. 4–24: Load Transient-Response

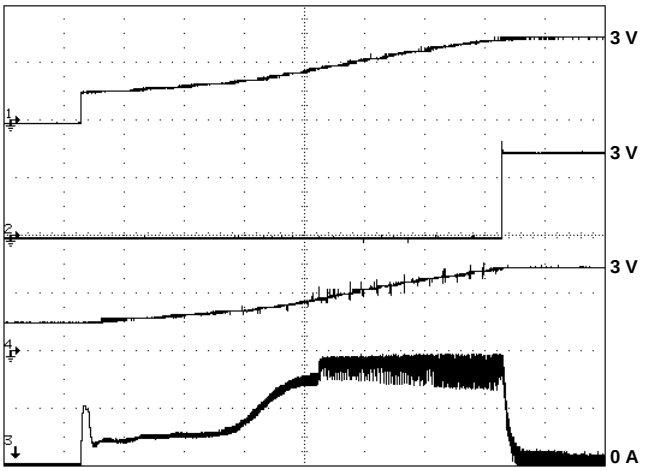


5.00 ms/Div

I_{load} = 100 mA; V_{out} = 3 V

1	V_{in}	2.000 V/Div
2	Output Voltage	50.00 mV/Div / AC-coupled
3	Inductor Current	200.0 mA/Div

Fig. 4–25: Line Transient-Response



500 µs/Div

V_{in} = 1 V; I_{load} = 0 mA

1	V (DCEN)	2.000 V/Div
2	V (PUP)	2.000 V/Div
3	Inductor Current	500.0 mA/Div
4	Output Voltage	2.000 V/Div

Fig. 4–26: Startup Waveform

5. Data Sheet History

1. Advance Information: “MAS 3504D G.729 Annex A Voice Codec”, March 10, 2000, 6251-522-1AI.
First release of the advance information.

2. Advance Information: “MAS 3504D G.729 Annex A Voice Codec”, Sept. 25, 2000, 6251-522-2AI.
Second release of the advance information.
Major changes:
“The respective paragraphs in sections 3., 3.3.5., 3.3.6., and 3.3.7. of the data sheet which state that reading from MAS 3504D via I^2C bus is not possible, are not valid.”

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Advance Information Supplement

Subject:	Change in Version A1
Data Sheet Concerned:	MAS 3504D 6251-522-1AI, Edition March 10, 2000
Supplement:	No. 1/ 6251-522-1AIS
Edition:	Sept. 25, 2000

Changes that apply to the MAS 3504D Version A1:

1. **Reading from MAS 3504D via I^2C is functional.**

The respective paragraphs in sections 3., 3.3.5, 3.3.6., and 3.3.7 of the data sheet which state that reading from MAS 3504D via I^2C bus is not possible, are not valid.