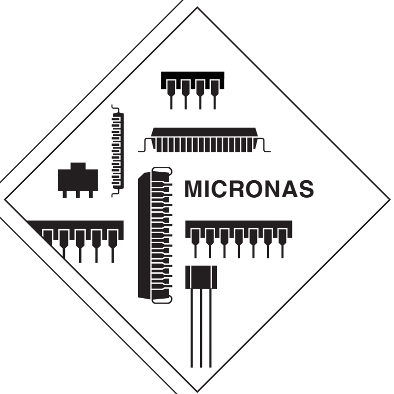

ADVANCE INFORMATION

MAS 35x9F
MPEG Layer 2/3, AAC Audio Decoder, G.729 Annex A Codec

Edition October 31, 2000
6251-505-2AI

MICRONAS

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MPEG Layer 2/3, AAC Audio Decoder,
G.729 Annex A Codec

Release Note: Revision bars indicate significant changes to the previous edition. This data sheet applies to MAS 35x9F version A2 .

1. Introduction

The MAS 35x9F is a single-chip, low-power MPEG layer 2/3 and MPEG2-AAC audio stereo decoder. It also contains the G.729 Annex A speech compression and decompression technology for use in memory-based or broadcast applications. Additional functionality is achievable via download software (e.g. CELP voice decoder, Micronas SC4 (ADPCM) encoder / decoder)

The MAS 35x9F decoding block accepts compressed digital data streams as serial bitstreams, or parallel format and provides serial PCM and/or S/PDIF output[1)] of decompressed audio. In addition to the signal processing function the IC incorporates a high-performance stereo D/A converter, headphone amplifiers, a stereo A/D converter, a microphone amplifier, and two DC/DC converters.

Thus, the MAS 35x9F provides a true '**ALL-IN-ONE**' solution that is ideally suited for highly optimized memory based portable music players with integrated speech decoding function.

In MPEG 1 (ISO 11172-3), three hierarchical layers of compression have been standardized. The most sophisticated and complex, layer 3, allows compression rates of approximately 12:1 for mono and stereo signals while still maintaining CD audio quality. Layer 2 (widely used in e.g. in DVD) achieves a compression of 8:1 without significant losses in audio quality.

The MAS 35x9F supports the 'Advanced Audio Coding' (AAC) that is also defined as aprt of MPEG 2. AAC provides compression rates up to 16:1. MPEG 2 defines several profiles for different applications. This IC decodes the 'low complexity profile' that is especially optimized for portable applications.

The MAS 35x9F also implements a voice encoder and decoder that is compliant to the ITU Standard G.729 Annex A.

SC4 is a proprietary Micronas speech codec technology that can be downloaded to the MAS 35x9F to allow recording and playing back speech at various sampling rates.

1.1. Features

Firmware

– MPEG 1/2 layer 2 and layer 3 decoder
– Extension to MPEG 2 layer 3 for low bit rates ("MPEG 2.5")
– Extraction of MPEG Ancillary Data
– MPEG 2 AAC[2)] decoder (low complexity profile)
– Master or slave clock operation
– Adaptive bit rates (bit rate switching)
– Intelligent power management (processor clock is dependent on sampling frequencies)
– Micronas G.729 Annex A speech compression and decompression
– SDMI-compliant security technology
– Stereo channel mixer
– Bass, treble and loudness function
– Micronas Dynamic Bass (MDB)
– Automatic Volume Control (AVC)

Interfaces

– 2 serial asynchronous interfaces for bitstreams and uncompressed digital audio
– Parallel handshake bit stream input
– Serial audio output via I^2S and related formats
– S/PDIF data input and output
– Controlling via I^2C interface

Hardware Features

– Two independent embedded DC/DC converters (e.g. for DSP and flash RAM supply)
– Low DC/DC converter start-up voltage (0.9 V)
– DC converter efficiency up to 95 %
– Battery voltage monitor
– Low supply voltage (down to 2.2 V)
– Low power dissipation (<70 mW)
– High-performance RISC DSP core
– On-chip crystal oscillator
– Hardware power management and power-off functions
– Microphone amplifier
– Stereo A/D converter for FM/AM-radio and speech input
– CD quality stereo D/A converter
– Headphone amplifier

– Noise and power-optimized volume
– External clock or crystal frequency of 13...20 MHz
– Standby current < 10 µA

[1] Not yet supported in version A2
[2] See License Note on page 4

1.2. Features of the MAS 35x9F Family

Feature	3509	3519	3529	3539	3549	3559
Layer 3 Decoder	X	X	X	X		
G.729 Encoder/Decoder	X	X			X	
AAC Decoder	X		X			X

1.3. Application Overview

The following block diagram shows an example application for the MAS 35x9F in a portable audio player device. Besides a simple controller and the external flash memories, all required components are integrated in the MAS 35x9F. The MAS 35x9F supports both speech and radio quality audio encoding, as well as compressed-audio decoding tasks.

Fig. 1–1 depicts a portable audio application that is power optimized. The two embedded DC/DC converters of the MAS 35x9F generate optimum power supply voltages for the DSP core and also for state-of-the art flash memories that typically require 2.7 to 3.3 V supply.

The performance of the DC/DC converters reaches efficiencies up to 95 %.

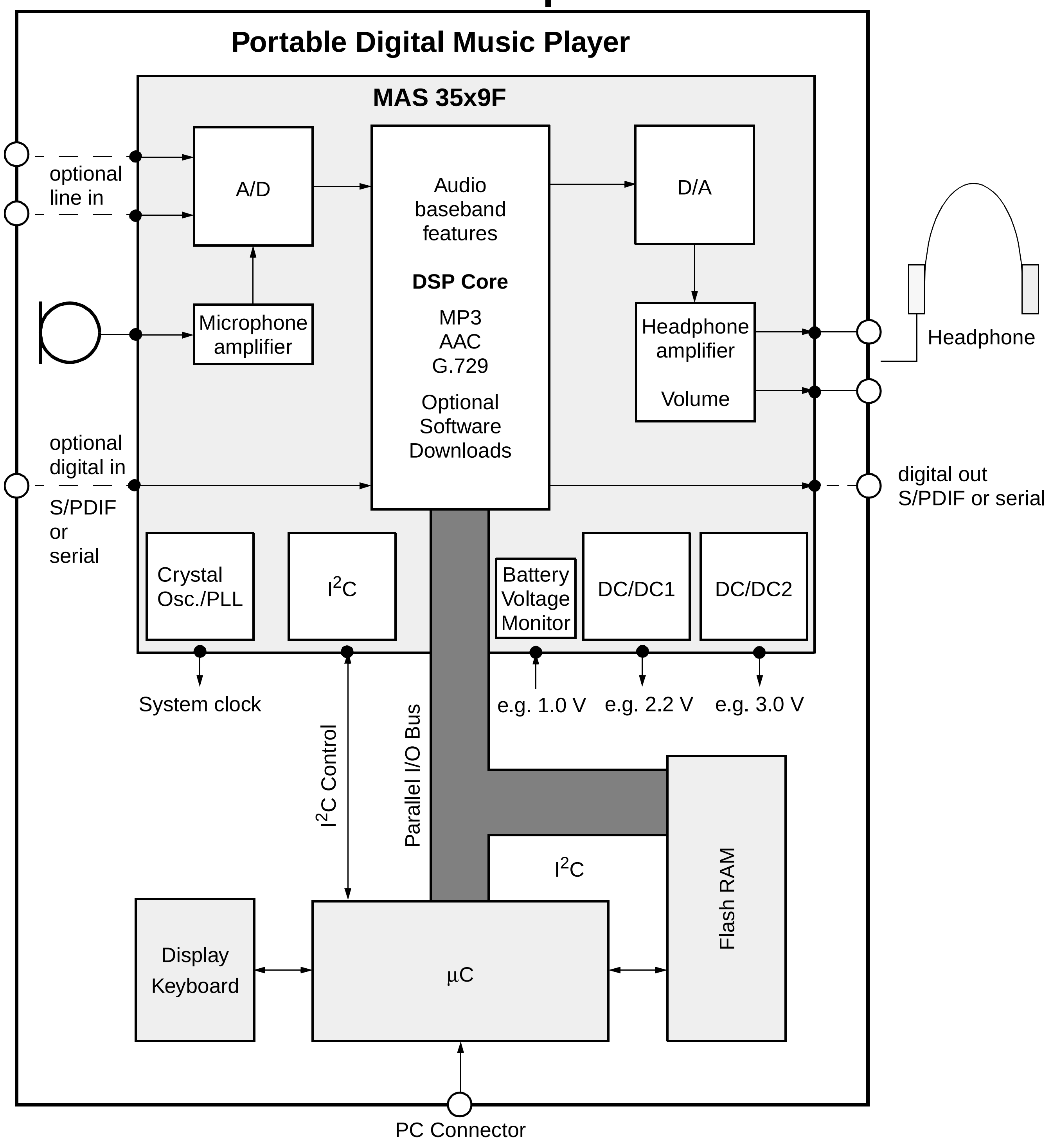


Fig. 1–1: Example application for the MAS 35x9F in a portable audio player device

2. Functional Description of the MAS 35x9F

2.1. Overview

The MAS 35x9F is intended for use in portable consumer audio applications. It receives S/PDIF, parallel or serial data streams and decodes MPEG Layer 2 and 3 (including the low sampling frequency extensions) and MPEG 2 AAC. In addition, special downloadable software expands the function to a low-bitrate CELP codec for speech recording. Other download options (SDMI, other audio encoders/decoders) are available on request. Compressed speech data may be stored in an external memory via the parallel port.

2.2. Architecture of the MAS 35x9F

The hardware of the MAS 35x9F consists of a high-performance RISC Digital Signal Processor (DSP), and appropriate interfaces. A hardware overview of the IC is shown in Fig. 2–1.

2.3. DSP Core

The internal processor is a dedicated DSP for advanced audio applications.

2.3.1. RAM and Registers

The DSP core has access to two RAM banks denoted D0 and D1. All RAM addresses can be accessed in a 20-bit or a 16-bit mode via I²C bus. For fast access of internal DSP states the processor core has an address space of 256 data registers which can be accessed by I²C bus. For more details please refer to Section 3.3. on page 25.

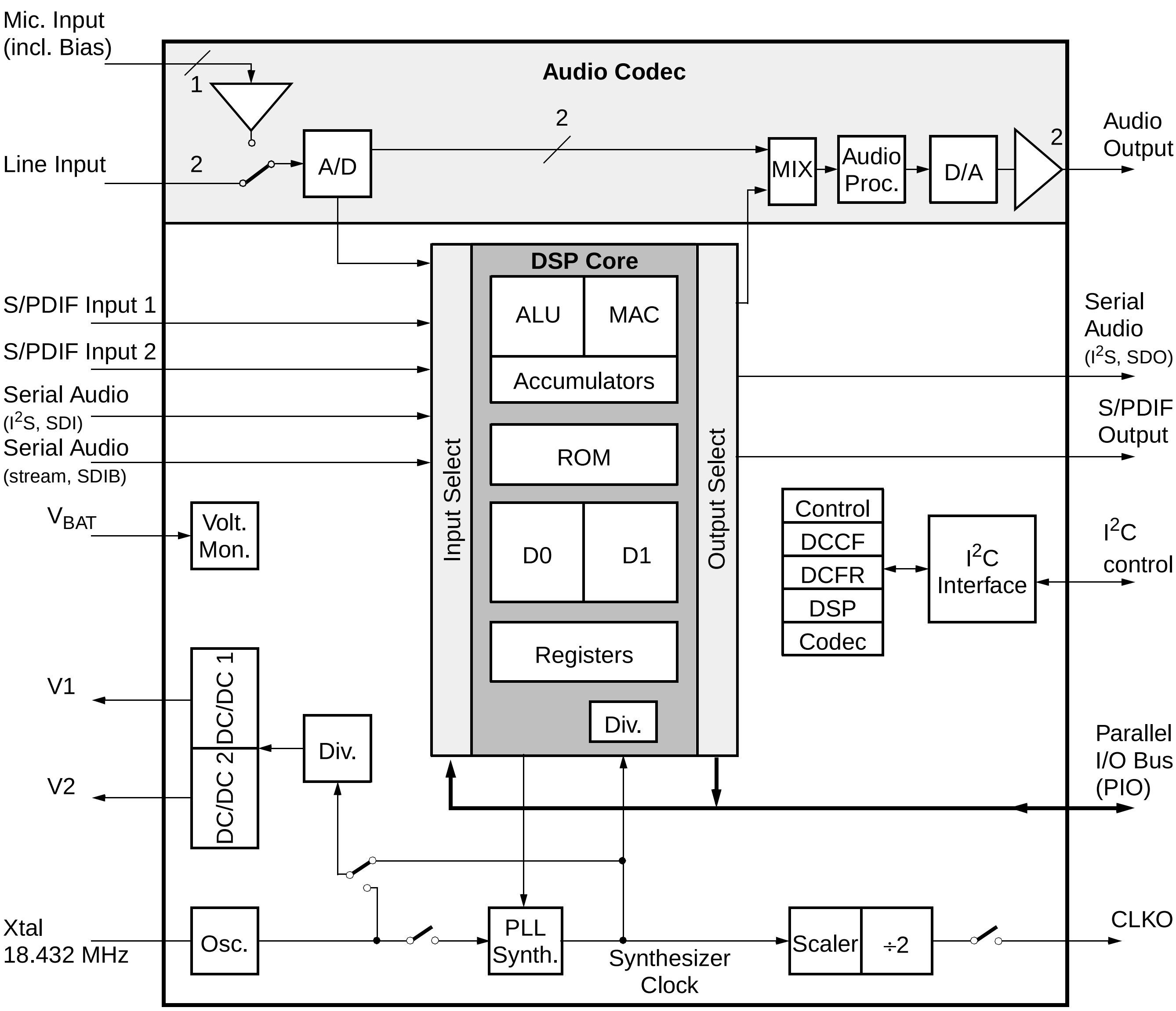


Fig. 2–1: The MAS 35x9F architecture

2.3.2. Firmware and Software

2.3.2.1. Internal Program ROM and Firmware, MPEG-Decoding

The firmware implemented in the program ROM of the MAS 35x9F provides MPEG 1/2 Layer 2, MPEG 1/2 Layer 3 and MPEG 2 AAC-decoding as well as a G.729 encoder and decoder.

The DSP operating system starts the firmware in the “Application Selection Mode”. By setting the appropriate bit in the Application Select memory cell (see Table 3–6 on page 31) the MPEG audio decoder or the G.729 Codec can be activated.

The MPEG decoder provides an automatic standard detection mode. If all MPEG audio decoders are selected, the Layer 2, Layer 3 or AAC bitstream is recognized and decoded automatically.

To add/remove MPEG layers while running in MPEG decoding mode (e.g. Layer 2, Layer 3 (0x0c) to Layer 2, Layer 3, AAC (0x1c)), the application selection has to be reset before writing the new value.

For general control purposes, the operation system provides a set of I^2C instructions that give access to internal DSP registers and memory areas.

An auxiliary digital volume control and mixer matrix is applied to the digital stereo audio data. This matrix is capable of performing the balance control and a simple kind of stereo basewidth enhancement. All four factors LL, LR, RL, and RR are adjustable, please refer to Fig. 3–3 on page 40.

2.3.2.2. Program Download Feature

The standard functions of the MAS 35x9F can be extended or substituted by downloading up to 4 kWords (1 Word = 20 bits) of program code and additionally up to 4 kWords of coefficients into the internal RAM .

The code must be downloaded by the *Fast Program Download* command (see Section 3.3.1.14. on page 29) into an area of RAM that is switchable from data memory to program memory. A *Run* command (see Section 3.3.1.1. on page 26) starts the operation.

2.4. Audio Codec

A sophisticated set of audio converters and sound features has been implemented to comply with various kinds of operating environments that range up to high-end equipment (see Fig. 2–2 on page 10).

2.4.1. A/D Converter and Microphone Amplifier

A pair of A/D converters is provided for recording or loop-through purposes. In addition, a microphone amplifier including voltage supply function for an electret type microphone has been integrated.

2.4.2. Baseband Processing

The several baseband functions are applied to the digital audio signal immediately before D/A conversion.

2.4.2.1. Bass, Treble, and Loudness

Standard baseband functions such as bass, treble, and loudness are provided.

2.4.2.2. Micronas Dynamic Bass (MDB)

The Micronas Dynamic Bass system (MDB) was developed to extend the frequency range of loudspeakers or headphones below the cutoff frequency of the speakers. In addition to dynamically amplifying the low frequency bass signals, the MDB exploits the psychoacoustic phenomenon of the ‘missing fundamental’. Adding harmonics of the frequency components below the cutoff frequency gives the impression of actually hearing the low frequency fundamental, while at the same time retaining the loudness of the original signal. Due to the parametric implementation of the MDB, it can be customized to create different bass effects and adapted to various loudspeaker characteristics.

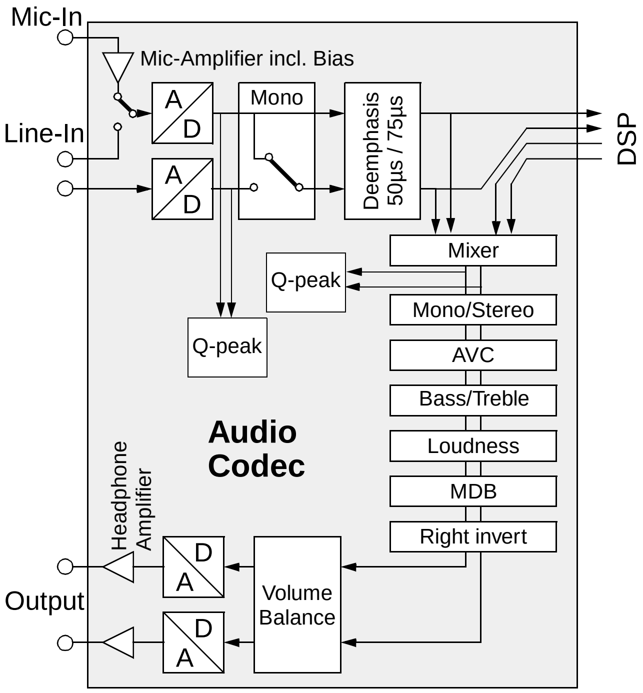


Fig. 2–2: Signal flow block diagram of Audio Codec

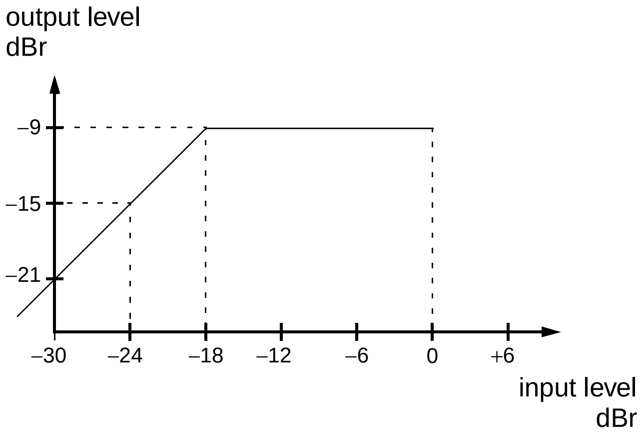


Fig. 2–3: Simplified AVC characteristics

2.4.2.3. Automatic Volume Control (AVC)

In a collection of tracks from different sources fairly often the average volume level varies. Especially in a noisy listening environment the user must adjust the volume to achieve a comfortable listening enjoyment. The Automatic Volume Correction (AVC) solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see Table 3–13 on page 42).

For input levels of -18 dBr to 0 dBr, the AVC maintains a fixed output level of -9 dBr. Fig. 2–3 shows the AVC output level versus its input level. For volume and baseband registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output.

2.4.2.4. Balance and volume

To minimize quantization noise, the main volume control is automatically split into a digital and an analog part. The volume range is –114...+12 dB with an additional mute position. A balance function is provided.

2.4.3. D/A Converters

A pair of Micronas' unique multibit sigma-delta D/A converters is used to convert the audio data with high linearity and a superior S/N. In order to attenuate high-frequency noise caused by noise-shaping, internal low-pass filters are included. They require additional external capacitors between pins FILTx and OUTx.

2.4.4. Output Amplifiers

The integrated output amplifiers are capable of directly driving stereo headphones or loudspeakers of 16...32 Ω impedance via 22-Ω series resistors. If more output power is required, the right output signal can be inverted and a single loudspeaker can be connected as a bridge between pins OUTL and OUTR. In this case for optimized power the source should be set to mono.

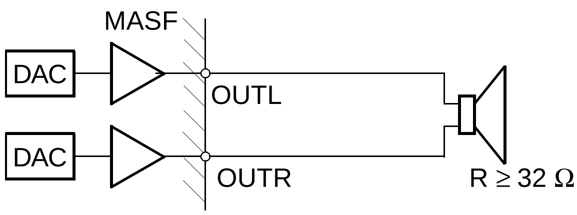


Fig. 2–4: Bridge operation mode

2.5. Clock Management

The MAS 35x9F is driven by a single crystal-controlled clock with a frequency of 18.432 MHz. It is possible to drive the MAS 35x9F with other reference clocks. In this case, the nominal crystal frequency must be written into memory location D0:348. The crystal clock acts as a reference for the embedded synthesizer that generates the internal clock.

For compressed audio data reception, the MAS 35x9F may act either as the clock master (Demand Mode) or as a slave (Broadcast Mode) as defined by bit 1 in IOControlMain memory cell (see Table 3–7 on page 32). In both modes, the output of the clock synthesizer depends on the sample rate of the decoded data stream as shown in Table 2–1.

In the BROADCAST MODE (PLL on), the incoming audio data controls the clock synthesizer via a PLL.

In the DEMAND MODE (PLL off) the MAS 35x9F acts as the system master clock. The data transfer is triggered by a demand signal at pin $\overline{\text{EOD}}$.

2.5.1. DSP Clock

The DSP clock has separate divider. For power conservation it is set to the lowest acceptable rate of the synthesizer clock which is capable to allow the processor core to perform all tasks.

2.5.2. Clock Output At CLKO

If the DSP or audio codec functions are enabled (bits 11 or 10 in the Control Register at I^2C subaddress $6a_{hex}$), the reference clock at pin CLKO is derived from the synthesizer clock.

Dependent on the sample rate of the decoded signal a scaler is applied which automatically divides the clockout by 1, 2, or 4, as shown in Table 2–1. An additional division by 2 may be selected by setting bit 17 of the OutClkConfig memory cell (see Table 3–7 on page 32). The scaler can be disabled by setting bit 8 of this cell.

The controlling at OutClkConfig is only possible as long as the DSP is operational (bit 10 of the Control Register). Settings remain valid if the DSP is disabled by clearing bit 10.

2.6. Power Supply Concept

The MAS 35x9F has been designed for minimal power dissipation. In order to optimize the battery management in portable players, two DC/DC converters have been implemented to supply the complete portable audio player with regulated voltages.

2.6.1. Power Supply Regions

The MAS 35x9F has five power supply regions.

The VDD/VSS pin pair supplies all digital parts including the DSP core, the XVDD/XVSS pin pair is connected to the digital signal pin output buffers, the AVDD0/AVSS0 supply is for the analog output amplifiers, AVDD1/AVSS1 for all other analog circuits like clock oscillator, PLL circuits, system clock synthesizer and A/D and D/A converters. The I^2C interface has an own supply region via pin I2CVDD. Connecting this to the microcontroller supply assures that the I^2C bus always works as long as the microcontroller is alive so that the operating modes can be selected.

Beside these regions, the DC/DC converters have start-up circuits of their own which get their power via pin VSENSx.

Table 2–1: Settings of bits 8 and 17 in OutClkConfig and resulting CLKO output frequencies

f_s/kHz	Output Frequency at CLKO/MHz				
	Synth. Clock bit 8=1	**Scaler On bit 8=0, bit 17=0**		**Scaler Plus Extra Division bit 8=0, bit 17=1**	
48	24.576	$512 \cdot f_s$	24.576	$256 \cdot f_s$	12.288
44.1	22.5792		22.5792		11.2896
32	24.576	$768 \cdot f_s$	24.576	$384 \cdot f_s$	12.288
24		$512 \cdot f_s$	12.288	$256 \cdot f_s$	6.144
22.05	22.5792		11.2896		5.6448
16	24.576	$768 \cdot f_s$	12.288	$384 \cdot f_s$	6.144
12		$512 \cdot f_s$	6.144	$256 \cdot f_s$	3.072
11.025	22.5792		5.6448		2.8224
8	24.576	$768 \cdot f_s$	6.144	$384 \cdot f_s$	3.072

2.6.2. DC/DC Converters

The MAS 35x9F has two embedded high-performance step-up DC/DC converters with synchronous rectifiers to supply both the DSP core itself and external circuitry such as a controller or flash memory at two different voltage levels. An overview is given in Fig. 2–9 on page 14.

The DC/DC converters are designed to generate an output voltage between 2.0 V and 3.5 V which can be programmed separately for each converter via the I^2C interface (see table 3.3). Both converters are of boot-strapped type allowing to start up from a voltage down to 0.9 V for use with a single battery or NiCd/NiMH cell. The default output voltages are 3.0 V. Both converters are enabled with a high level at pin DCEN and enabled/disabled by the I^2C interface.

The MAS 35x9F DC/DC converters feature a constant-frequency, low noise pulse width modulation (PWM) mode and a low quiescent current, pulse frequency modulation (PFM) mode for improved efficiencies at low current loads. Both modes – PWM or PFM – can be selected independently for each converter via I^2C interface. The default mode is PWM.

In PWM mode the switching frequency of the power-MOSFET-switches is derived from the crystal oscillator. Switching harmonics generated by constant frequency operation are consistent and predictable. When the audio codec is enabled the switching frequency of the converters is synchronised to the audio codec clock to avoid interferences into the audio band. The actual switching frequency can be selected via the I^2C-interface between 300 kHz and 580 kHz (for details see DCFR Register in Table 3–3 on page 21).

In PFM operation mode the switching frequency is controlled by the converters themself, it will be just high enough to service the output load thus resulting in the best possible efficiency at low current loads. PFM mode does not need a clock signal from the crystal oscillator. If both converters do not use the PWM-mode, the crystal clock will be shut down as long it is not needed from other internal blocks.

The synchronous rectifier bypasses the external Schottky diode to reduce losses caused by the diode forward voltage providing up to 5% efficiency improvement. By default, the P-channel synchronous rectifier switch is turned on when the voltage at pin(s) DCSOn exceeds the converter’s output voltage at pin(s) VSENSn and turns off when the inductor current drops below a threshold. If one or both converters are disabled, the corresponding P-channel switch will be turned on, connecting the battery voltage to the DC/DC converters output voltage at pin VSENSn. However, it is possible to individually disable both synchronous rectifier switches by setting the corresponding bits (bit 8 and 0 in DCCF-register).

If both DC/DC-converters are off, a high signal may be applied at pin DCEN. This will start the converters in their default mode (PWM with 3.0 V output voltage). The PUP signal will change from low to high when both converters have reached their nominal output voltage and will return to low when both converters output voltages have dropped 200 mV below their programmed output voltage. The signal at pin PUP can be used to control the reset of an external microcontroller (see Section 2.10.2. on page 16 for details on start up procedure).

If only DC/DC-converter 1 is used, the output of the unused converter 2 (VSENS2) must be connected to the output of converter 1 (VSENS1) to make the PUP signal work properly. Also, if a DC/DC-converter is not used (no inductor connected), the pin DCSO must be left vacant.

2.6.3. Power Supply Configurations

One of the following supply configurations may be used:

– Power-optimized solution (recommended operation). DC/DC 1 (e.g. 2.2 V) drives the MAS 35x9F DSP and the audio circuitry, DC/DC 2 (e.g. 2.7 V) supplies controller and flash (see Fig. 2–5 on page 13)
– Volume-optimized solution. DC/DC 1 (e.g. 2.7 V) supplies controller, flash and MAS 35x9F audio parts, DC/DC 2 generates e.g. 2.2 V for the MAS 35x9F DSP (see Fig. 2–6 on page 13).
– Minimized external components. DC/DC 1 operates on e.g. 2.7 V and feeds all components, DC/DC 2 remains off (see Fig. 2–7 on page 13).
– External power supply. All components are powered by an external source, no DC/DC converter is used (see Fig. 2–8 on page 13).

If DC/DC converter 1 is used, it must supply the analog circuits (pins AVDD0, AVDD1) of the MAS 35x9F.

If only one DC/DC converter is required, DC/DC1 must be used. Pin DCSO2 must be left vacant, pin VSENS2 should be connected to pin VSENS1.

If the DC/DC converters are not used, pin DCEN must be connected to VSS, DCSOx must be left vacant.

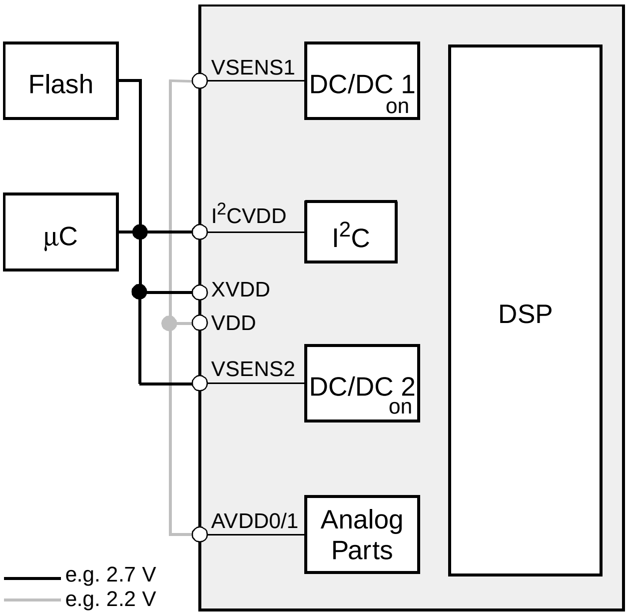


Fig. 2–5: Solution 1: Power-optimized

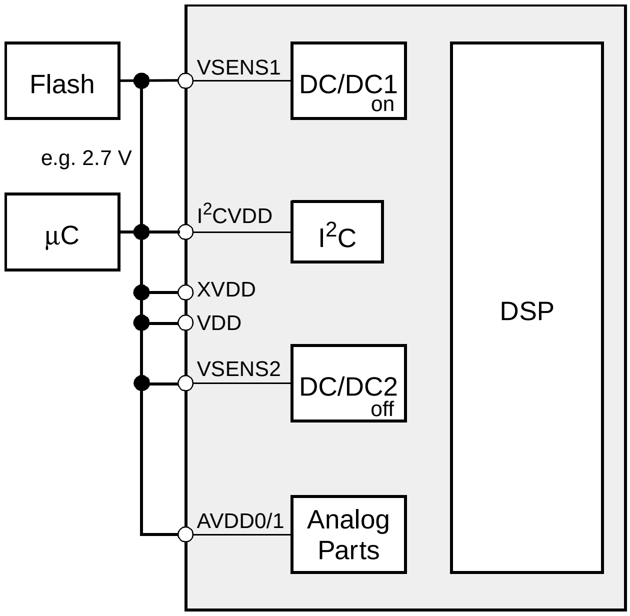


Fig. 2–7: Solution 3: Minimized components

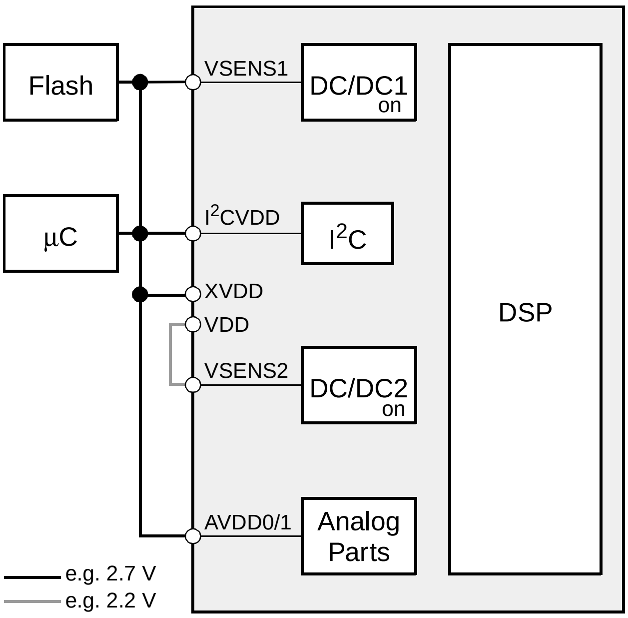


Fig. 2–6: Solution 2: Volume-optimized

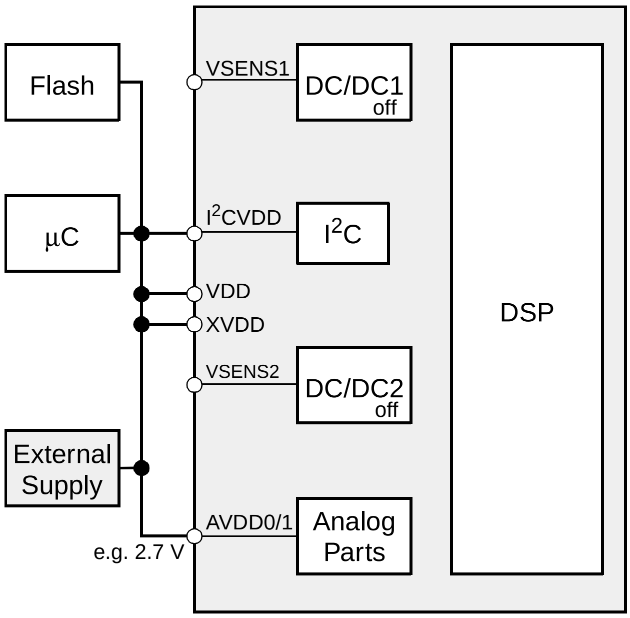


Fig. 2–8: Solution 4: External power supply

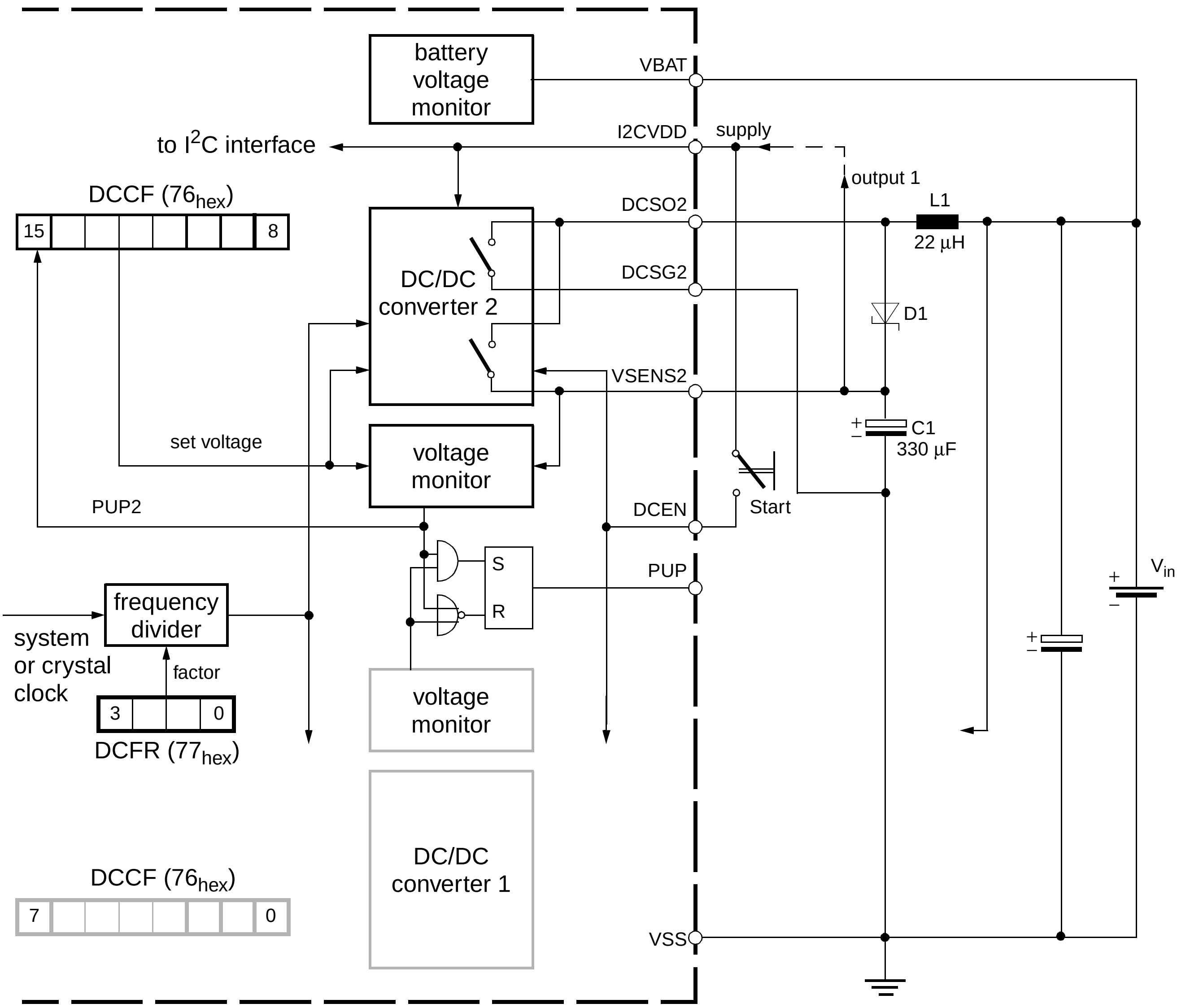


Fig. 2–9: DC/DC converter overview. The DCEN input must be connected to pin I2CVDD via the start-up push button.

2.7. Battery Voltage Supervision

A battery voltage supervision circuit (at pin VBAT) is provided which is independent of the DC/DC converters. It can be programmed to supervise one or two battery cells. The voltage is measured by subsequently setting a series of voltage thresholds and checking the respective comparison result in register 77_{hex}.

2.8. Interfaces

The MAS 35x9F uses an I^2C control interface, a serial input interface for MPEG bit streams, and a digital audio output interface for the decoded audio data (I^2S or similar). Alternatively, SPDIF input and output interfaces can be used. A parallel I/O interface (PIO) may be used for fast data exchange.

2.8.1. I^2C Control Interface

For controlling and program download purposes, a standard I^2C slave interface is implemented. A detailed description of all functions can be found in Section 3.

2.8.2. SPDIF Input Interface

The SPDIF interface receives a one-wire serial bus signal. In addition to the signal input pin SPDI1/SPDI2, a reference pin SPDIR is provided to support balanced signal sources or twisted pair transmission lines.

The synchronization time on the input signal is < 50 ms.

The SPDIF input signal can also be switched to the SPDO pin. In this case the analog input circuit of the SPDIF inputs (see Fig. 4–18 on page 59) restores the SPDIF input signal to a full swing signal at SPDO.

For controlling details please refer to Table 3–7 on page 32.

2.8.3. S/PDIF Output

In the next version of the IC the S/PDIF output of the baseband audio signals will be provided at pin SPDO.

2.8.4. Multiline Serial Audio Input (SDI, SDIB)

There are two multiline serial audio input interfaces (SDI, SDIB) each consisting of the three pins SI(B)C, SI(B)I, and SI(B)D. The standard firmware only supports SDIB for bitstream signals.

The interfaces can be configured as continuous bit stream or word-oriented inputs. For the MPEG bitstreams the word strobe pin SIBI must always be connected to V_{SS}, bits must be sent MSB first as created by the encoder.

If the optional downloadable software uses the inputs for PCM data, the interface acts as a I^2S-type with SI(B)I as a word strobe.

In case of the Demand Mode (see Section 2.5.), the signal clock coming from the data source must be higher than the nominal data transmission rate (e.g. 128 kbit/s). Pin $\overline{EOD}$ is used to interrupt the data flow whenever the input buffer of the MAS 35x9F is filled.

For controlling details please refer to Table 3–7 on page 32.

2.8.5. Multiline Serial Output (SDO)

The serial audio output interface of the MAS 35x9F is a standard I^2S-like interface consisting of the data lines SOD, the word strobe SOI and the clock signal SOC. It is possible to choose between two standard interface configurations (16-bit data words with word strobe time offset or 32-bit data words with inverted SOI-signal).

If the serial output generates 32 bits per audio sample, only the first 20 bits will carry valid audio data. The 12 trailing bits are set to zero by default.

2.8.6. Parallel Input/Output Interface (PIO)

The parallel interface of the MAS 35x9F consists of the 8 data lines PI12...PI19 (MSB) and the control lines $\overline{PCS}$, PR, $\overline{PRTR}$, $\overline{PRTW}$, and $\overline{EOD}$. It can be used for data exchange with an external memory, for fast program download and for other special purposes as defined by the DSP software.

For MPEG-data input, the PIO interface is activated by setting bits 9,8 in D0:346 to 01. For the handshake protocol please refer to Section 4.6.3.6. on page 72

2.9. MPEG Synchronization Output

The signal at pin SYNC is set to '1' after the internal decoding for the MPEG header has been finished for one frame. The rising edge of this signal can be used as an interrupt input for the controller that triggers the read out of the control information and ancillary data. As soon as the MAS 35x9F has received the SYNC reset command (see Section 3.3.1.12. on page 28), the SYNC signal is cleared. If the controller does not issue a reset command, the SYNC signal returns to '0' as soon as the decoding of the next MPEG frame is started. MPEG status and ancillary data become invalid until the frame is completely decoded and the signal at pin SYNC rises again. The controller must have finished reading all MPEG information before it becomes invalid. The MPEG Layer 2/3 frame lengths are given in Table 2–2. AAC has no fixed frame length.

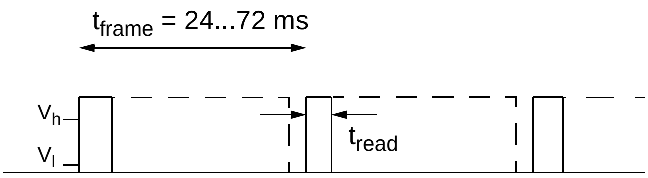


Fig. 2–10: Schematic timing of the signal at pin SYNC. The signal is cleared at t_{read} when the controller has issued a Clear SYNC Signal command (see Section 3.3.1.12. on page 28). If no command is issued, the signal returns to '0' just before the decoding of the next MPEG frame.

Table 2–2: Frame length in MPEG Layer 2/3

f_s/kHz	Frame Length Layer 2	Frame Length Layer 3
48	24 ms	24 ms
44.1	26.12 ms	26.12 ms
32	36 ms	36 ms
24	24 ms	24 ms
22.05	26.12 ms	26.12 ms
16	36 ms	36 ms
12	not available	48 ms
11.025	not available	52.24 ms
8	not available	72 ms

2.10. Default Operation

This sections refers to the standard operation mode "power-optimized solution" (see Section 2.6.3.).

2.10.1. Stand-by Functions

After applying the battery voltage, the system will remain stand-by, as long as the DCEN pin level is kept low. Due to the low stand-by current of CMOS circuits, the battery may remain connected to DCSOn/VSENSn at all times.

2.10.2. Power-Up of the DC/DC Converters and Reset

The battery voltage must be applied to pin DCSOn via the 22-µH inductor and, furthermore, to the sense pin VSENSn via a Schottky diode (see Fig. 2–9 on page 14).

For start-up, the pin DCEN must be connected via an external "start" push button to the I2CVDD supply, which is equivalent to the battery supply voltage (> 0.9 V) at start-up.

The supply at DCEN must be applied until the DC/DC converters have started up (signal at pin PUP) and then removed for normal operation.

As soon as the output voltage at VSENSn reaches the default voltage monitor reset level of 3.0 V, the respective internal PUPn bit will be set. When both PUPn bits are set, the signal at pin PUP will go high and can be used to start and reset the microcontroller.

Before transmitting any I^2C commands, the controller must issue a power-on reset to pin $\overline{POR}$. The separate supply pin I2CVDD assures that the I^2C interface works independently of the DSP or the audio codec. Now the desired supply voltage can be programmed at I^2C subaddress 76_{hex}.

The signal at pin PUP will return to low only when both PUPn flags (I^2C subaddress 76_{hex}) have returned to zero. Care must be taken when changing both DC/DC output voltages to higher values. In this case, both output voltages are momentarily insufficient to keep the PUPn flags up; the resulting dip in the signal at the PUP pin may in turn reset the microcontroller. To avoid this condition, only one DC/DC output voltage should be changed at a time. Before modifying the second voltage, the microcontroller must wait for the PUPn flag of the first voltage to be set again.

The operating mode (pulse width modulation or pulse frequency modulation, synchronized rectifier for higher efficiency) are controlled at I^2C subaddress 76_{hex}, the operating frequency at I^2C subaddress 77_{hex}.

2.10.3. Control of the Signal Processing

Before starting the DSP, the controller should check for a sufficient voltage supply (respective flag PUPn at I^2C subaddress 76_{hex}). The DSP is enabled by setting the appropriate bit in the Control register (I^2C subaddress $6a_{hex}$). The nominal frequency of the crystal oscillator must be written into D0:348. After an initialization phase of 5 ms, the DSP data registers can be accessed via I^2C.

Input and output control is performed via memory location D0:346 and D0:347. The serial input interface SDIB is the default. The decoded audio can be routed to either the SPDIF, the SDO and the analog outputs. The output clock signal at pin CLKO is defined in D0:349.

All changes in the D0-memory cells become effective synchronously upon setting the LSB of Main I/O Control (see Table 3–7 on page 32). Therefore, this cell should always be written at last.

The digital volume control (see Table 3–7 on page 32) is applied to the output signal of the DSP. The decoded audio data will be available at the SPDO output interface in the next version.

The DSP does not have to be started if its functions are not needed, e.g. for routing audio via the A/D and the D/A converters through the codec part of the IC.

2.10.4. Start-up of the Audio Codec

Before enabling the audio codec, the controller should check for a sufficient voltage supply (respective flag PUPn at I^2C subaddress 76_{hex}).

The audio codec is enabled by setting the appropriate bit at the Control register (I^2C subaddress $6a_{hex}$). After an initialization phase of 5 ms, the DSP data registers can be accessed via I^2C.The A/D and the D/A converters must be switched on explicitly (00 00_{hex} at I^2C subaddress $6c_{hex}$). The D/A converters may either accept data from the A/D converters or the output of the DSP, or a mix of both[1)] (register 00 06_{hex} and 00 07_{hex} at I^2C subaddress $6c_{hex}$). Finally, an appropriate output volume (00 10_{hex} at I^2C subaddress $6c_{hex}$) must be selected.

[1)] mixer available in version A2 and later; in version A1 please use selector 00 $0f_{hex}$.

2.10.5. Power-Down

All analog outputs should be muted and the A/D and the D/A converters must be switched off (register 00 10_{hex} and 00 00_{hex} at I^2C subaddress $6c_{hex}$). The DSP and the audio codec must be disabled (clear DSP_EN and CODEC_EN bits in the Control register, I^2C subaddress $6a_{hex}$). By clearing both DC/DC enable flags in the Control register (I^2C subaddress $6a_{hex}$), the microcontroller can power down the complete system.

3. I²C Interface

3.1. General

3.1.1. Device Address

Controlling the MAS 35x9F is done via an I²C slave interface. The device addresses are 3C/3E$_{hex}$ (device write) and 3D/3F$_{hex}$ (device read) as shown in Table 3–1. The device address pair 3C/3D$_{hex}$ applies if the DVS pin is connected to VSS, the device address pair 3E/3F$_{hex}$ applies if the DVS pin is connected to VDD.

Table 3–1: I²C device address

A7	A6	A5	A4	A3	A2	A1	W/R
0	0	1	1	1	1	DVS	0/1

I²C clock synchronization is used to slow down the interface if required.

3.1.2. I²C Registers and Subaddresses

The interface uses one level of subaddresses. The MAS 35x9F interface has 7 subaddresses allocated for the corresponding I²C registers. The registers can be divided into three categories as shown in Table 3–2.

The address 6A$_{hex}$ is used for basic control, i.e. reset and task select. The other addresses are used for data transfer from/to the MAS 35x9F.

The I²C registers of the MAS 35x9F are 16 bits wide, the MSB is denoted as bit[15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, MSB sent first); thus, for each register access, two 8-bit data words must be sent/received via I²C bus.

Table 3–2: I²C subaddresses

Sub-address (hex)	I²C-Register Name	Function
Direct Configuration		
6A	CON-TROL	Controller writes to MAS 35x9F control register
76	DCCF	Controller writes to first DC/DC configuration register
77	DCFR	Controller writes to second DC/DC config reg.
DSP Core Access		
68	DATA (WRITE)	Controller writes to MAS 35x9F DSP
69	DATA (READ)	Controller reads from MAS 35x9F DSP
Codec Access		
6C	CODEC (WRITE)	Controller writes to MAS 35x9F codec register
6D	CODEC (READ)	Controller reads from MAS 35x9F codec register

3.1.3. Naming Convention

The description of the various controller commands uses the following formalism:

– **Abbreviations** used in the following descriptions:
  a address
  d data value
  n count value
  o offset value
  r register number
  x don’t care

– A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.

– Data values in nibbles are always shown in hexadecimal notation.

– A hexadecimal 20-bit number **d** is written, e.g. as **d** = $17C63_{hex}$, its five nibbles are d0 = 3_{hex}, d1 = 6_{hex}, d2 = C_{hex}, d3 = 7_{hex}, and d4 = 1_{hex}.

– **Variables** used in the following descriptions:
  I²C address:
  DW 3C/$3E_{hex}$
  DR 3D/$3F_{hex}$
  DSP core:
  data_write 68_{hex}
  data_read 69_{hex}
  Codec:
  codec_write $6C_{hex}$
  codec_read $6D_{hex}$

– **Bus signals**
  S Start
  P Stop
  A ACK = Acknowledge
  N NAK = Not acknowledge

– **Symbols** in the telegram examples
  < Start Condition
  > Stop
  dd data bytes
  xx ignore
  All telegram numbers are hexadecimal, data originating from the MAS 35x9F are greyed.
  Example:
  `<DW 68 dd dd>` write data to DSP
  `<DW 69 <DR dd dd>` read data from DSP and stop with NAK

Fig. 3–1 shows I²C bus protocols for write and read operations of the interface; the read operations require an extra start condition and repetition of the chip address with the device read command (DR). Fields with signals/data originating from the MAS 35x9F are marked by a gray background. Note that in some cases the data reading process must be concluded by a NAK condition.

Example: I²C write access

S	DW	A	subaddress	A	high data word	A	low data word	A	P

Example: I²C read access

S	DW	A	subaddress	A	S	DR	A	high data word	A	
								low data word	N	P

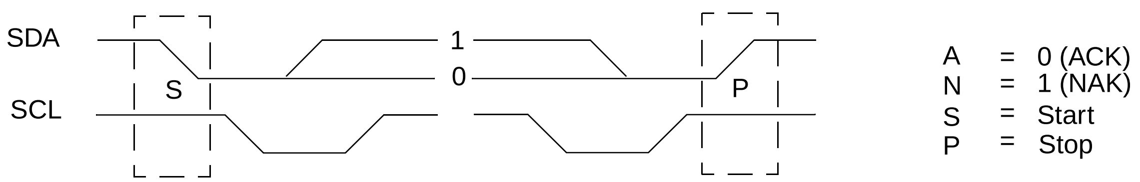


Fig. 3–1: Example of an I²C bus protocol for the MAS 35x9F (MSB first; data must be stable while clock is high)

3.2. Direct Configuration Registers

The task selection of the DSP and the DC/DC converters are controlled in the direct configuration registers Control, DCCF, and DCFR.

3.2.1. Write Direct Configuration Registers

S	DW	A	subaddress	A	d3,d2	A	d1,d0	A	P

The write protocol for the direct configuration registers only consists of device address, subaddress and one 16-bit data word.

3.2.2. Read Direct Configuration Register

1) send subaddress

S	DW	A	subaddress	A	P

2) get register value

S	DW	A	subaddress	A	S	DR	A

d3,d2	A	d1,d0	N	P

To check the PUP1 and PUP2 power-up flags, it is necessary to read back the content of the direct configuration registers.

Table 3–3: Direct Configuration Registers

<table>
<tr><th>I²C Sub-address (hex)</th><th>Function</th><th>Name</th></tr>
<tr><td>6A</td><td>Control Register (reset value = 3000_{hex})

bit[15:14] Analog Supply Voltage Range

Code AGNDC recommended for voltage range of AVDD
00 1.1 V 2.0 ... 2.4 V (reset)
01 1.3 V 2.4 ... 3.0 V
10 1.6 V 3.0 ... 3.6 V
11 reserved reserved

Higher voltage ranges permit higher output levels and thus a better signal-to-noise ratio.

bit[13] enable DC/DC 2 (reset=1)
bit[12] enable DC/DC 1 (reset=1)

Both DC/DC converters are switched on by default.

bit[11] enable and reset audio codec
bit[10] enable and reset DSP core

For normal operation (MPEG-decoding and D/A conversion), both, the DSP core and the audio codec have to be enabled after the power-up procedure. The DSP can be left off if an audio signal is routed from the analog inputs to the analog outputs (set bit[15] in codec register 00 $0F_{hex}$). The audio codec can be left off if the DSP uses digital inputs and outputs only.

bit[9] reset codec
bit[8] reset DSP core

bit[7] disable task 7 of DSP core
bit[6] disable task 6 of DSP core
bit[5] disable task 5 of DSP core
bit[4] disable task 4 of DSP core

bit[3] set task 3 of DSP core
bit[2] set task 2 of DSP core
bit[1] set task 1 of DSP core
bit[0] set task 0 of DSP core

bit[7] [1)] enable XTAL input clock divider (extended crystal range up to 28 MHz)
bit[6:0] [1)] reserved, must be set to zero</td><td>CONTROL</td></tr>
<tr><td>6B [1)]</td><td>bit[15:8] reserved, must be set to zero

bit[7] disable task 7 of DSP core
bit[6] disable task 6 of DSP core
bit[5] disable task 5 of DSP core
bit[4] disable task 4 of DSP core

bit[3] set task 3 of DSP core
bit[2] set task 2 of DSP core
bit[1] set task 1 of DSP core
bit[0] set task 0 of DSP core

Unless downloaded optional software is used, the bits 7...0 must be set to zero.</td><td>DSP_TASK</td></tr>
<tr><td colspan="3">[1)] available in the next version</td></tr>
</table>

Table 3–3: Direct Configuration Registers

<table>
<tr><th>I²C Sub-address (hex)</th><th>Function</th><th>Name</th></tr>
<tr><td>76</td><td>DCCF Register (reset = 5050_{hex})</td><td>DCCF</td></tr>
<tr><td></td><td>
DC/DC Converter 2
bit[15] PUP2: Voltage monitor 2 flag (readback)
bit[14:11] Voltage between VSENS2 and DCSG2
<table>
<tr><th>Code</th><th>Nominal output volt.</th><th>set level of PUP2</th><th>reset level of PUP2</th></tr>
<tr><td>1111</td><td>3.5 V</td><td>3.4 V</td><td>3.3 V</td></tr>
<tr><td>1110</td><td>3.4 V</td><td>3.3 V</td><td>3.2 V</td></tr>
<tr><td>1101</td><td>3.3 V</td><td>3.2 V</td><td>3.1 V</td></tr>
<tr><td>1100</td><td>3.2 V</td><td>3.1 V</td><td>3.0 V</td></tr>
<tr><td>1011</td><td>3.1 V</td><td>3.0 V</td><td>2.9 V</td></tr>
<tr><td>1010</td><td>3.0 V</td><td>2.9 V</td><td>2.8 V (reset)</td></tr>
<tr><td>1001</td><td>2.9 V</td><td>2.8 V</td><td>2.7 V</td></tr>
<tr><td>1000</td><td>2.8 V</td><td>2.7 V</td><td>2.6 V</td></tr>
<tr><td>0111</td><td>2.7 V</td><td>2.6 V</td><td>2.5 V</td></tr>
<tr><td>0110</td><td>2.6 V</td><td>2.5 V</td><td>2.4 V</td></tr>
<tr><td>0101</td><td>2.5 V</td><td>2.4 V</td><td>2.3 V</td></tr>
<tr><td>0100</td><td>2.4 V</td><td>2.3 V</td><td>2.2 V</td></tr>
<tr><td>0011</td><td>2.3 V</td><td>2.2 V</td><td>2.1 V</td></tr>
<tr><td>0010</td><td>2.2 V</td><td>2.1 V</td><td>2.0 V</td></tr>
<tr><td>0001[1)]</td><td>2.1 V</td><td>2.0 V</td><td>1.9 V</td></tr>
<tr><td>0000[1)]</td><td>2.0 V</td><td>1.9 V</td><td>1.8 V</td></tr>
</table>
bit[10] Mode
1 Pulse frequency modulation (PFM)
0 Pulse width modulation (PWM) (reset)
bit[9] reserved, must be set to zero
bit[8] Disable synchronized rectifier
1 disable synchronized recitifier
0 enable synchronized recitifier (reset)
The DC/DC converters are up-converters only. Thus, if the battery voltage is higher than the selected nominal voltage, the output voltage will exceed the nominal voltage.
1) refer to Section 4.6.2. on page 61
</td><td></td></tr>
</table>

Table 3–3: Direct Configuration Registers

I^2C Sub-address (hex)	Function	Name
76 (continued)	**DC/DC Converter 1** bit[7] PUP1: Voltage monitor 1 flag (readback) bit[6:3] Voltage between VSENS1 and DCSG1 (see table above) bit[2] Mode 1 Pulse frequency modulation (PFM) 0 Pulse width modulation (PWM) (reset) bit[1] reserved, must be set to zero bit[0] Disable synchronized rectifier 1 disable synchronized recitifier 0 enable synchronized recitifier (reset) Note, that the reference voltage for DC/DC converter 1 is derived from the main reference source supplied via pin AVDD1. Therefore, if this DC/DC converter is used, its output must be connected to the analog supply. The DC/DC converters are up-converters only. Thus, if the battery voltage is higher than the selected nominal voltage, the output voltage will exceed the nominal voltage.	

Table 3–3: Direct Configuration Registers

I^2C Sub-address (hex)	Function	Name
77	**DCFR Register** (reset = 00_{hex})	DCFR

Battery Voltage Monitor

bit[15]		Comparison result (readback)
	1	input voltage at pin VBAT above defined threshold
	0	input voltage at pin VBAT below defined threshold
bit[14]		Number of battery cells
	0	1 cell (range 0.8...1.5 V) (reset)
	1	2 cells (range 1.6...3.0 V)

bit[13:10] Voltage threshold level

	1 cell	2 cells
1111	1.5	3.0 V
1110	1.45	2.9 V
...		
0010	0.85	1.7 V
0001	0.8	1.6 V
0000	Battery voltage supervision off (reset)	

bit[9:8] Reserved, must be set to 0

The result is stable after 1 ms after enabling. The setup time for switching between two thresholds is negligibly small.

For power management reasons, the battery voltage monitor should be switched off by setting bit[13:10] to zero when the measurement is completed.

DC/DC Converter Frequency Control (PWM)

bit[7:4] Reserved, must be set to 0

bit[3:0] Frequency of DC/DC converter

Reference:	24.576	22.5792	18.432 MHz
0111	315.1	289.5	297.3 kHz
0110	323.4	297.1	307.2 kHz
0101	332.1	305.1	317.8 kHz
0100	341.3	313.6	329.1 kHz
0011	351.1	322.6	341.3 kHz
0010	361.4	332.0	354.5 kHz
0001	372.4	342.1	368.6 kHz
0000	384.0	352.8	384.0 kHz (reset)
1111	396.4	364.2	400.7 kHz
1110	409.6	376.3	418.9 kHz
1101	423.7	389.3	438.9 kHz
1100	438.9	403.2	460.8 kHz
1011	455.1	418.1	485.1 kHz
1010	472.6	434.2	512.0 kHz
1001	491.5	451.6	542.1 kHz
1000	512.0	470.4	576.0 kHz

If the audio codec is not enabled (bit 11 of the Control register at I^2C-subaddress $6A_{hex}$ is zero), the clock for the DC/DC converters is directly derived from the crystal frequency (nominal 18.432 MHz). Otherwise, the synthesizer clock is used as the reference (please refer to the respective column in Table 2–1 on page 11).

3.3. DSP Core

The DSP Core of the MAS 35x9F has two RAM banks denoted D0 and D1. The word size is 20 bits. All RAM addresses can be accessed in a 20-bit or a 16-bit mode via I^2C bus. For fast access of internal DSP states, the processor core also has an address space of 256 data registers. All register and RAM addresses are given in hexadecimal notation.

3.3.1. Access Protocol

The access of the DSP Core in the MAS 35x9F uses a special command syntax. The commands are executed by the DSP during its normal operation without any loss or interruption of the incoming data or outgoing audio data stream. These I^2C commands allow the controller accessing the internal DSP registers and RAM cells and thus, monitoring internal states and setting the parameters for the DSP firmware. This access also provides a download option for alternative software modules.

The MAS 35x9F firmware scans the I^2C interface periodically and checks for pending or new commands. However, due to some time critical firmware parts, a certain latency time for the response has to be expected. The theoretical worst case response time does not exceed 4 ms. However, the typical response time is less than 0.5 ms.

Table 3–4 gives an overview over the different commands which the DSP Core receives via the I^2C data register. The “Code” is always the first data nibble transmitted after the “data_write” subaddress byte. A second auxiliary code nibble is used for the short memory (16-bit) access commands.

Due to the 16-bit width of the I^2C data register, all actions transmit telegrams with multiples of 16 data bits.

S	DW	A	data_write	A	Code, ...	A	..., ...	A	...

Fig. 3–2: General core access protocol

Table 3–4: Basic controller command codes

Code (hex)	Command	Function
0...3	Run	Start execution of an internal program. *Run* with start address 0 means freeze the operating system.
5	Read Ancillary Data	The controller reads a block of MPEG Ancillary Data from the MAS 35x9F
6	Fast Program Download	The controller downloads custom software via the PIO interface
A	Read from Register	The controller reads an internal register of the MAS 35x9F
B	Write to Register	The controller writes an internal register of the MAS 35x9F
C	Read D0 Memory	The controller reads a block of the DSP memory
D	Read D1 Memory	The controller reads a block of the DSP memory
E	Write D0 Memory	The controller writes a block of the DSP memory
F	Write D1 Memory	The controller writes a block of the DSP memory

3.3.1.1. Run and Freeze

S	DW	A	data_write	A	**a3**,a2	A	a1,a0	A	P

The *Run* command causes the start of a program part at address **a** = (a3,a2,a1,a0). Since nibble a3 is also the command code (see Table 3–4), it is restricted to values between 0 and 3.

If the start address is $1000_{hex} \le \mathbf{a} < 3FFF_{hex}$ and the respective RAM area has been configured as program RAM (see Table 3–5 on page 29), the MAS 35x9F continues execution with a custom program already downloaded to this area.

Example 1: Start program execution at address 345_{hex}:

```
<DW 68 03 45>
```

Example 2: Start execution of a downloaded code at address 3000_{hex}:

```
<DW 68 30 00>
```

Freeze is a special run command with start address 0. It suspends all normal program execution. The operating system will enter an idle loop so that all registers and memory cells can be watched. This state is useful for operations like downloading code or contents of memory cells because the internal program cannot overwrite these values. This freezing will be required if alternative software is downloaded into the internal RAM of the MAS 35x9F.

Freeze has the following I^2C protocol:

```
<DW 68 00 00>
```

3.3.1.2. Read Register (Code A_{hex})

1) send command

S	DW	A	data_write	A	**a**,r1	A	r0,0	A	P

2) get register value

S	DW	A	data_write	A	S	DR	A				
			x,x	A	x,d4	A	d3,d2	A	d1,d0	N	P

Some registers (**r** = r1,r0 in the figure above) are direct control inputs for various hardware blocks, others control the internal program flow. In contrast to memory cells, registers cannot be accessed as a block but must always be addressed individually.

Example:
Read the content of the PIO data register ($C8_{hex}$):

```
<DW 68 ac 80>                define register
<DW 69 <DR xx xd dd dd>      and read
```

3.3.1.3. Write Register (Code B_{hex})

S	DW	A	data_write	A	**b**,r1	A	r0,d4	A	
					d3,d2	A	d1,d0	A	P

The controller writes the 20-bit value (**d** = d4,d3,d2, d1,d0) into the MAS 35x9F register (**r** = r1,r0).

Example: Writing the value 81234_{hex} into the register with the number AA_{hex}:

```
<DW 68 ba a8 12 34>
```

In Table 3–5 on page 29 the registers of interest with respect to the firmware are described in detail.

3.3.1.4. Read D0 Memory (Code C_{hex})

The MAS 35x9F has 2 memory areas of 2048 words called D0 and D1 memory. Both memory areas have different read and write commands. All D0/D1 memory addresses are given in hexadecimal notation.

1) send command

S	DW	A	data_write	A	**c**,0	A	0,0	A	
					n3,n2	A	n1,n0	A	
					a3,a2	A	a1,a0	A	P

2) get memory value

S	DW	A	data_read	A	S	DR	A				
		x,x	A	x,d4	A	d3,d2	A	d1,d0	A		

... repeat for n data values ...

x,x	A	x,d4	A	d3,d2	A	d1,d0	N	P

The *Read D0 Memory* command gives the controller access to all 20 bits of D0 memory cells of the MAS 35x9F. The telegram to read 3 words starting at location D0:100 is

```
<DW 68 c0 00 00 03 01 00>
<DW 69 <DR xx xd dd dd
           xx xd dd dd xx xd dd dd>
```

3.3.1.5. Short Read D0 Memory (Code $C4_{hex}$)

Because most cells in the user interface are only 16 bits wide, it is faster and more convenient to access the memory locations with a special 16 bit mode for reading:

1) send command

S	DW	A	data_write	A	**c,4**	A	0,0	A	
					n3,n2	A	n1,n0	A	
					a3,a2	A	a1,a0	A	P

2) get memory value

S	DW	A	data_read	A	S	DR	A

d3,d2	A	d1,d0	A

... repeat for n data values ...

d3,d2	A	d1,d0	N	P

This command is similar to the normal 20 bit read command and uses the same command code C_{hex}, however it is followed by a 4_{hex} rather than a 0_{hex}.

3.3.1.6. Read D1 Memory (Code D_{hex})

1) send command

S	DW	A	data_write	A	**d**,0	A	0,0	A	
					n3,n2	A	n1,n0	A	
					a3,a2	A	a1,a0	A	P

2) get memory value

S	DW	A	data_read	A	S	DR	A

x,x	A	x,d4	A	d3,d2	A	d1,d0	A

... repeat for n data values ...

x,x	A	x,d4	A	d3,d2	A	d1,d0	N	P

The *Read D1 Memory* command is provided to get information from D1 memory cells of the MAS 35x9F.

3.3.1.7. Short Read D1 Memory (Code $D4_{hex}$)

1) send command

S	DW	A	data_write	A	**d,4**	A	0,0	A	
					n3,n2	A	n1,n0	A	
					a3,a2	A	a1,a0	A	P

2) get memory value

S	DW	A	data_read	A	S	DR	A

d3,d2	A	d1,d0	A

... repeat for n data values ...

d3,d2	A	d1,d0	N	P

The *Short Read D1 Memory* command works similar to the *Read D1 Memory* command but with the code D_{hex} followed by a 4_{hex}.

Example: Read 16 bits of D1:123 has the following I^2C protocol:

```
<DW 68 d4 00            read 16 bits from D1
   00 01                1 word to be read
   01 23                start address
   <DW 69 DR dd dd>     start reading
```

3.3.1.8. Write D0 Memory (Code E_{hex})

S	DW	A	data_write	A	**e**,0	A	0,0	A
					n3,n2	A	n1,n0	A
					a3,a2	A	a1,a0	A
					0,0	A	0,d4	A
					d3,d2	A	d1,d0	A

... repeat for n data values ...

0,0	A	0,d4	A	
d3,d2	A	d1,d0	A	P

With the *Write D0 Memory* command n 20-bit memory cells in D0 can be initialized with new data.

Example: Write 80234_{hex} to D0:456 has the following I^2C protocol:

```
<DW 68 e0 00            write D1 memory
     00 01              1 word to write
     04 56              start address
     00 08              value = 80234hex
     02 34>
```

3.3.1.9. Short Write D0 Memory (Code E4$_{hex}$)

S	DW	A	data_write	A	**e**,**4**	A	0,0	A	
					n3,n2	A	n1,n0	A	
					a3,a2	A	a1,a0	A	
					d3,d2	A	d1,d0	A	
					... repeat for n data values ...				
					d3,d2	A	d1,d0	A	P

For faster access only the lower 16 bits of each memory cell are accessed. The 4 MSBs of the cell are cleared.

3.3.1.10. Write D1 Memory (Code F$_{hex}$)

S	DW	A	data_write	A	**f**,0	A	0,0	A	
					n3,n2	A	n1,n0	A	
					a3,a2	A	a1,a0	A	
					0,0	A	0,d4	A	
					d3,d2	A	d1,d0	A	
					... repeat for n data values ...				
					0,0	A	0,d4	A	
					n3,n2	A	d1,d0	A	P

For further details, see the *Write D0 Memory* command.

3.3.1.11. Short Write D1 Memory (Code F4$_{hex}$)

S	DW	A	data_write	A	**f**,**4**	A	0,0	A	
					n3,n2	A	n1,n0	A	
					a3,a2	A	a1,a0	A	
					d3,d2	A	d1,d0	A	
					... repeat for n data values ...				
					d3,d2	A	d1,d0	A	P

Only the 16 lower bits of each memory cell are written, the upper 4 bits are cleared.

3.3.1.12. Clear SYNC Signal (Code 5$_{hex}$)

S	DW	A	data_write	A	**5**,0	A	0,0	A	P

After the successful decoding of an MPEG frame the signal at pin SYNC rises and thus generates an interrupt event for the microcontroller. Issuing this command lets the signal at pin SYNC return to ’0’.

3.3.1.13. Default Read

The *Default Read* command is the fastest way to get information from the MAS 35x9F. Executing the *Default Read* in a polling loop can be used to detect a special state during decoding.

S	DW	A	data_read	A	S	DR		A		
						d3,d2	A	d1,d0	N	P

The *Default Read* command immediately returns the lower 16 bit content of a specific RAM location as defined by the pointer D0:ffb. The pointer must be loaded before the first *Default Read* action occurs. If the MSB of the pointer is set, the pointer refers to a memory location in D1 rather than to one in D0.

Example: For watching D1:123 the pointer D0:ffb must be loaded with 8123$_{hex}$:

```
<DW 68 e0 00          write to D0 memory
    00 01             1 word to write
    0f fb             start address ffb
    00 08             value = 8...
    01 23>                 ...0123hex
```

Now *Default Read* commands can be issued as often as desired:

```
<DW 69 <DR            Default Read command
           dd dd>     16 bit content of the
                      address as defined by the
                      pointer
<DW 69 <DR dd dd>     ... and do it again
```

3.3.1.14. Fast Program Download

S	DW	A	data_read	A	**6**,n2	A	n1,n0	A	
					a3,a2	A	a1,a0	A	P

The *Fast Program Download* command introduces a data transfer via the parallel port. **n** = n2,n1,n0 denotes the number of 20-bit data words to be transferred, a = a3,a2,a1,a0 gives the start address. The data at the PIO port must be padded with three 0-nibbles to get multiples of 16 bits.

The download must be initiated in the following sequence:

– Issue *Freeze* command

– Stop all DMA transfers

– Issue *Fast Program Download* command

– Download code via PIO interface

– Switch appropriate memory area to act as program RAM (register ED_{hex})

– Issue *Run* command to start program execution at entry point of downloaded code

Example for *Fast Program Download* command:
Download 4 words starting at D0:1400:

	(stop all data transfers)
`<DW 68 00 00>`	*Freeze*
`<DW 68 60 04 10 00>`	initiate download of 4 words start at address D0:1000

Now transfer 8-bit words via the parallel PIO port:

```
0,0  0,d4  d3,d2  d1,d0
0,0  0,d4  d3,d2  d1,d0
0,0  0,d4  d3,d2  d1,d0
0,0  0,d4  d3,d2  d1,d0
```

`<DW 68 be d0 00 03>`	reconfigure memory from D0:1000 to D0:17ff
`<DW 68 10 00>`	start program execution at address D0:1000

3.3.1.15. Serial Program Download

Program downloads may also be performed via the I²C interface by using the Write D0/1 Memory commands. A similar command sequence as in the Fast Program Download (stop transfers, *Freeze*...) applies.

3.3.2. List of DSP Registers

Table 3–5 lists the registers used in the standard Layer 2/3 and AAC firmware (MPEG) and for the download option (Download).

Note: Registers not given in the tables must not be written.

Table 3–5: DSP Register Table

Address (hex)	R/W	Function	Mode	Default (hex)	Name
6B	R/W	**Configuration of Variable RAM Areas** Affected RAM area bit[19] D0:800 ... D0:BFF bit[18] D0:C00 ... D0:FFF bit[17] D1:800 ... D1:BFF bit[16] D1:C00 ... D1:FFF This register is used to switch four RAM areas from data to program usage and thus enabling the DSP’s program counter to access downloaded program code stored at these locations. For normal operation (firmware in ROM) this register must be kept to zero. For details of program code download please refer to Section 3.3.1.14.	**Download**	0000	PSelect_Shadow

Table 3–5: DSP Register Table

Address (hex)	R/W	Function	Mode	Default (hex)	Name
aa	W	**Soft Mute** %0 (reset) mute off %1 mute on **Note**: The location of the SoftMute register is to be changed.	**MPEG**	0000	SoftMute

3.3.3. List of DSP Memory Cells

Among the user interface control memory cells there are some which have a global meaning and some which control application specific parts of the DSP core. In the tables below this is reflected by the keywords All, MPEG, and G.729

3.3.3.1. Application Select and Running

The AppSelect cell is a global user interface configuration cell, which has to be written in order to start a specific application.

The AppRunning cell is a global user interface status cell, which indicates, which application loop is actually running.

The meaning of the bits in both cells is given in Table 3–6.

3.3.3.2. Application Specific Control

The configuration of the MPEG Layer 2/3, AAC decoding and the G.729 codec firmware is done via the control memory cells described in Table 3–7. The changes applied to any of the control memory cells have to be validated by setting bit[0] of memory cell Main I/O Control. This bit will be reset automatically after the changes have been taken over by the DSP.

The status memory cells are used to read the decoder status and to get additional MPEG bitstream information.

Note: Memory cells not given in the tables must not be written.

Table 3–6: Application Control and Status

Memory Address (hex)	Function	Name
D0:34b	**Application Selection** **All** AppSelect is used for selecting an application. This is done by setting the appropriate bit to one. It is principally allowed to set more than one bit to one, e.g. setting AppSelect to 0x1c will select all MPEG audio decoders. The auto-detection feature will automatically detect the Layer 2, Layer 3, or AAC data. Setting bit[0] or bit[1] will make the DSP loop in the OS loop or the Top Level loop respectively. To add/remove MPEG layers while running in MPEG decoding mode (e.g. Layer 2, Layer 3 (0x0c) to Layer 2, Layer 3, AAC (0x1c)), the application selection has to be reset before writing the new value. bit[5] G.729 Codec bit[4] MPEG AAC Decoder bit[3] MPEG Layer 3 Decoder bit[2] MPEG Layer 2 Decoder bit[1] Top Level bit[0] Operating System	**AppSelect**
D0:34c	**Application Running** **All** The AppRunning cell is a global user interface status cell, that indicates which application loop is actually running. Prior to writing any of the configuration registers or memory cells (except AppSelect), it has to be checked whether the appropriate bit(s) in the AppRunning cell is set. bit[5] G.729 Codec bit[4] MPEG AAC Decoder bit[3] MPEG Layer 3 Decoder bit[2] MPEG Layer 2 Decoder bit[1] Top Level bit[0] Operating System	**AppRunning**

Table 3–7: D0 Control Memory Cells

Memory Address (hex)	Function	Name
D0:346	**Main I/O Control** (reset = 24_{hex}) **MPEG** IOControlMain is used for selecting/deselecting the appropriate data input interface and for setting up the serial data output interface. In serial input mode the coded audio data (Layer 2, Layer 3, AAC) is expected at the serial input interface SDIB (default). In the 8-bit-parallel input mode the PIO pins PI[19:12] are used. bit[15] Reserved, must be set to zero bit[14] Invert serial output clock (SOC) 0 (reset) do not invert SOC 1 invert SOC bit[13:12] Reserved, must be set to zero bit[11] Serial data output delay 0 (reset) no additional delay (reset) 1 additional delay of data related to word strobe bit[10] Reserved, must be set to zero bit[9:8] Input Select Main 00 (reset) serial input at interface B 01 parallel input at PIO pins PI[19...12] 10 S/PDIF input (not yet supported) 11 no main input In the standard firmware the serial input interface A (SDI) cannot be selected. bit[7:6] Reserved, must be set to zero bit[5] SDO Word Strobe Invert 0 do not invert 1 (reset) invert outgoing word strobe signal bit[4] Bits per Sample at SDO 0 (reset) 32 bits/sample 1 16 bits/sample bit[3] Reserved, must be set to zero bit[2] Serial data input interface B clock invert (pin SIBC) 0 not inverted (data latched at rising clock edge) 1 (reset) incoming clock signal is inverted (data latched at falling clock edge) bit[1] 0 (reset) DEMAND MODE (PLL off, MAS 35x9F is clock master) 1 BROADCAST MODE (PLL on, clock of MAS 35x9F locks on data stream) bit[0] Validate 0 (reset) changes in control memory cell will be ignored 1 changes in control memory will become effective Bit[0] is reset after the DSP has recognized the changes. The controller should set this bit after the other D0 control memory cells have been initialized with the desired values.	IOControlMain

Table 3–7: D0 Control Memory Cells

Memory Address (hex)	Function	Name
D0:347	**Interface Status Control** (reset = 04_{hex}) **MPEG** This control cell allows to enable/disable the data I/O interfaces. In addition, the clock of the output data interface interfaces, S/PDIF and SDO, can be set to a low-impedance mode. bit[6] S/PDIF input selection (not yet supported) 0 (reset) select S/PDIF input 1 1 select S/PDIF input 2 bit[5] Enable/disable S/PDIF output (will be supported in the next version) 0 (reset) enable S/PDIF output 1 S/PDIF output off (tristate) bit[4] Reserved, must be set to zero bit[3] Enable/disable serial data output SDO 0 SDO on 1 (reset) SDO off bit[2] Output clock characteristic (SDO and S/PDIF outputs) 0 low impedance 1 (reset) high impedance bit [1:0] reserved, must be set to zero Both digital outputs, S/PDIF and I^2S, and the D/A converters may use the decoded audio independent of each other. Changes at this memory address must be validated by setting bit [0] of D0:346.	InterfaceControl
D0:348	**Oscillator Frequency** (reset = 18432_{dec}) **All** bit[19:0] oscillator frequency in kHz In order to achieve a correct internal operating frequency of the DSP, the nominal crystal frequency has to be deposited into this memory cell. Changes at this memory address must be validated by setting bit 0 of D0:346.	OfreqControl

Table 3–7: D0 Control Memory Cells

Memory Address (hex)	Function	Name
D0:349	**Output Clock Configuration** (pin CLKO) (reset = 80000_{hex}) **All** bit[19] CLKO configuration 0 output clock signal at CLKO 1 (reset) CLKO is tristate The CLKO output pin of the MAS 35x9F can be disabled via bit [19]. bit[18] Reserved, must be set to zero bit[17] Additional division by 2 if scaler is on (bit[8] cleared) 0 (reset) oversampling factor 512/768 1 oversampling factor 256/384 bit[16:9] Reserved, must be set to zero bit[8] Output clock scaler 0 (reset) set output clock according to audio sample rate (see Table 2–1) 1 output clock fixed at 24.576 or 22.5792 MHz For a list of output frequencies at pin CLKO please refer to Table 2–1. bit[7:0] reserved, must be set to zero Changes at this memory address must be validated by setting bit[0] of D0:346.	OutClkConfig

Table 3–7: D0 Control Memory Cells

Memory Address (hex)	Function	Name
D0:34d	**Operation Mode Selection** (reset = 0_{hex}) **G.729** The register is used to switch between basic G.729 operation modes. bit[19:7] Reserved, set to 0 bit[6] Page headers 0 enable 1 disable If the page headers bit is 0, a header frame is transfered before each page of 50 data frames. If the header bit is 1, all the frames are G.729 data frames. Please refer to Section 3.3.6. on page 41. bit[5:4] Decoding speed 00 8 kHz (normal) 01 6 kHz (slow) 10 12 kHz (fast) 11 not allowed The recording (encoding) is always done with a sampling rate of 8 kHz. During decoding this control can be used to speed up or slow down the playback. bit[3] Reserved, set to 0 bit[2] Pause encoder/decoder 0 normal operation 1 pause If the pause bit is set, the processing continues until the current page is finished and then en-/decoding is paused. The pause mode lasts until the pause bit is cleared again or the mode is set to 0. bit[1:0] Mode 00 idle 01 decode 10 not allowed 11 encode To switch to **encoder** operation mode, UserControl has to be set to 3_{hex}. Then 50 frames are encoded and sent via the PIO interface. This is repeated until the UserControl register is changed. If the transmission of headers is enabled, each page of 50 frames is preceeded by a header frame as shown in Fig. 3–5. To switch to **decoder** operation mode, UserControl has to be set to 1_{hex}. For decoding with slow speed, UserControl must be 11_{hex}, for decoding with fast speed it must be 21_{hex}. Then the decoder is requesting several frames via the PIO interface to fill its internal buffer. If enough data is available, 50 frames are decoded. This is repeated until the UserControl register is changed. If the transmission of headers is enabled, a header frame (as shown in Fig. 3–5) has to be sent before each page of 50 frames. To switch off the encoder or decoder, UserControl has to be set to 0_{hex}. Then the encoding/decoding and sending/receiving of frames continues until the end of the current page and the operation mode is set to stop.	UserControl

Table 3–7: D0 Control Memory Cells

Memory Address (hex)	Function	Name
D0:34e	**The G.729 encoder is not working with the internal ADC and both, input and output wordstrobe inverted (reset configuration). Therefore this memory cell must be set to 0 to work with the integrated ADC.** **I²S Audio Input/Output Interface** (reset = 60_{hex}) **G.729** bit[19:15] Reserved, set to 0 bit[14] Output clock signal 0 standard signal 1 inverted signal bit[13] Reserved, set to 0 bit[12] Additional delay of input data related to word strobe 0 no delay 1 1 bit delay bit[11] Additional delay of output data related to word strobe 0 no delay 1 1 bit delay bit[10:7] Reserveded, set to 0 bit[6] Input word strobe signal 0 standard signal 1 inverted signal bit[5] Output word strobe signal 0 standard signal 1 inverted signal bit[4] Wordlength 0 32 bits/sample 1 16 bits/sample This setting affects the wordlength on the SDI and SDO interfaces. bit[3] Input clock signal 0 standard signal 1 inverted signal bit[2:0] Reserved, set to 0 Changes become effective when the codec is started or the mode is changed by writing to the UserControl memory cell.	SDISDOConfig
D0:34f	**Interface Status Control** (reset = 25_{hex}) **G.729** This control cell is used to enable/disable interfaces in G.729 mode. It contains the same settings as memory cell D0:347 (InterfaceControl), but is initialized to a different default setting.	g729_InterfaceControl
D0:352	**Volume input control: left gain** (reset=80000_{hex}) **G.729**	in_L
D0:353	**Volume input control: right gain** (reset=0_{hex}) **G.729**	in_R
D0:354	**Volume output control: left → left gain** (reset=80000_{hex}) **All**	out_LL
D0:355	**Volume output control: left → right gain** (reset=0_{hex}) **All**	out_LR

Table 3–7: D0 Control Memory Cells

Memory Address (hex)	Function		Name
D0:356	**Volume output control: right → left gain**(reset=0_{hex})	**All**	out_RL
D0:357	**Volume control: right → right gain** (reset=80000_{hex})	**All**	out_RR

Table 3–8: D0 Status Memory Cells

Memory Address	Function	Name
D0:FD0	**MPEG Frame Counter** bit[19:0] number of MPEG frames after synchronization The counter will be incremented with every new frame that is decoded. With an invalid MPEG bit stream at its input (e.g. an invalid header is detected), the MAS 35x9F resets the MPEGFrameCount to ‘0’.	MPEGFrameCount
D0:FD1	**MPEG Header and Status Information** bit[15] reserved, must be set to zero bit[14:13] MPEG ID, Bits 12, 11 of the MPEG header 00 MPEG 2.5 01 reserved 10 MPEG 2 11 MPEG 1 not valid in case of AAC decoding (bit[12:11] = 00) bit[12:11] Bits 14 and 13 of the MPEG header 00 AAC 01 Layer 3 10 Layer 2 11 Layer 1 bit[10] CRC Protection 0 bitstream protected by CRC 1 bitstream not protected by CRC bit[9:2] Reserved bit[1] CRC error 0 no CRC error 1 CRC error bit[0] Invalid frame 0 no invalid frame´ 1 invalid frame This location contains bits 15...11 of the original MPEG header and other status bits. It will be set each frame directly after the header has been decoded from the bit stream.	MPEGStatus1

Table 3–8: D0 Status Memory Cells

Memory Address	Function	Name
D0:FD2	**MPEG Header Information** bit[15:12] MPEG Layer 2/3 Bitrate MPEG1, L2 / MPEG1, L3 / MPEG2+2.5, L2/3 0000 free free free 0001 32 32 8 0010 48 40 16 0011 56 48 24 0100 64 56 32 0101 80 64 40 0110 96 80 48 0111 112 96 56 1000 128 112 64 1001 160 128 80 1010 192 160 96 1011 224 192 112 1100 256 224 128 1101 320 256 144 1110 384 320 160 1111 forbidden forbidden forbidden bit[13:10] Sampling frequency for MPEG2-AAC in Hz 0000..0010 reserved 0011 48000 0100 44100 0101 32000 0110 24000 0111 22050 1000 16000 1001 12000 1010 11025 1011 8000 1100..1111 reserved ...	MPEGStatus2

Table 3–8: D0 Status Memory Cells

Memory Address	Function	Name
D0:FD2 (continued)	**MPEG Header Information, continued** bit[11:10] Sampling frequencies in Hz MPEG1 MPEG2 MPEG2.5 00 44100 22050 11025 01 48000 24000 12000 10 32000 16000 8000 11 reserved reserved reserved bit[9] Padding Bit bit[8] reserved bit[7:6] Mode 00 stereo 01 joint_stereo (intensity stereo / m/s stereo) 10 dual channel 11 single channel bit[5:4] Mode extension (applies to joint stereo only) intensity stereo m/s stereo 00 off off 01 on off 10 off on 11 on on bit[3] Copyright Protect Bit 0/1 not copyright protected/copyright protected bit[2] Copy/Original Bit 0/1 bitstream is a copy/bitstream is an original bit[1:0] Emphasis, indicates the type of emphasis 00 none 01 50/15 µs 10 reserved 11 CCITT J.17 This memory cell contains the 16 LSBs of the MPEG header. It will be set directly after synchronizing to the bit stream. Note that for AAC four bits are needed to define the sampling frequency while for Layer2/Layer3 two bits are sufficient. This leads to an inconsistency in the format of bits 13...10.	MPEGStatus2
D0:FD3	**MPEG CRC Error Counter** The counter will be increased by each CRC error detected in the MPEG bisstream. It will not be reset when losing the synchronization.	CRCErrorCount
D0:FD4	**Number of Bits in Ancillary Data** Number of valid ancillary bits in the current MPEG frame.	NumberOfAncillary-Bits
D0:FD5 ... D0:FF1	**Ancillary Data** Section 3.3.4. on page 40.	AncillaryData

3.3.4. Ancillary Data

The memory fields D0:FD5...D0:ff1 contain the ancillary data. It is organized in 28 words of 16 bit each. The last ancillary bit of a frame is placed at bit 0 in D0:FD5. The position of the first ancillary data bit received can be located via the content of NumberOfAncillaryBits because

int[(NumberOfAncillaryBits-1)/16] + 1

of memory words are used.

Example:

First get the content of 'NumberOfAncillaryBits'

```
<DW 68 c4 00 00 01 0f d4>
<DW 69 <DR dd dd>
```

Assume that the MAS 35x9F has received 19 ancillary data bits. Therefore, it is necessary to read two 16-bit words:

```
<DW 68 c4 00       Short Read from D0
  00 02 0f d5>     read 2 words starting at D0:fd5
<DW 69 <DR dd dd
           dd dd>
                   receive the 2 16-bit words
```

The first bit received from the MPEG source is at position 2 of D0:FD6; the last bit received is at the LSB of D0:fd5.

3.3.5. DSP Volume Control

The digital baseband volume matrix is used for controlling the digital gain as shown in Fig. 3–3. This volume control is effective on both, the digital audio output and the data stream to the D/A converters. The values are in 20-bit 2's complement notation.

Table 3–9 shows the proposed settings for the 4 volume matrix coefficients for stereo, left and right mono. The gain factors are given in fixed point notation ($-1.0\times2^{19} = 80000_{hex}$).

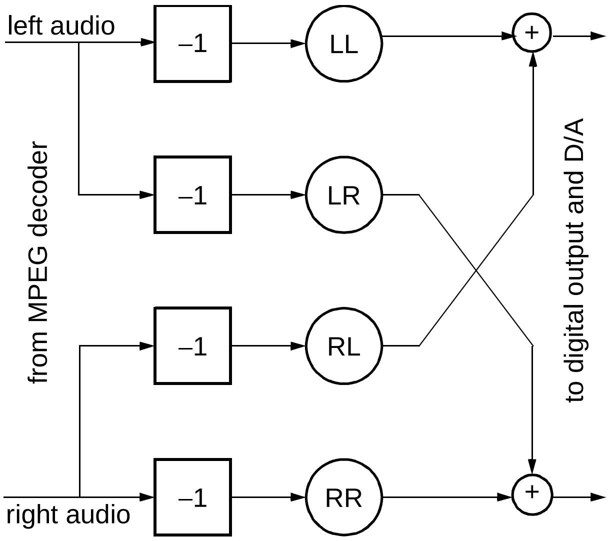


Fig. 3–3: Digital volume matrix

Table 3–9: Settings for the digital volume matrix

Memory	**D0:354**	**D0:355**	**D0:356**	**D0:357**
Name	**LL**	**LR**	**RL**	**RR**
Stereo (default)	–1.0	0	0	–1.0
Mono left	–1.0	–1.0	0	0
Mono right	0	0	–1.0	–1.0

If channels are mixed, care must be taken to prevent clipping at high amplitudes. Therefore the sum of the absolute values of coefficients for one output channel should be less than 1.0.

For normal operating conditions it is recommended to use the main volume control of the audio codec instead (register 00 10_{hex} of the audio codec).

Table 3–10: Content of D0:fd5 after reception of 19 ancillary bits.

D0:fd5	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
Ancillary Data	4th bit	5th bit	6th bit	...	...	...	...	...	...	...	...	...	...	17th bit	18th bit	last bit

Table 3–11: Content of D0:fd6 after reception of 19 ancillary bits.

D0:fd6	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
Ancillary Data	x	x	x	x	x	x	x	x	x	x	x	x	x	first bit	2nd bit	3rd bit

3.3.6. Explanation of the G.729 Data Format

The codec is working on a page basis where the encoding and decoding is performed in blocks of 50 G.729 frames, whereas each frame consists of 10 bytes in byteswapped order (see Fig. 3–5 on page 49). Therefore most changes to the UserControl register become effective when processing of the current page is finished. The pages are optionally preceeded by 10 byte header frames (see Table 3–12).

Table 3–12: Content of Page Header

Byte	1	2	3	4	5	6	7	8	9	10
Value (hex)	64	6d	72	31	64	61	74	61	F4	01

Switching directly from encoding to decoding mode or vice versa is not allowed. Instead the controller has to send a stop request to the MAS 35x9F (writing 0_{hex} to UserControl) and must keep on sending data in decoding mode or receive data in encoding mode until the current page of 50 frames is finished. After this run out time, the encoding or decoding can be started again.

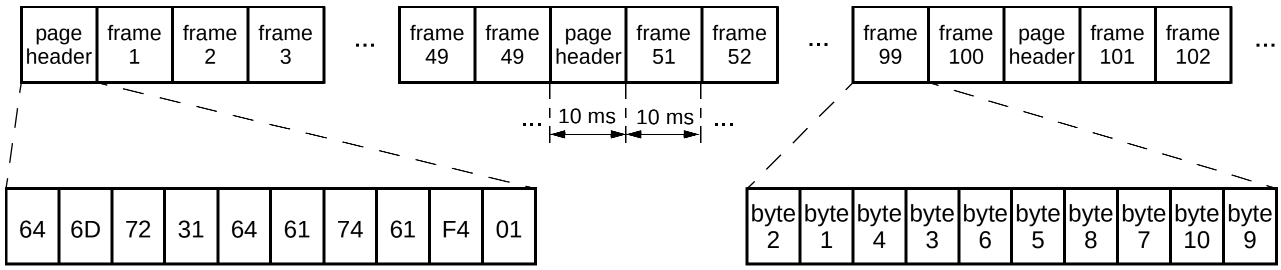


Fig. 3–4: Schematic timing of the data transmission with preceeding header

3.4. Audio Codec Access Protocol

The MAS 35x9F has 16-bit wide registers for the control of the audio codec. These registers are accessed via the I²C subaddresses codec_write ($6C_{hex}$) and codec_read ($6D_{hex}$).

3.4.1. Write Codec Register

S	DW	A	codec_write	A	r3,r2	A	r1,r0	A	
					d3,d2	A	d1,d0	A	P

The controller writes the 16-bit value (**d** = d3,d2,d1,d0) into the MAS 35x9F codec register (**r** = r3,r2,r1,r0). A list of registers is given in Table 3–13.

Example: Writing the value 1234_{hex} into the codec register with the number 00 $1B_{hex}$:

```
<DW 6c 00 1b 12 34>
```

3.4.2. Read Codec Register

1) send command

S	DW	A	codec_write	A	r3,r2	A	r1,r0	A	P

2) get register value

S	DW	A	codec_read	A	S	DR	A		
					d3,d2	A	d1,d0	N	P

Reading the codec registers also needs a set-up for the register address and an additional start condition during the actual read cycle. A list of registers is given in Table 3–14.

3.4.3. Codec Registers

Table 3–13: Codec control registers on I^2C subaddress $6c_{hex}$

Register Address (hex)	Function	Name
CONVERTER CONFIGURATION		
00 00	**Audio Codec Configuration** Please refer to Section 4.6.4. on page 74. bit[15:12] A/D converter left amplifier gain = n*1.5–3 [dB] bit[11:8] A/D converter right amplifier gain = n*1.5–3 [dB] 1111 +19.5 dB 1110 +18.0 dB ... ... 0011 +1.5 dB 0010 0.0 dB 0001 –1.5 dB 0000 – 3.0 dB bit[7:4] Microphone amplifier gain = n*1.5+21 [dB] 1111 +43.5 dB 1110 +42.0 dB ... ... 0001 +22.5 dB 0000 +21.0 dB bit[3] Input selection for left A/D converter channel 0 line-in 1 microphone bit[2] Enable left A/D converter[1)] bit[1] Enable right A/D converter[1)] bit[0] Enable D/A converter[1)]	CONV_CONF
	[1)] The generation of the internal DC reference voltage for the D/A converter is also controlled with this bit. In order to avoid click noise, the reference voltage at pin AGNDC should have reached a near ground potential before repowering the D/A converter after a short down phase. Alternatively at least one of the A/D converters (bits [2] or [1]) should remain set during short power-down phases of the D/A. Then the DC reference voltage generation for the D/A converter will not be interrupted.	
INPUT MODE SELECT		
00 08	**Input Mode Setting** bit[15] Mono switch 0 stereo input mode 1 left channel is copied into the right channel bit[14:2] Reserved, must be set to 0 bit[1:0] Deemphasis select 0 deemphasis off 1 deemphasis 50 µs 2 deemphasis 75 µs	ADC_IN_MODE

Table 3–13: Codec control registers on I^2C subaddress $6c_{hex}$

Register Address (hex)	Function	Name
OUTPUT MODE SELECT		
00 0F [1]	**D/A Converter Source** bit[15] D/A converter source select 0 DSP Core output 1 A/D converter output bit[14:0] reserved, must be set to 0	DAC_IN_SEL
	D/A Converter Source Mixer	
00 06[2]	**MIX ADC scale**	DAC_IN_ADC
00 07[2]	**MIX DSP scale** bit[15:8] Linear scaling factor (hex) 0 off 20 50 % (–6 dB gain) 40 100 % (0 dB gain) 7f 200 % (+6 dB gain) In the sum of both mixing inputs exceeds 100 %, clipping may occur in the successive audio processing.	DAC_IN_DSP
00 0E	**D/A Converter Output Mode** bit[15] Mono switch 0 stereo through 1 mono matrix applied bit[14] Invert right channel 0 through 1 right channel is inverted bit[1:0] Reserved, must be set to 0 In order to achieve more output power a single loudspeaker can be connected as a bridge between pins OUTL and OUTR. In this mode bit[15] and bit[14] must be set.	DAC_OUT_MODE
[1] Version A1 only [2] since version A2		

Table 3–13: Codec control registers on I²C subaddress $6c_{hex}$

Register Address (hex)	Function	Name
BASEBAND FEATURES		
00 14	**Bass** bit[15:8] Bass range 60_{hex} +12 dB 58_{hex} +11 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ –1 dB ... $A8_{hex}$ –11 dB $A0_{hex}$ –12 dB Higher resolution is possible, one LSB step results in a gain step of about 1/8 dB. With positive bass settings clipping of the output signal may occur. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain. The settings require: max (bass, treble) + loudness + volume ≤ 0 dB bit[7:0] Not used, must be set to 0	BASS
00 15	**Treble** bit[15:8] Treble range 60_{hex} +12 dB 58_{hex} +11 dB ... 08_{hex} +1 dB 00_{hex} 0 dB $F8_{hex}$ –1 dB ... $A8_{hex}$ –11 dB $A0_{hex}$ –12 dB Higher resolution is possible, one LSB step results in a gain step of about 1/8 dB. With positive treble settings, clipping of the output signal may occur. Therefore, it is not recommended to set treble to a value that, in conjunction with loudness and volume, would result in an overall positive gain. The settings require: max (bass, treble) + loudness + volume ≤ 0 dB bit[7:0] Not used, must be set to 0	TREBLE

Table 3–13: Codec control registers on I^2C subaddress $6c_{hex}$

Register Address (hex)	Function	Name
00 1E	**Loudness** bit[15:8] Loudness Gain 44_{hex} +17 dB 40_{hex} +16 dB ... 04_{hex} +1 dB 00_{hex} 0 dB bit[7:0] Loudness Mode 00_{hex} normal (constant volume at 1 kHz) 04_{hex} Super Bass (constant volume at 2 kHz) Higher resolution of Loudness Gain is possible: An LSB step results in a gain step of about 1/4 dB. Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the 1-kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain. The settings should be: max (bass, treble) + loudness + volume ≤ 0 dB The corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz.	LDNESS

Table 3–13: Codec control registers on I^2C subaddress $6c_{hex}$

Register Address (hex)	Function	Name
Micronas Dynamic Bass (MDB)		
00 22	**MDB Effect Strength** bit[15:8] 00_{hex} MDB off (default) $7F_{hex}$ maximum MDB The MDB effect strength can be adjusted in 1dB steps. A value of 40_{hex} will yield a medium MDB effect.	MDB_STR
00 23	**MDB Harmonics** bit[15:8] 00_{hex} no harmonics are added (default) 64_{hex} 50% fundamentals + 50% harmonics $7F_{hex}$ 100% harmonics The MDB exploits the psychoacoustic phenomenon of the ‘missing fundamental by creating harmonics of the frequencies below the center frequency of the bandpass filter (MDB_FC). This enables a loudspeaker to display frequencies that are below its cutoff frequency. The Variable MDB_HAR describes the ratio of the harmonics towards the original signal.	MDB_HAR
00 24	**MDB Center Frequency** bit[15:8] 2 20 Hz 3 30 Hz ... 30 300 Hz The MDB Center Frequency defines the center frequency of the MDB bandpass filter (see Fig. 3–5 on page 49). The center frequency should approximately match the cutoff frequency of the loudspeakers. For high end loudspeakers, this frequency is around 50 Hz, for low end speakers around 90 Hz	MDB_FC
00 21	**MDB Shape** bit[15:8] 5...30 corner frequency in 10-Hz steps (range: 50...300 Hz) With a second lowpass filter the steepness of the falling slope of the MDB bandpass can be increased (see Fig. 3–5 on page 49). Choosing the corner frequency of this filter close to the center frequency of the bandpass filter (MDB_FC) results in a narrow MDB frequency range. The smaller this range, the harder the bass sounds. The recommended value is around $1.5 \times$ MDB_FC	MDB_SHAPE
	MDB Switch bit[7:2] reserved, must be set to zero bit[1] MDB switch 0 MDB off 1 MDB on bit [0] reserved,must be set to zero	MDB_SWITCH

Table 3–13: Codec control registers on I²C subaddress $6c_{hex}$

Register Address (hex)	Function	Name
VOLUME		
00 12	**Automatic Volume Correction (AVC) Loudspeaker Channel** bit[15:12] 0_{hex} AVC off (and reset internal variables) 8_{hex} AVC on bit[11:8] 8_{hex} 8 s decay time 4_{hex} 4 s decay time 2_{hex} 2 s decay time 1_{hex} 20 ms decay time (intended for quick adaptation to the average volume level after track or source change) **Note:** To reset the internal variables, the AVC should be switched off and then on again during any track or source change. For standard applications, the recommended decay time is 4 s.	AVC
00 11	**Balance** bit[15:8] Balance range $7F_{hex}$ left –127 dB, right 0 dB $7E_{hex}$ left –126 dB, right 0 dB ... 01_{hex} left –1 dB, right 0 dB 00_{hex} left 0 dB, right 0 dB FF_{hex} left 0 dB, right –1 dB ... 81_{hex} left 0 dB, right –127 dB 80_{hex} left 0 dB, right –128 dB Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected.	BALANCE
00 10	**Volume Control** bit[15:8] Volume table with 1 dB step size $7F_{hex}$ +12 dB (maximum volume) $7E_{hex}$ +11 dB ... 74_{hex} +1 dB 73_{hex} 0 dB 72_{hex} –1 dB ... 02_{hex} –113 dB 01_{hex} –114 dB 00_{hex} mute (reset) bit[7:0] Not used, must be set to 0 This main volume control is applied to the analog outputs only. It is split between a digital and an analog function. In order to avoid noise due to large changes of the setting, the actual setting is internally low-pass filtered. With large scale input signals, positive volume settings may lead to signal clipping.	VOLUME

Table 3–14: Codec status registers on I²C subaddress $6d_{hex}$

Register Address (hex)	Function	Name
INPUT QUASI-PEAK		
00 0A	**A/D Converter Quasi-Peak Detector Readout Left** bit[14:0] positive 15-bit value, linear scale 0000 0 % 2000 25 % (–12 dBFS) 4000 50 % (–6 dBFS) 7FFF 100 % (0 dBFS)	QPEAK_L
00 0B	**A/D Converter Quasi-Peak Detector Readout Right** bit[14:0] positive 15-bit value, linear scale 0000 0 % 2000 25 % (–12 dBFS) 4000 50 % (–6 dBFS) 7FFF 100 % (0 dBFS)	QPEAK_R
OUTPUT QUASI-PEAK		
00 0C	**Audio Processing Input Quasi-Peak Detector Readout Left** bit[14..0] positive 15-bit value, linear scale	DQPEAK_L
00 0D	**Audio Processing Input Quasi-Peak Detector Readout Right** bit[14..0] positive 15-bit value, linear scale	DQPEAK_R

3.4.4. Basic MDB Configuration

With the parameters described in Table 3–13, the Micronas Dynamic Bass system (MDB) can be customized to create different bass effects as well as to fit the MDB to various loudspeaker characteristics. The easiest way to find a good set of parameter is by selecting one of the settings below, listening to music with strong bass content and adjusting the MDB parameters:

– MDB_STR: Increase/decrease the strength of the MDB effect

– MDB_HAR: Increase/decrease the content of low frequency harmonics

– MDB_FC: Shift the MDB effect to lower/higher frequencies

– MDB_SHAPE: Widen/narrow MDB frequency range (which results in a softer/harder bass sound), turn on/off the MDB

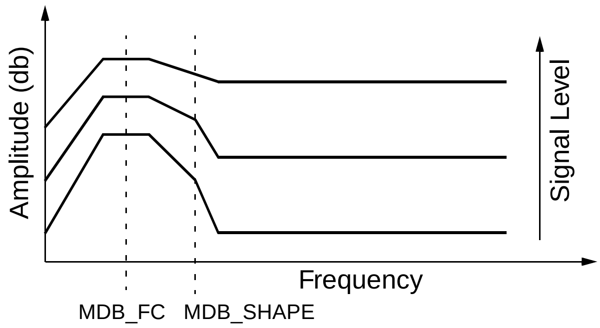


Fig. 3–5: Micronas Dynamic Bass (MDB): Bass boost in relation to input signal leve

Table 3–15: suggested MDB settings

Function	MDB_STR (22_{hex})	MDB_HAR (23_{hex})	MDB_FC (24_{hex})	MDB_SHAPE (21_{hex})
MDB off	$xxxx_{hex}$	$xxxx_{hex}$	$xxxx_{hex}$	$xx00_{hex}$
Low end headphones, medium effect	5000_{hex}	3000_{hex}	0600_{hex}	0902_{hex}
Low end headphones, strong effect	**tbd**	**tbd**	**tbd**	**tbd**
High end headphones, medium effect	**tbd**	**tbd**	**tbd**	**tbd**
High end headphones, strong effect	**tbd**	**tbd**	**tbd**	**tbd**

4. Specifications

4.1. Outline Dimensions

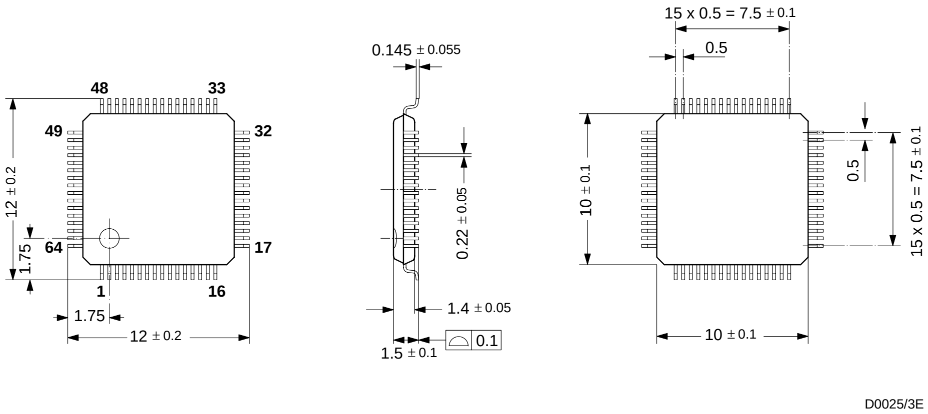


Fig. 4–1:
64-Pin Plastic Low-Profile Quad Flat Pack
(PLQFP64)
Weight approximately 0.35 g
Dimensions in mm

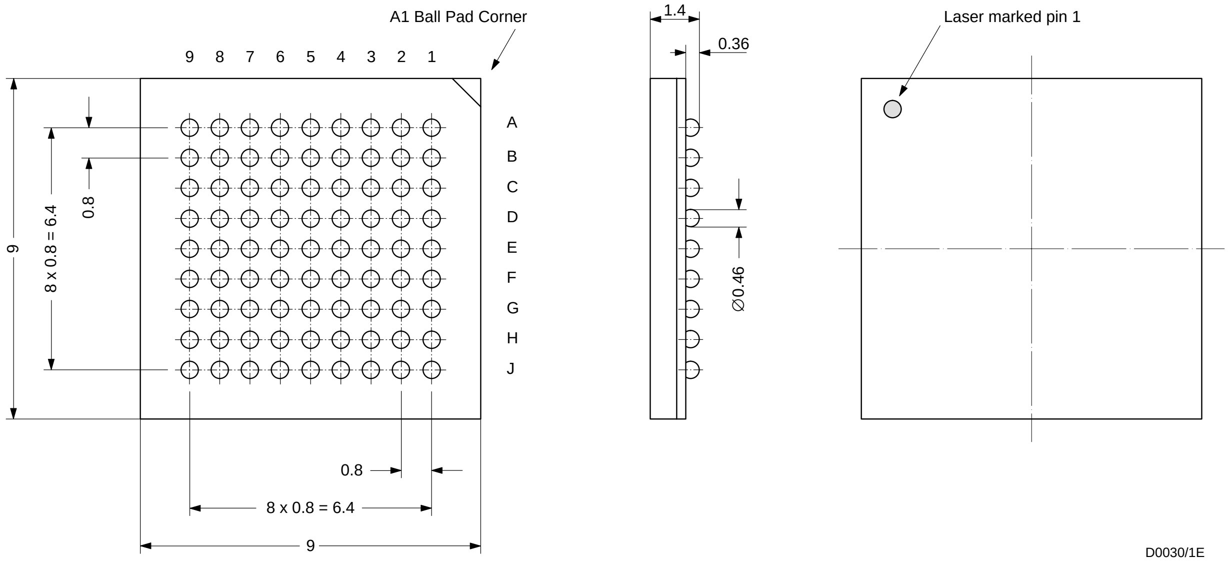


Fig. 4–2:
Plastic Ball Grid Array 81-Pin
(LFBGA81)
Weight approximately 0.19 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC not connected, leave vacant
LV If not used, leave vacant
X obligatory, pin must be connected as described in application information (see Fig. 4–32 on page 80)

VDD connect to positive supply
VSS connect to ground

Pin No. PLQFP 64	Pin No. LFBGA 81	Pin Name	Type	Default Connection (if not used)	Short Description
1	H2	AGNDC		X	Analog reference voltage
2	J2	MICIN	IN	LV	Input for internal microphone amplifier
3	J3	MICBI	IN	LV	Bias for internal microphone
4	H3	INL	IN	LV	Left A/D input
5	H4	INR	IN	LV	Right A/D input
6	G4	TE	IN	X	Test enable
7	J4	XTI	IN	X	Crystal oscillator (ext. clock) input
8	J5	XTO	OUT	LV	Crystal oscillator output
9	G5	$\overline{\text{POR}}$	IN	X	Power on reset, active low
10	H5	VSS	SUPPLY	X	DSP supply ground
11	J6	XVSS	SUPPLY	X	Digital output supply ground
12	J7	VDD	SUPPLY	X	DSP supply
13	H6	XVDD	SUPPLY	X	Digital output supply
14	H7	I2CVDD	SUPPLY	X	I^2C supply
15	G6	DVS	SUPPLY	X	I^2C device address selector
16	J8	VSENS1	IN/OUT	VDD	Sense input and power output of DC/DC 1 converter
17	J9	DCSO1	SUPPLY	LV	DC/DC 1 switch output
18	H8	DCSG1	SUPPLY	VSS	DC/DC 1 switch ground
19	H9	DCSG2	SUPPLY	VSS	DC/DC 2 switch ground
20	G8	DCSO2	SUPPLY	LV	DC/DC 2 switch output
21	G9	VSENS2	IN/OUT	VDD	Sense input and power output of DC/DC 2 converter
22	F8	DCEN	IN	VSS	DC/DC enable (both converters)
23	F9	CLKO	OUT	LV	Clock output
24	E8	I2CC	IN/OUT	X	I^2C clock
25	E9	I2CD	IN/OUT	X	I^2C data

Pin No. PLQFP 64	Pin No. LFBGA 81	Pin Name	Type	Default Connection (if not used)	Short Description
26	E7	SYNC	OUT	LV	Sync output
27	D9	VBAT	IN	LV	Battery voltage monitor input
28	D8	PUP	OUT	LV	DC Converter Power-Up Signal
29	C9	$\overline{\text{EOD}}$	OUT	LV	PIO end of DMA, active low
30	C8	$\overline{\text{PRTR}}$	OUT	LV	PIO ready to read, active low
31	B9	$\overline{\text{PRTW}}$	OUT	LV	PIO ready to write, active low
32	B8	PR	IN	VDD	PIO DMA request, active high
33	A9	$\overline{\text{PCS}}$	IN	VSS	PIO chip select, active low
34	A8	PI19	IN/OUT	LV	PIO data bit 7 (MSB)
35	B7	PI18	IN/OUT	LV	PIO data bit 6
36	A7	PI17	IN/OUT	LV	PIO data bit 5
37	B6	PI16	IN/OUT	LV	PIO data bit 4
38	A6	PI15	IN/OUT	LV	PIO data bit 3
39	C6	PI14	IN/OUT	LV	PIO data bit 2
40	A5	PI13	IN/OUT	LV	PIO data bit 1
41	B5	PI12	IN/OUT	LV	PIO data bit 0 (LSB)
42	C5	SOD	OUT	LV	Serial output data
43	A4	SOI	OUT	LV	Serial output frame identification
44	B4	SOC	OUT	LV	Serial output clock
45	B3	SID	IN	VSS	Serial input data, interface A
46	A3	SII	IN	VSS	Serial input frame identification, interface A
47	C4	SIC	IN	VSS	Serial input clock, interface A
48	E3	SPDO	OUT	LV	S/PDIF output interface
49	A1	SIBD	IN	VSS	Serial input data, interface B
50	A2	SIBC	IN	VSS	Serial input clock, interface B
51	B2	SIBI	IN	VSS	Serial input frame identification, interface B
52	B1	SPDI2	IN	LV	Active differential S/PDIF input 2
53	C2	SPDI1	IN	LV	Active differential S/PDIF input 1
54	D2	SPDIR	IN	LV	Reference differential S/PDIF input 1 and 2

Pin No. PLQFP 64	Pin No. LFBGA 81	Pin Name	Type	Default Connection (if not used)	Short Description
55	C1	FILTL	IN	X	Feedback input for left amplifier
56	E2	AVDD0	SUPPLY	X	Analog supply for output amplifiers
57	D1	OUTL	OUT	LV	Left analog output
58	E1	OUTR	OUT	LV	Right analog output
59	F2	AVSS0	SUPPLY	X	Analog ground for output amplifiers
60	F1	FILTR	IN	X	Feedback for right output amplifier
61	G2	AVSS1	SUPPLY	X	Analog ground
62	G1	VREF		X	Analog reference ground
63	H1	PVDD	SUPPLY	X	Internal power supply
64	J1	AVDD1	SUPPLY	X	Analog Supply
		SUB		VSS	Substrate connection

In the 81-pin LFBGA housing, the pins C3, C7, D3, D4, D5, D6, D7, E4, E5, E6, F3, F4, F5, F6, F7, G3 and G7 are common substrate contacts.

4.3. Pin Descriptions

4.3.1. Power Supply Pins

The use of all power supply pins is mandatory to achieve correct function of the MAS 35x9F.

VDD, VSS **SUPPLY**
Digital supply pins.

XVDD, XVSS **SUPPLY**
Supply for digital output pins.

I2CVDD **SUPPLY**
Supply for I^2C interface circuitry. This net uses VSS or XVSS as the ground return line.

PVDD **SUPPLY**
Auxiliary pin for analog circuitry. This pin has to be connected via a 3-nF capacitor to AVDD1. Extra care should be taken to achieve a low inductance PCB line.

AVDD0/AVSS0 **SUPPLY**
Supply for analog output amplifier.

AVDD1/AVSS1 **SUPPLY**
Supply for internal analog circuits (A/D, D/A converters, clock, PLL, S/PDIF input).

AVDD0/AVSS0 and AVDD1/AVSS1 should receive the same supply voltages.

4.3.2. Analog Reference Pins

AGNDC
Internal analog reference voltage. This pin serves as the internal ground connection for the analog circuitry.

VREF
Analog reference ground. All analog inputs and outputs should drive their return currents using separate traces to a ground starpoint close to this pin. Connect to AVSS1. This reference pin should be as noise free as possible.

4.3.3. DC/DC Converters and Battery Voltage Supervision

DCSG1/DCSG2 **SUPPLY**
DC/DC converters switch ground. Connect using separate wide trace to negative pole of battery cell. Connect also to AVSS0/1 and VSS/XVSS.

DCSO1/DCSO2 **SUPPLY**
DC/DC converter switch connection. If the respective DC/DC converter is not used, this pin must be left vacant.

VSENS1/VSENS2 **IN**
Sense input and power output of DC/DC converters. If the respective DC/DC converter is not used, this pin should be connected to a supply.

DCEN **IN**
Enable signal for both DC/DC converters. If none of the DC/DC converters is used, this pin must be connected to VSS.

PUP **OUT**
Power-up. This signal is set when the required voltages are available at both DC/DC converter output pins VSENS1 and VSENS2. The signal is cleared when both voltages have dropped below the reset level in the DCCF Register.

VBAT **IN**
Analog input for battery voltage supervision.

4.3.4. Oscillator Pins and Clocking

XTI **IN**
XTO **OUT**
The XTI pin is connected to the input of the internal crystal oscillator, the XTO pin to its output. Each pin should be directly connected to the crystal and to a ground-connected capacitor (see application diagram, Fig. 4–32 on page 80).

CLKO **OUT**
The CLKO can drive an output clock line.

4.3.5. Control Lines

I2CC **SCL** **IN/OUT**
I2CD **SDA** **IN/OUT**
Standard I^2C control lines.

DVS **IN**
I^2C device address selector. Connect this pin either to VDD (I^2C device address: $3E/3F_{hex}$) or VSS (I^2C device address: $3C/3D_{hex}$) to select a proper I^2C device address (see also Table 3–1 on page 18).

4.3.6. Parallel Interface Lines

PI12..PI19 **IN/OUT**
The PIO input pins PI12..PI19 are used as 8-bit I/O interface to a microcontroller in order to transfer compressed and uncompressed data. PI12 is the LSB, PI19 the MSB.

4.3.6.1. PIO Handshake Lines

$\overline{\text{PCS}}$ **IN**
The PIO chip select $\overline{\text{PCS}}$ must be set to ‘0’ to activate the PIO in operation mode.

PR **IN**
Pin PR must be set to ‘1’ to validate data output from MAS 35x9F PIO pins.

$\overline{\text{PRTR}}$ **OUT**
Ready to read. This signal indicates that the MAS 35x9F is able to receive data in PIO input mode.

$\overline{\text{PRTW}}$ **OUT**
Ready to write. This pin indicates that MAS 35x9F has data available for PIO output mode.

$\overline{\text{EOD}}$ **OUT**
$\overline{\text{EOD}}$ indicates the end of an DMA cycle in the IC’s PIO input mode. In ’serial’ input mode it is used as Demand signal, that indicates that new input data are required.

4.3.7. Serial Input Interface (SDI)

SID **DATA** **IN**
SII **WORD STROBE** **IN**
SIC **CLOCK** **IN**
I^2S compatible serial interface A for digital audio data. In the standard firmware this interface is not used.

4.3.8. Serial Input Interface B (SDIB)

SIBD **DATA** **IN**
SIBI **WORD STROBE** **IN**
SIBC **CLOCK** **IN**
The serial interface B is primarily used as bitstream input interface. The SIBI line must be connected to VSS in the standard application.

4.3.9. Serial Output Interface (SDO)

SOD **DATA** **OUT**
SOI **WORD STROBE** **OUT**
SOC **CLOCK** **IN/OUT**
Data, Frame Indication, and Clock line of the serial output interface. The SOI is reconfigurable and can be adapted to several I^2S compliant modes.

4.3.10. S/PDIF Input Interface

SPDI1 **IN**
SPDI2 **IN**
SPDIR **IN**
SPDIF1 and SPDIF2 are alternative input pins for S/PDIF sources according to the IEC 958 consumer specification. A switch at D0:ff6 selects one of these pins at a time. The SPDIR pin is a common reference for both input lines (see Fig. 4–33 on page 81).

4.3.11. S/PDIF Output Interface

SPDO **OUT**
The SPDO pin provides an digital output with standard CMOS level that is compliant to the IEC 958 consumer specification.

4.3.12. Analog Input Interfaces

In the standard MPEG-decoding DSP firmware the analog inputs are not used. However, they can be selected as a source for the D/A converters (set bit [15] in audio codec register 00 $0F_{hex}$).

MICIN **IN**
MICBI **IN**
The MICIN input may be directly used as electret microphone input, which should be connected as described in application information. The MICBI signal provides the supply voltage for these microphones.

INL **IN**
INR **IN**
INL and INR are analog line-in input lines. They are connected to the embedded stereo A/D converter of the MAS 35x9F. The sources should be AC coupled. The reference ground for these analog input pins is the VREF pin.

4.3.13. Analog Output Interfaces

OUTL **OUT**
OUTR **OUT**
OUTL and OUTR are left and right analog outputs, that may be directly connected to the headphones as described in the application information (see Fig. 4–33 on page 81).

FILTL **IN**
FILTR **IN**
Connection to input terminal of output amplifier.Can be used to connect a capacitance from OUTL respectively OUTR to FILTL respectively FILTR in parallel to feedback resistor and thus implement a low pass filter to reduce the out-of-band noise of the DAC.

4.3.14. Miscellaneous

SYNC **OUT**
The SYNC signal indicates the detection of a frame start in the input data of MAS 35x9F. Usually this signal generates an interrupt in the controller.

$\overline{\text{POR}}$ **IN**
The Power-On Reset pin is used to reset the whole MAS 35x9F, except for the DC/DC converter circuitry. $\overline{\text{POR}}$ is an active-low signal.

TE **IN**
The TE pin is for production test only and must be connected with VSS in all applications.

SUB (LFBGA-81 ONLY)
Chip substrate connection. Must be connected to VSS in all applications.

4.4. Pin Configurations

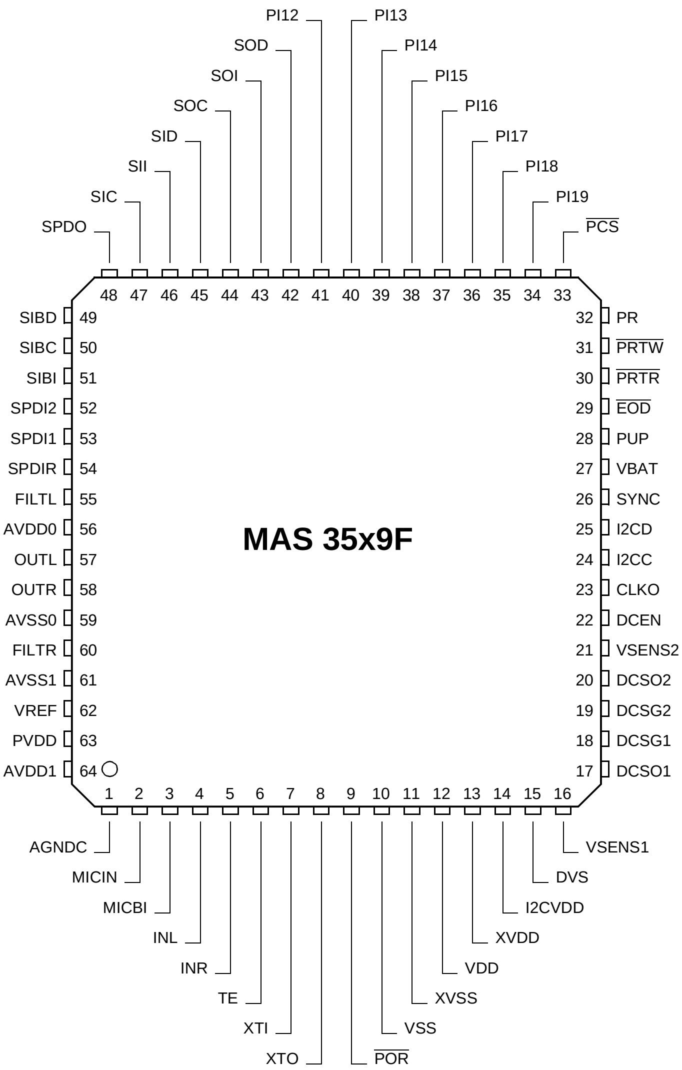


Fig. 4–3: 64-pin PLQFP package

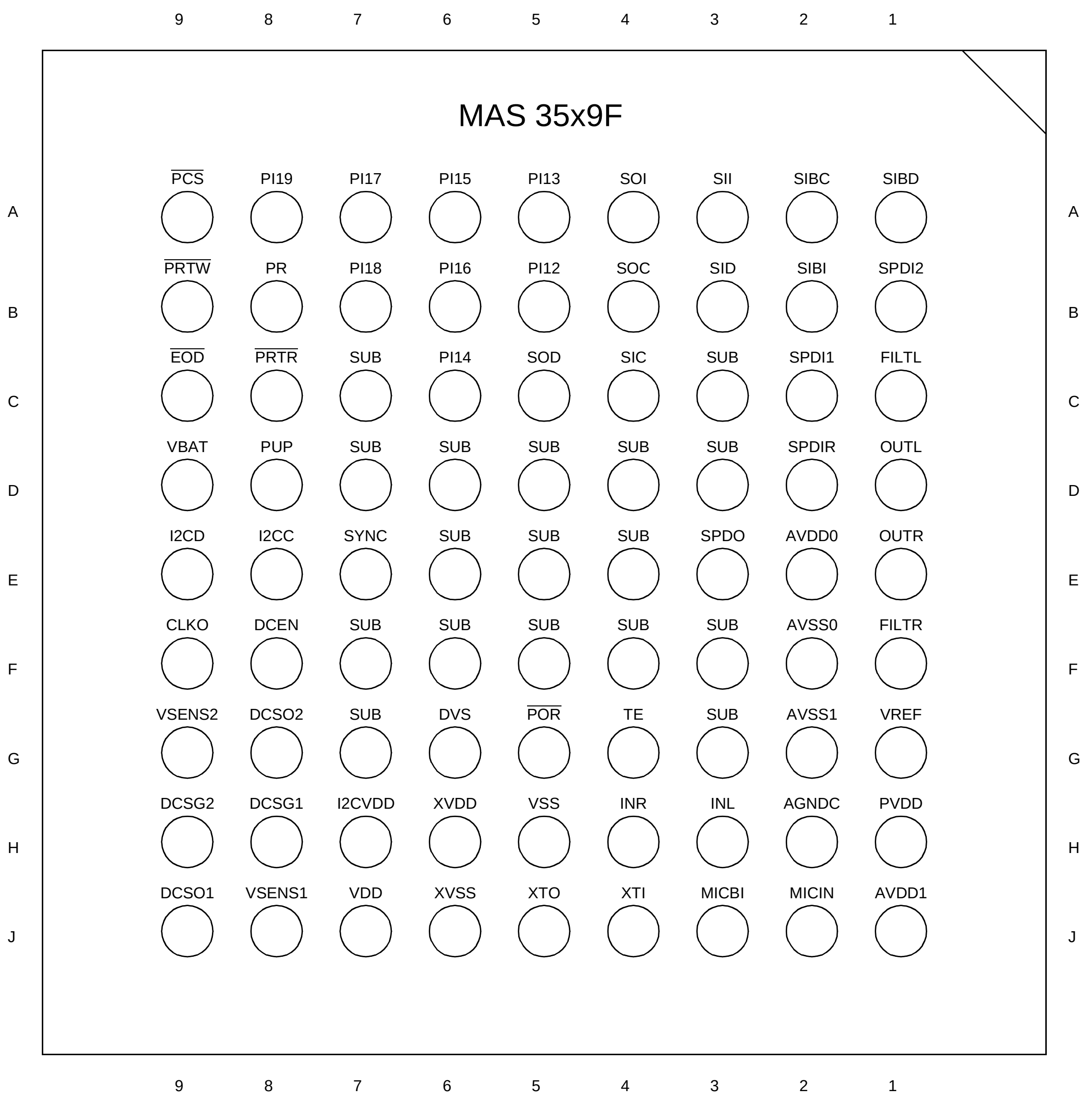


Fig. 4–4: 81-pin LFBGA package

4.5. Internal Pin Circuits

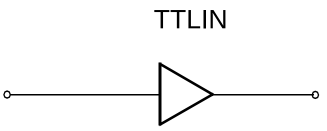


Fig. 4–5: Input pins $\overline{PCS}$, PR

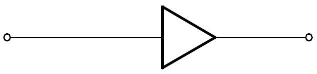


Fig. 4–6: Input pin TE, DVS, $\overline{POR}$

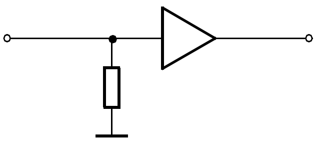


Fig. 4–7: Input pin DCEN

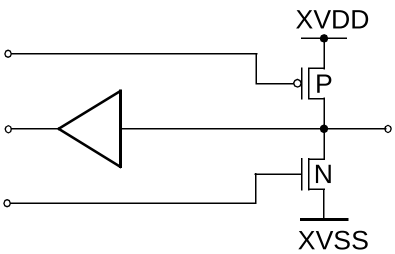


Fig. 4–8: Input/output pins SOC, SOI, SOD, PI12...PI19, SPDO

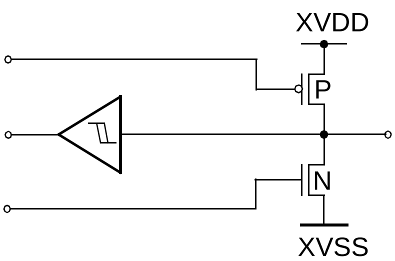


Fig. 4–9: Input pins SI(B)C, SI(B)I, SI(B)D

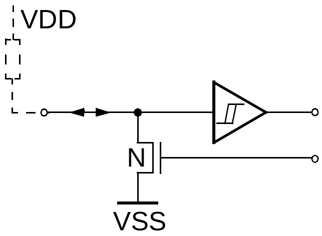


Fig. 4–10: Input/output pins I2CC, I2CD

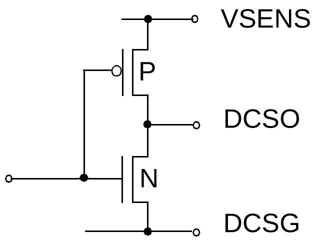


Fig. 4–11: Input/output pins DCSO1/2, DCSG1/2, VSENS1/2

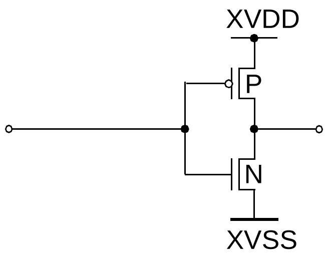


Fig. 4–12: Output pins $\overline{PRTW}$, $\overline{EOD}$, $\overline{PRTR}$, CLKO, SYNC, PUP

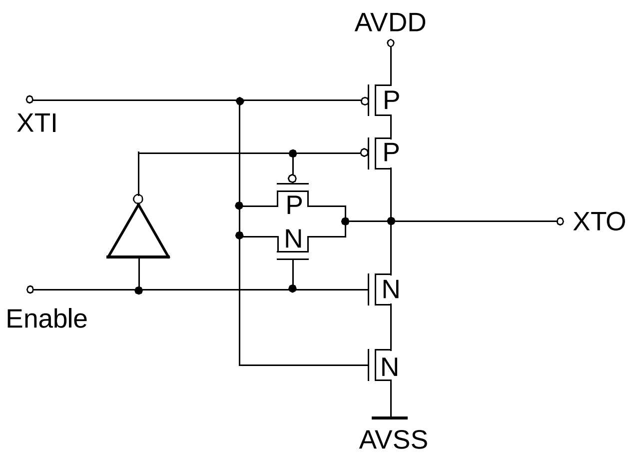


Fig. 4–13: Clock oscillator XTI, XTO

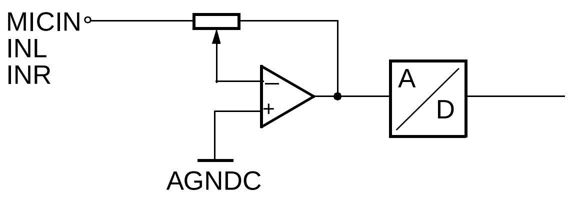


Fig. 4–14: Analog input pins MICIN, INL, INR

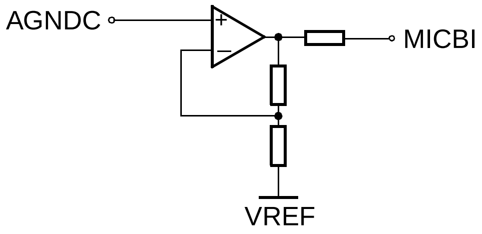


Fig. 4–15: Microphone bias pin (MICBI)

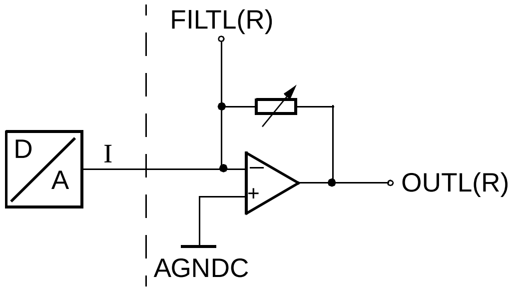


Fig. 4–16: Analog outputs OUTL(R) and connections for filter capacitors FILTL(R)

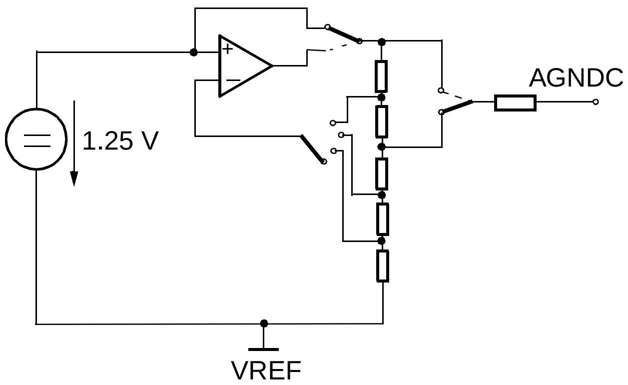


Fig. 4–17: Analog ground generation with pin to connect external capacitor

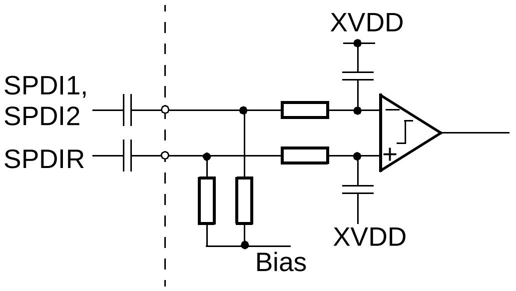


Fig. 4–18: S/PDIF inputs

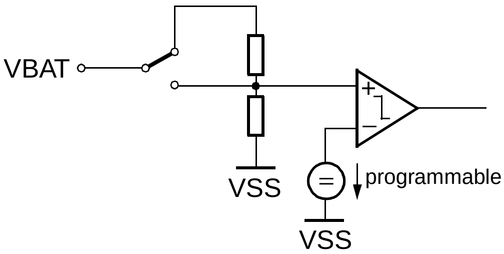


Fig. 4–19: Battery voltage monitor VBAT

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient operating temperature		–40	85	°C
T_S	Storage Temperature		–40	125	°C
P_{TOT}	Power dissipation	VDD, XVDD, AVDD0/1, I2CVDD		650	mW
V_{SUPA}	Analog supply voltages[1)]	AVDD0/1	–0.3	6	V
V_{SUP}	Digital supply voltage	VDD, XVDD, I2CVDD	–0.3	6	V
V_{Idig}	Input voltage, all digital inputs		–0.3	V_{SUP} +0.3	V
I_{Idig}	Input current, all digital inputs		–20	+20	mA
V_{Iana}	Input voltage, all analog inputs		–0.3	V_{SUP} + 0.3	V
I_{Iana}	Input current, all analog inputs		–5	+5	mA
I_{Oaudio}	Output current, audio output[2)]	OUTL/R	–0.2	0.2	A
I_{Odig}	Output current, all digital outputs[3)]		–50	+50	mA
I_{Odcdc1}	Output current DCDC converter 1	DCSO1		1.5	A
I_{Odcdc2}	Output current DCDC converter 2	DCSO2		1.5	A

1) Both AVDD0 and AVDD1 have to be connected together!
2) These pins are not short-circuit proof!
3) Total chip power dissipation must not exceed absolute maximum rating

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Temperature Range 1 and Supply Voltages						
T_{A1}	Ambient temperature range 1		–40		85	°C
V_{SUPD}	Digital supply voltage	VDD, XVDD	2.2	2.5	3.6	V
V_{SUPI2C}	I^2C bus supply voltage	I2CVDD	V_{SUPD} at VDD	2.5	3.6	V
V_{SUPA}	Analog audio supply voltage	AVDD0/1		**tbd**		V
V_{SUPA}	Analog audio supply voltage in relation to the digital supply voltage	AVDD0/1		**tbd**		
Temperature Range 2 and Supply Voltages						
T_{A2}	Ambient temperature range 2		0		85	°C
V_{SUPD}	Digital supply voltage	VDD, XVDD	2.2	2.5	3.6	V
V_{SUPI2C}	I^2C bus supply voltage	I2CVDD	V_{SUPD} at VDD	2.5	3.6	V
V_{SUPA}	Analog audio supply voltage	AVDD0/1	2.2	2.7	3.6	V
V_{SUPA}	Analog audio supply voltage in relation to the digital supply voltage	AVDD0/1	0.62 of V_{SUPD}		1.6 of V_{SUPD}	

Table 4–1: Reference Frequency Generation and Crystal Recommendation

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
External Clock Input Recommendations						
f_{CLK}	Clock frequency	XTI, XTO	13.00	18.432	20.00	MHz
V_{DCCLK}	DC voltage at oscillator pins			$0.5 \times V_{SUPA}$		V
V_{ACLK}	Clock amplitude [1)]		0.5		$V_{SUPA} - 0.5$	V_{pp}
	Transconductance [1)]		3.3			mA/V
[1)] Detailed information(diagrams) are still under investigation						

Table 4–1: Reference Frequency Generation and Crystal Recommendation

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Crystal Recommendation						
f_P	Load resonance frequency at C_l = 20 pF	XTI, XTO		18.432		MHz
$\Delta f/f_S$	Accuracy of frequency adjustment		–50		50	ppm
$\Delta f/f_S$	Frequency variation vs. temperature		–50		50	ppm
R_{EQ}	Equivalent series resistance			12	30	Ω
C_0	Shunt (parallel) capacitance			3	5	pF

Table 4–2: Input Levels

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
I_{IL}	Input low voltage at V_{SUPI2C} = 2.2 V	I2CC, I2CD			0.3	V
I_{IH}	Input high voltage at V_{SUPI2C} = 2.2 V		1.4			V
I_{IL}	Input low voltage at V_{SUPD} = 2.2 V	$\overline{\text{POR}}$, DCEN			0.2	V
I_{IH}	Input high voltage at V_{SUPD} = 2.2 V		0.9			V
I_{ILD}	Input low voltage	PI<I>, SI(B)I, SI(B)C, $\overline{\text{SI(B)D}}$, PR, $\overline{\text{PCS}}$, TE, DVS			0.3	V
I_{IHD}	Input high voltage		V_{SUP} –0.5			V

Table 4–3: Analog Input and Output Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Analog Reference						
C_{AGNDC1}	Analog filter capacitor	AGNDC	1.0	3.3		µF
C_{AGNDC2}	Ceramic capacitor in parallel			10		nF
C_{PVDD}	Capacitor for analog circuitry	PVDD	3			nF

Table 4–3: Analog Input and Output Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Analog Audio Inputs						
C_{inAD}	DC-decoupling capacitor at A/D-converter inputs	INL/R		390		nF
C_{inMI}	DC-decoupling capacitor at microphone-input	MICIN		100		nF
Analog Audio Filter Outputs						
C_{FILT}	Filter capacitor for headphone amplifier high-Q type, NP0 or C0G material	FILTL/R OUTL/R	–20 %	470	+20 %	pF
Analog Audio Output						
Z_{AOL_HP}	Analog output load with stereo headphones	OUTL/R	16			Ω
				100		pF

Table 4–3: Analog Input and Output Recommendations

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
DC/DC-Converter External Circuitry (please refer to application example)						
C_1	VSENS blocking (<100 mΩ ESR)	VSENS1/2		330		µF
V_{TH}	Schottky diode threshold voltage	DCSO1/2 VSENS1/2			0.35	V
L	Ferrite ring core coil inductance	DCSO1/2		22		µH
S/PDIF Interface Analog Input						
C_{SPI}	S/PDIF coupling capacitor	SPDI1/2 SPDIR		100		nF

4.6.3. Digital Characteristics

at $T_A = T_{A2}$, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Supply Voltage							
I_{SUPD}	Current consumption	VDD, XVDD, I2CVDD		35		mA	2.2 V, sampling frequency ≥ 32 kHz
I_{SUPD}	Current consumption			18		mA	2.2 V, sampling frequency ≤ 24 kHz
I_{SUPD}	Current consumption			10		mA	2.2 V, sampling frequency ≤ 12 kHz
Digital Outputs and Inputs							
O_{DigL}	Output low voltage	PI<I>, SOI, SOC, $\overline{SOD}$, $\overline{EOD}$, $\overline{PRTR}$, PRTW, CLKO, SYNC, PUP, SPDO			0.3	V	I_{load} = 2 mA
O_{DigH}	Output low voltage		V_{SUPD} –0.3			V	I_{load} = –2 mA
Z_{DigI}	Input impedance	ALL DIGITAL INPUTS			7	pF	
I_{DLeak}	Digital input leakage current		–1		1	µA	0 V < V_{pin} < V_{SUPD}
$I_{STANDBY}$	Total current at stand-by				10	µA	DSP off, Codec off, DC/DC off, AD and DAC off, no I^2C access

4.6.3.1. I^2C Characteristics

at T_A=25°C, V_{SUPI2C} = 2.2...3.6 V

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
I^2C Input Specifications							
f_{I2C}	Upper limit I^2C bus frequency operation	I2CC	400			kHz	
t_{I2C1}	I^2C START condition setup time	I2CC, I2CD	300			ns	
t_{I2C2}	I^2C STOP condition setup time	I2CC, I2CD	300			ns	
t_{I2C3}	I^2C clock low pulse time	I2CC	1250			ns	
t_{I2C4}	I^2C clock high pulse time	I2CC	1250			ns	
t_{I2C5}	I^2C data setup time before rising edge of clock	I2CC	80			ns	
t_{I2C6}	I^2C data hold time after falling edge of clock	I2CC	80			ns	
V_{I2COL}	I^2C output low voltage	I2CC, I2CD			0.4	V	I_{load} = 3 mA
I_{I2COH}	I^2C output high leakage current	I2CC, I2CD			1	µA	
t_{I2COL1}	I^2C data output hold time after falling edge of clock	I2CC, I2CD	20			ns	
t_{I2COL2}	I^2C data output setup time before rising edge of clock	I2CC, I2CD	250			ns	f_{I2C} = 400 kHz
V_{I2CIL}	I^2C input low voltage	I2CC; I2CD			0.3	V	
V_{I2CIH}	I^2C input high voltage	I2CC, I2CD	0.6			V_{SUPI2C}	

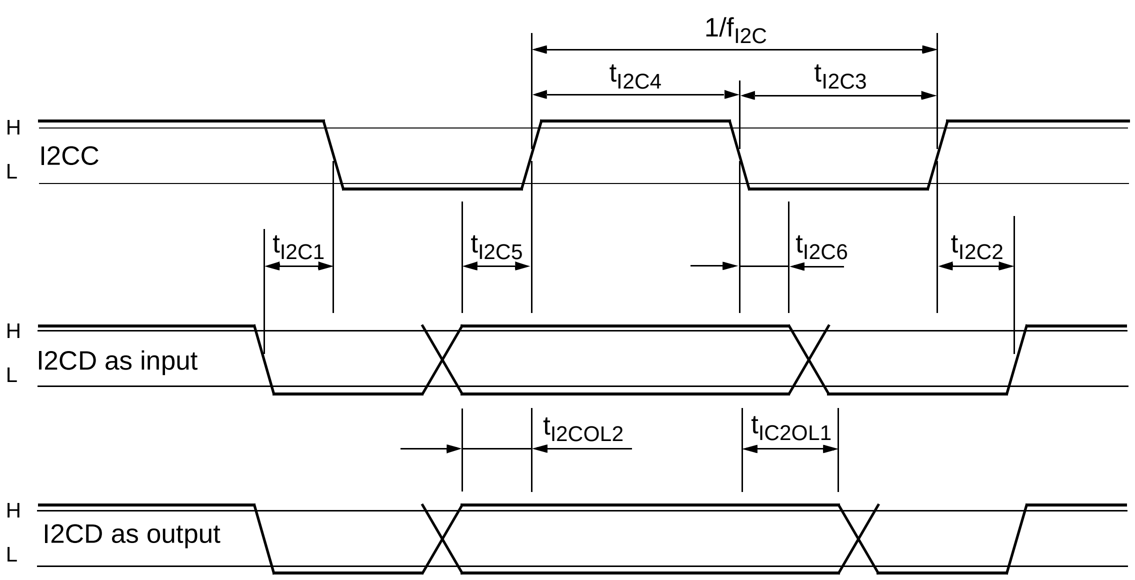


Fig. 4–20: I^2C timing diagram

4.6.3.2. Serial (I^2S) Input Interface Characteristics (SDI, SDIB)

at $T_A = T_{A2}$, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SICLK}	I^2S clock input clock period	SI(B)C	f_C			ns	demand mode (see Table 4–4)
t_{SIDS}	I^2S data setup time before falling edge of clock	SI(B)C, SI(B)D	50		t_{SICLK} –100	ns	
t_{SIDH}	I^2S data hold time	SI(B)D	50			ns	
t_{SIIS}	I^2S ident setup time before falling edge of clock	SI(B)C, SI(B)I	50		t_{SICLK} –100	ns	
t_{SIIH}	I^2S ident hold time	SI(B)I	50			ns	
t_{bw}	Burst wait time	SI(B)C, SI(B)D	480				

Table 4–4: Maximum demand clock frequency

f_{Sample} (kHz)	f_C (MHz)
48, 32	6.144
44.1	5.6448
24, 16	3.072
22.05	2.8224
12, 8	1.536
11.025	1.4112

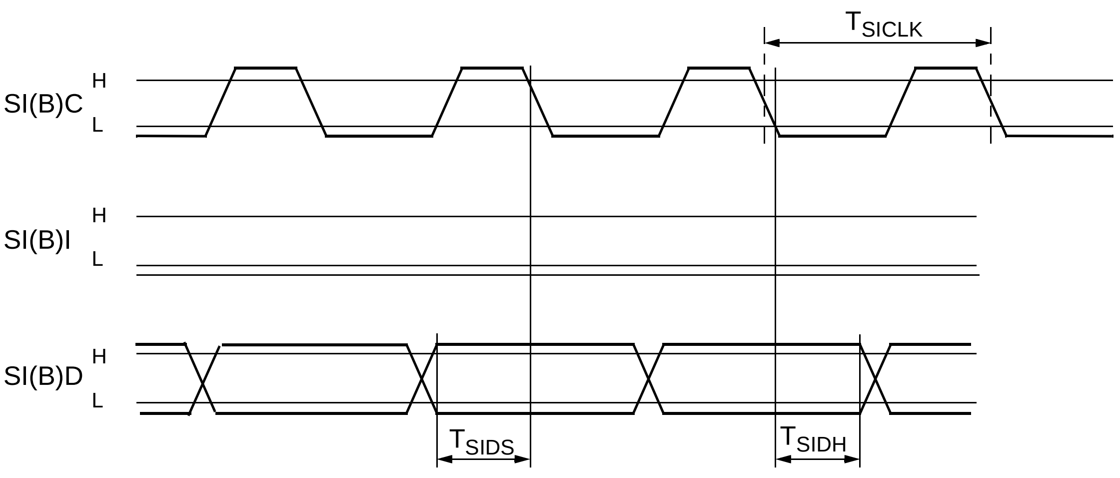


Fig. 4–21: Continuous data stream at serial input A or B. In this mode, the word strobe SI(B)I is not used and the data are read at the falling edge of the clock (bit 2 in D0:346 is set).

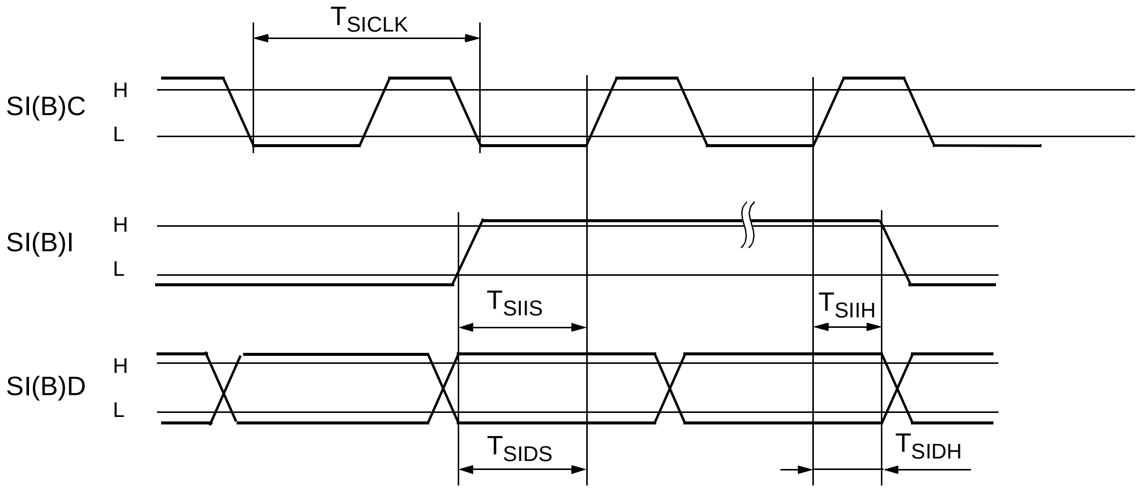


Fig. 4–22: Serial input of I^2S signal

4.6.3.3. Serial Output Interface Characteristics (SDO)

at $T_A = T_{A2}$, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
t_{SOCLK}	I^2S clock output frequency	SOC		325		ns	f_S=48 kHz Stereo 32 bits per sample
t_{SOISS}	I^2S word strobe delay time after falling edge of clock	SOC, SOI	0		t_{SOCLK} /4	ns	C_{load} = t.b.d. R_{load} = t.b.d.
t_{SOODC}	I^2S data delay time after falling edge of clock	SOC, SOD	0		t_{SOCLK} /4	ns	C_{load} = t.b.d. R_{load} = t.b.d.

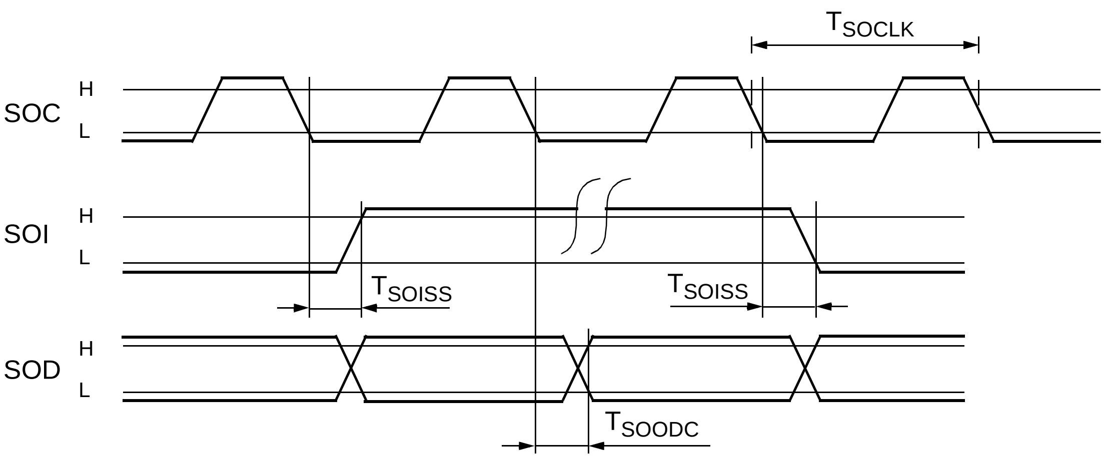


Fig. 4–23: Serial output interface timing.

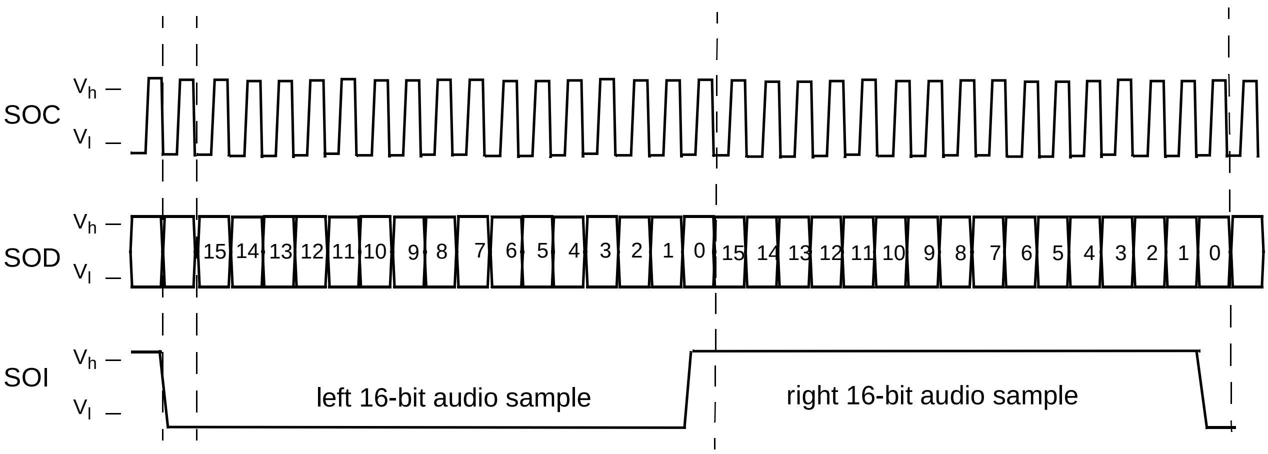


Fig. 4–24: Sample timing of the SDO interface in 16 bit/sample mode. D0:346 settings are: Bit 14 = 0 (SOC not inverted), bit 11 = 1 (SOI delay), bit 5 = 0 (word strobe not inverted), bit 4 = 1 (16 bits/sample).

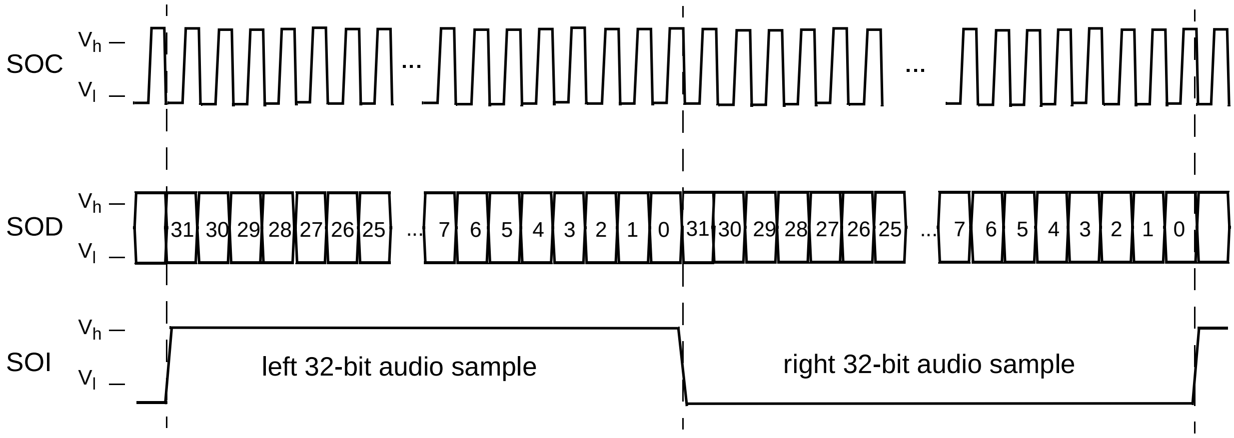


Fig. 4–25: Sample timing of the SDO interface in 32 bit/sample mode. D0:346 settings are: Bit 14 = 0 (SOC not inverted), bit 11 = 0 (no SOI delay), bit 5 = 1 (word strobe inverted), bit 4 = 0 (32 bits/sample).

4.6.3.4. S/PDIF Input Characteristics

at $T_A = T_{A2}$, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_S	Signal amplitude	SPDI1, SPDI2, SPDIR	200	500	1000	mV_{pp}	
f_{s1}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		2.048		MHz	±1000 ppm, f_S = 48 kHz
f_{s2}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		2.822		MHz	±1000 ppm, f_S = 44.1 kHz
f_{s3}	Bi-phase frequency	SPDI1, SPDI2, SPDIR		3.072		MHz	±1000 ppm, f_S = 32 kHz
t_P	Bi-phase period	SPDI1, SPDI2, SPDIR		326		ns	at f_S = 48 kHz, (highest sampling rate)
t_R	Rise time	SPDI1, SPDI2, SPDIR	0		65	ns	at f_S = 48 kHz, (highest sampling rate)
t_F	Fall time	SPDI1, SPDI2, SPDIR	0		65	ns	at f_S = 48 kHz, (highest sampling rate)
	Duty cycle	SPDI	40	50	60	%	at bit value=1 and f_S = 48 kHz
$t_{H1,L1}$		SPDI	81		163	ns	minimum/maximum pulse duration with a level above 90 % or below 10 % and at f_S = 48 kHz
$t_{H0,L0}$		SPDI	163		244	ns	minimum/maximum pulse duration with a level above 90 % or below 10 % and at f_S = 48 kHz

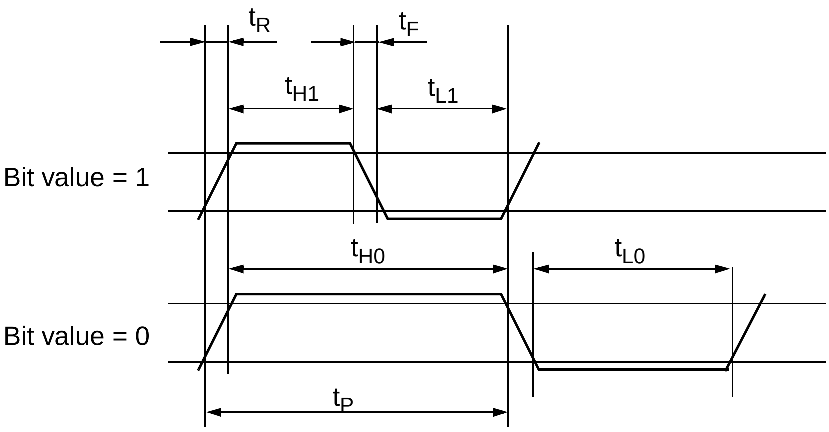


Fig. 4–26: Timing of the S/PDIF input

4.6.3.5. S/PDIF Output Characteristics

at $T_A = T_{A2}$, V_{SUPD}, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 18.432 MHz, Typ. values for T_A = 25 °C.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
f_{s1}	Bi-phase frequency	SPDO		3.072		MHz	f_s = 48 kHz
f_{s2}	Bi-phase frequency	SPDO		2.822		MHz	f_s = 44.1 kHz
f_{s3}	Bi-phase frequency	SPDO		2.048		MHz	f_s = 32 kHz
t_P	Bi-phase period	SPDO		326		ns	at f_s = 48 kHz, (highest sampling rate)
t_R	Rise time	SPDO	0		2	ns	C_{load} = 10 pF R_{load} = t.b.d.
t_F	Fall time	SPDO	0		2	ns	C_{load} = 10 pF R_{load} = t.b.d.
	Duty cycle	SPDO		50		%	
$t_{H1,L1}$		SPDO		163		ns	minimum/maximum pulse duration with a level above 90 % or below 10 % and at f_s = 48 kHz
$t_{H0,L0}$		SPDO		326		ns	minimum/maximum pulse duration with a level above 90 % or below 10 % and at f_s = 48 kHz
V_S	Signal amplitude	SPDO		V_{SUPD}			

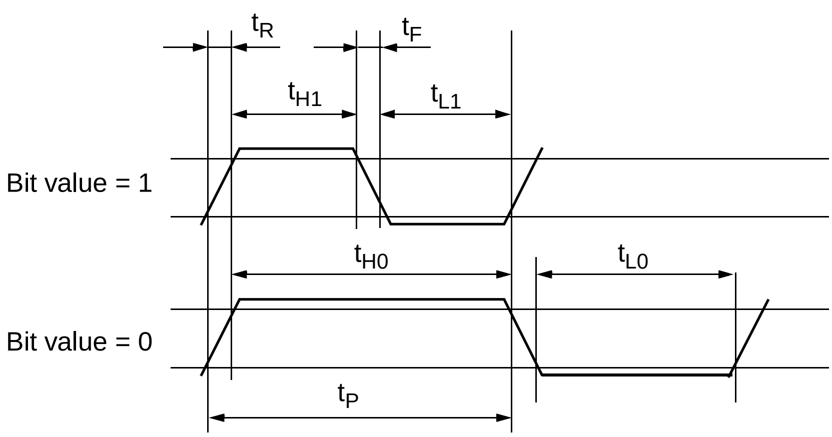


Fig. 4–27: Timing of the S/PDIF output

4.6.3.6. PIO As Parallel Input Interface: Demand Mode

The data transfer can be started after the $\overline{EOD}$ pin of the MAS 35x9F is set to “high”. After verifying this, the controller signalizes the sending of data by activating the PR line. The MAS 35x9F responds by setting the RTR line to the “low” level. The MAS 35x9F reads the data PI[19:12] at t_{pd} after rising edge of the PR signal. The next data word write operation will be initialized again by setting the PR line via the controller. Please refer to Figure 4–28 for the exact timing

The procedure above will be repeated until the MAS 35x9F sets the $\overline{EOD}$ signal to “0” which indicates that the transfer of one data block has been executed. Subsequently, the controller should set PR to “0”, wait until $\overline{EOD}$ rises again and then repeat the procedure to send the next block of data. The DMA buffer is 15 bytes long.

.

Symbol	Pin Name	Min.	Max.	Unit
t_{st}	PR, $\overline{EOD}$	0.010	2000	µs
t_r	PR, $\overline{RTR}$	40	160	ns
t_{pd}	PR, PI[19:12]	120	480	ns
t_{set}	PI[19:12]	160	no limit	ns
t_h	PI[19:12]	160	no limit	ns
t_{rtrq}	RTR	200	30000	ns
t_{pr}	PR	480	no limit	ns
t_{rpr}	PR, $\overline{RTR}$	160	no limit	ns
t_{eod}	PR, $\overline{EOD}$	40	160	ns
t_{eodq}	EOD	2.5	500	µs

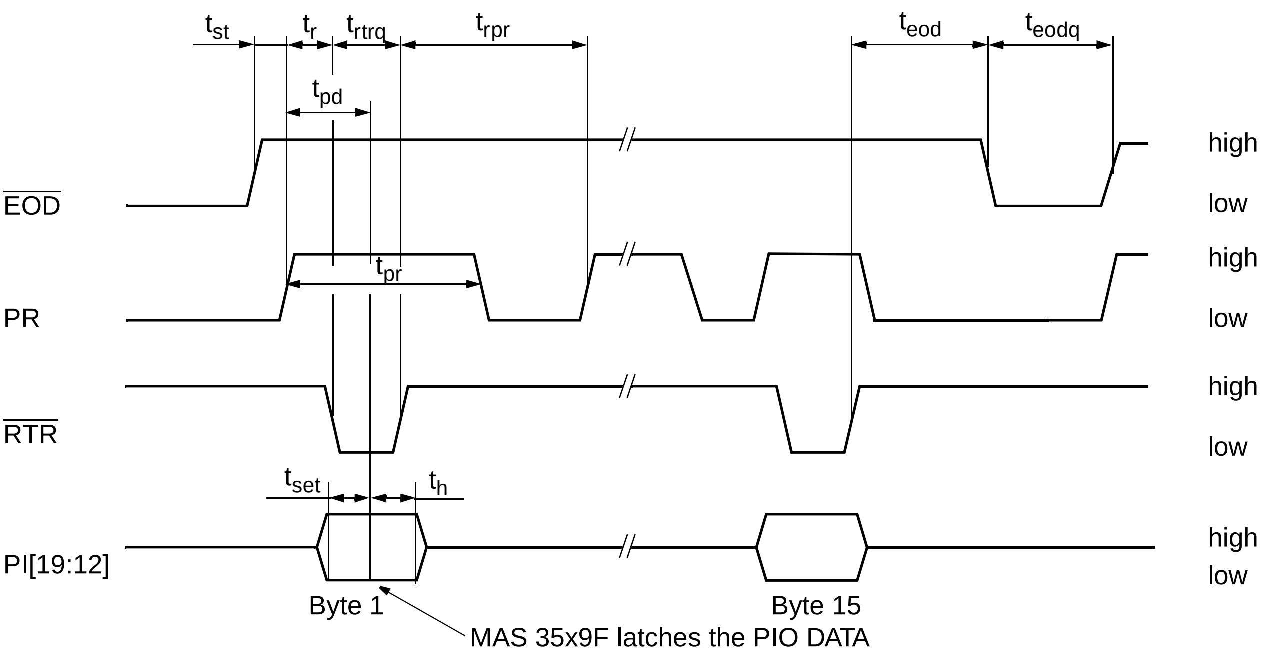


Fig. 4–28: Handshake protocol for writing MPEG data to the PIO-DMA

4.6.3.7. PIO as Parallel Output Interface

Some downloadable software may use the PIO interface (lines PI19...PI12) as output. The data transfer rate and conditions are defines by the software function.

Handshaking for PIO output mode is accomplished through the $\overline{\text{RTW}}$, $\overline{\text{PCS}}$, and PI12..PI19 signal lines (see Fig. 4–29). The PR line has to be set to high level.

$\overline{\text{RTW}}$ will go low as soon as a byte is available in the output buffer and will stay low until a byte has been read. Reading of a byte is performed with a $\overline{\text{PCS}}$ pulse. Data is latched out from the MAS on the falling edge of $\overline{\text{PCS}}$ and removed from the bus on the rising edge of $\overline{\text{PCS}}$.

Table 4–5: PIO output mode timing

Symbol	Pin	Min.	Max.	Unit
t_0	$\overline{\text{RTW}}$, $\overline{\text{PCS}}$	0.010	1800	µs
t_1	PCS	0.330		µs
t_2	$\overline{\text{PCS}}$, $\overline{\text{RTW}}$	0.010		µs
t_3	RTW	0.330	10000	µs
t_4	PI	0.330		µs
t_5	PI	0.081		µs

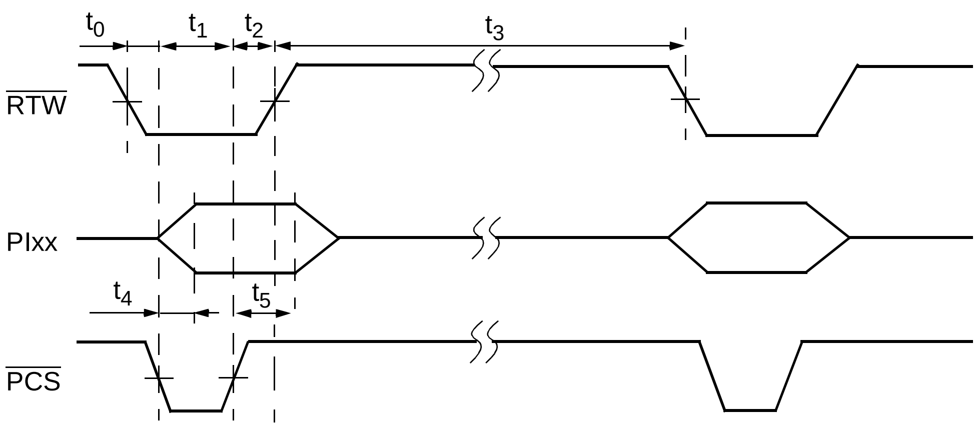


Fig. 4–29: Output Timing

4.6.4. Analog Characteristics

at $T_A = T_{A2}$, V_{SUPD} = 2.2...3.6 V, V_{SUPA} = 2.2 ... 3.6 V, $f_{Crystal}$ = 13...20 MHz,
typical values at T_A = 25 °C and $f_{CRYSTAL}$ = 18.432 MHz

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions	
Analog Supply								
I_{AVDD}	Current consumption analog audio	AVDD0/1		5		mA	V_{SUPA} = 2.2 V, Mute	
I_{QOSC}	Current consumption crystal oscillator	AVDD0/1		200		µA	Codec = off DSP = off DC/DC = on	
Analog Audio								
V_{AI}	Analog line input clipping level (at minimum analog input gain,i.e. –3 dB)	INL/R				V_{pp}	V_{SUPA}	Bits 15, 14 in Reg. $6A_{hex}$
				2.2			>2.2 V	00
				2.6			>2.4 V	01
				3.2			>3.0 V	10
V_{MI}	Microphone input clipping level (at minimum analog input gain, i.e. +21 dB)	MICIN				mV_{PP}	V_{SUPA}	Bits 15,14 in Reg. $6A_{hex}$
				141			>2.0 V	00
				167			>2.4 V	01
				282			>3.0 V	10
V_{AO1}	Analog Output Voltage AC	OUTL/R					$R_L \geq 1$ kΩ Input=0 dBFS digital V_{SUPA}	Bits 15, 14 in Reg $6A_{hex}$
	at 0 dB output gain			1.56		V_{pp}	>2.2 V	00
				1.84			>2.4 V	01
				2.26			>3.0 V	10
	at +3 dB output gain			2.20		V_{pp}	>2.2 V	00
				2.60			>2.6 V	01
				3.20			>3.2 V	10

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{AO2}		OUTL/R					R_L is 16 Ω Headphone and 22 Ω seriesresistor Input=0 dBFS digital (see Fig. 4–33 on page 81) V_{SUPA} Bits 15, 14 in Reg $6A_{hex}$
	at 0 dB output gain			1.56		V_{pp}	>2.2 V 00
				1.84			>2.4 V 01
				2.26			>3.0 V 10
	at +3 dB output gain			2.00		V_{pp}	>2.2 V 00
				2.40			>2.6 V 01
				3.00			>3.2 V 10
R_{inAI}	Analog line input resistance	INL/R		92		kΩ	at minimum analog input gain, i.e. –3 dB
				20			at maximum analog input gain, i.e. +19.5 dB
				67			not selected
R_{inMI}	Microphone input resistance	MICIN		94		kΩ	at minimum analog input gain, i.e. –21 dB
				8			at maximum analog input gain, i.e. +43.5 dB
				94			not selected
R_{inAO}	Analog output resistance	OUTL/R			6	Ω	analog gain=+3 dB, Input=0 dBFS digital
SNR_{AI}	Signal-to-noise ratio of line input	INL/R		61		dB	BW = 20 Hz...20 kHz, analog gain=0 dB, input 1 kHz at V_{AI}–20 dB
SNR_{MI}	Signal-to-noise ratio of microphone input	MICIN		61		dB	BW = 20 Hz...20 kHz, analog gain=+21 dB, input 1 kHz at V_{MI}–20 dB
THD_{AI}	Total harmonic distortion of analog inputs	INL/R MICIN			0.02	%	BW = 20 Hz...20 kHz, analog gain = 0 dB, input 1 kHz at –3 dBFS=V_{AI}–6 dB resp. V_{MI}-6 dB
$XTALK_{AI}$	Crosstalk attenuation left/right channel (analog inputs)	INL/R MICIN		80		dB	f = 1 kHz, sine wave, analog gain = 0 dB, input = –3 dBFS
$PSRR_{AI}$	Power supply rejection ratio for analog audio inputs	AVDD0/1, INL/R MICIN		50		dB	1 kHz sine at 100 mV_{rms}
				20		dB	≤100 kHz sine at 100 mV_{rms}

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Audio output							
SNR_{AO}	Signal-to-noise ratio of analog output	OUTL/R				dB	$R_L \geq 16\ \Omega$ (external 22 Ω series resistor required) BW=20 Hz...20kHz unweighted, analog gain=0 dB
				90		dB	input=–20 dBFS
				96			input=–40 dBFS
THD_{AO}	Total harmonic distortion (headphone)	OUTL/R					
	for $R_L \geq 16\Omega$ plus 22Ω series resistor (see Fig. 4–33 on page 81)				0.05	%	
	for $R_L \geq 1k\Omega$				0.01		
Lev_{MuteAO}	Mute level	OUTL/R		–110		dBV	BW=20 Hz...22kHz unweighted, no digital input signal, analog gain=mute
$XTALK_{AO}$	Crosstalk attenuation left/right channel (headphone)	OUTLR		80		dB	f=1 kHz, sine wave, OUTL/R: $R_L \geq 16\ \Omega$ (22 Ω series resistor required) (see Fig. 4–33 on page 81) analog gain=0 dB input=-3 dBFS
$PSRR_{AO}$	Power supply rejection ratio for analog audio outputs	AVDD0/1 OUTL/R		50		dB	1 kHz sine at 100 mV_{rms}
				20		dB	≤100 kHz sine at 100mV_{rms}
V_{AGNDC}	Analog Reference Voltage	AGNDC				V	R_L >> 10 MΩ, referred to VREF
							V_{SUPA} — Bits 15, 14 in in Reg. $6A_{hex}$
				1.1			>2.2 V — 00
				1.3			>2.4 V — 01
				1.6			>3.0 V — 10
V_{MICBI}	Bias voltage for microphone	MICBI					V_{SUPA} — Bits 15, 14 in in Reg. $6A_{hex}$
				1.8			>2.2 V — 00
				2.13			>2.4 V — 01
				2.62			>3.0 V — 10

4.6.5. DC/DC Converter Characteristics

at $T_A = T_{A2}$, V_{in} = 1.2 V (unless otherwise noted), V_{outn} = 3.0 V, f_{clk} = 18.432 MHz, f_{sw} = 384 kHz,
Typ. values for T_A = 25 °C

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IN}	Minimum start-up input voltage	*		0.9		V	$I_{LOAD} \leq$ 1 mA, DCCF = 5050_{hex} (reset)
V_{IN}	Minimum operating input voltage (*see Fig. 4–33 on page 81)						
	DC1* DC2*			0.7 0.8		V	I_{LOAD} = 50 mA, DCCF = 5050_{hex} (reset)
	DC1* DC2*			1.0 1.1		V	I_{LOAD} = 200 mA, DCCF = 5050_{hex} (reset)
V_{OUT}	Programmable output voltage range	VSENSn	2.0		3.5	V	Voltage settings in DCCF register (I^2C subaddress 76_{hex})
V_{OTOL}	Output voltage tolerance	VSENSn	2.9		3.1	V	I_{LOAD} = 20 mA T_A = 25 °C
I_{LOAD1}	Output current 1 battery cell	VSENSn			200	mA	V_{IN} = 0.9...1.5 V C_{OUT} = 330 µF
I_{LOAD2}	Output current 2 battery cells				600	mA	V_{IN} = 1.8...3.0 V C_{OUT} = 330 µF
$dV_{OUT}/dV_{IN}/V_{OUT}$	Line regulation	VSENSn		0.8		%/V	I_{LOAD} = 50 mA V_{IN} = 1.2 V
dV_{OUT}/V_{OUT}	Load regulation						
	DC1	VSENS1		–1.7		%	I_{LOAD} = 20...200 mA,
	DC2	VSENS2		–1.8			
h_{max}	Maximum efficiency	–			95	%	V_{IN} = 2.4 V, V_{OUT} = 3.5 V
f_{switch}	Switching frequency	DCSOn	297	384	t.b.d.	kHz	(see Table 2–1 on page 11)
$f_{startup}$	Switching frequency during start-up	DCSOn		250		kHz	VSENSEn < 1.9 V
$I_{supPFM1}$	Supply current in PFM mode	VSENS1		75		µA	1)
$I_{supPFM2}$		VSENS2		135			
$I_{supPWM1}$	Supply current in PWM mode	VSENS1		265		µA	VSENSn 1) 2)
$I_{supPWM2}$		VSENS2		325			
I_{lnmax}	NMOS switch current limit (low side switch)	DSCOn, DCSGn		1		A	
I_{lptoff}	PMOS switch turnoff current (rectifier switch)	DCSOn, VSENSn		70		mA	
I_{LEAK}	leakage current	DCSOn, DCSGn		0.1	**tbd**	µA	T_j = 25 °C, converter off, I_{LOAD} = 0 µA

1) Current into VSENSn. VIN > VOUT+ΔV; (ΔV≈0.4 V); no DC/DC-Converter regulation switching action present
2) Add. current of oscillator at PIN AVDD0/1, (see Section 4.6.4. on page 74)

4.6.6. Typical Performance Characteristics

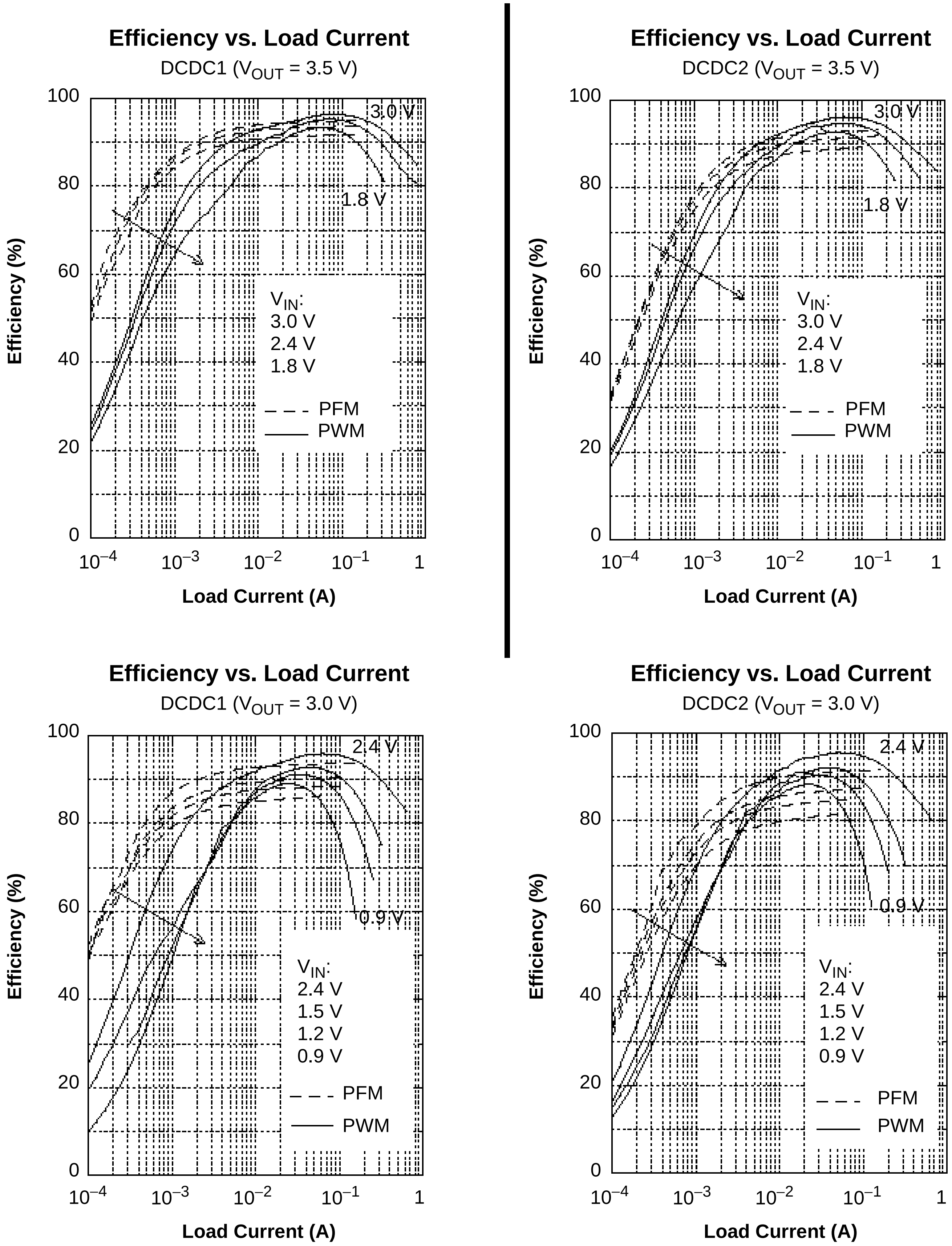
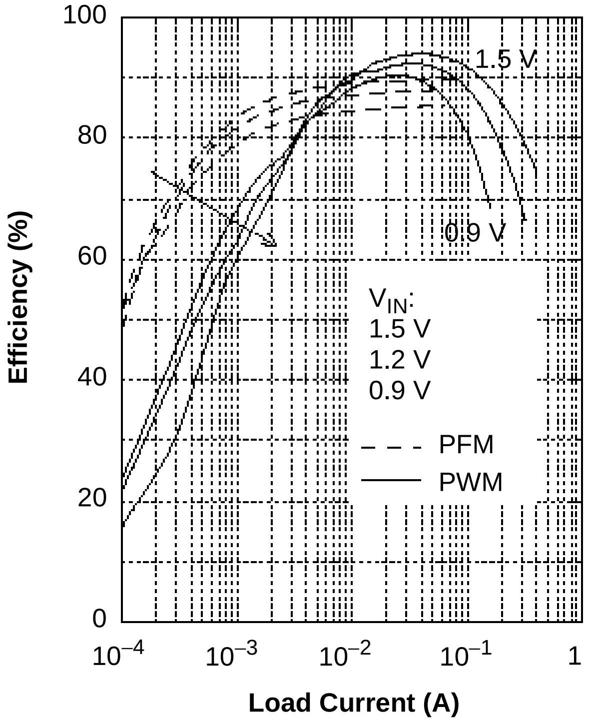


Fig. 4–30: Efficiency vs. Load Current

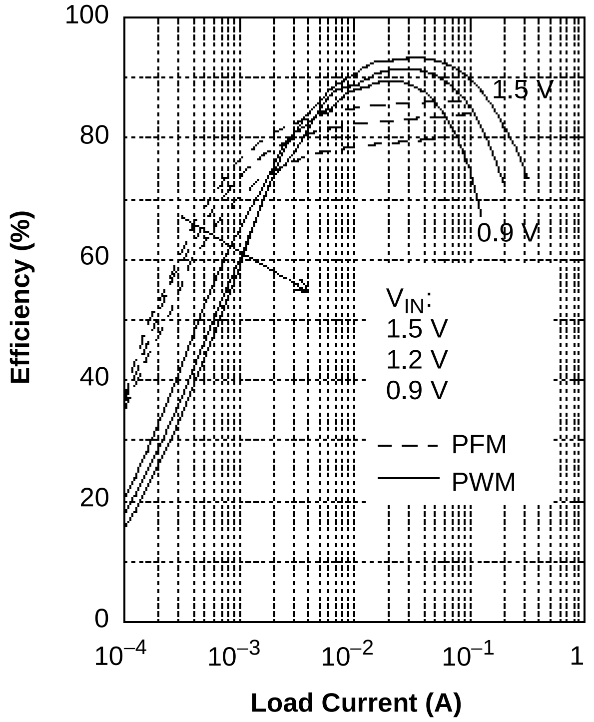
Efficiency vs. Load Current

DCDC1 (V_{OUT} = 2.2 V)

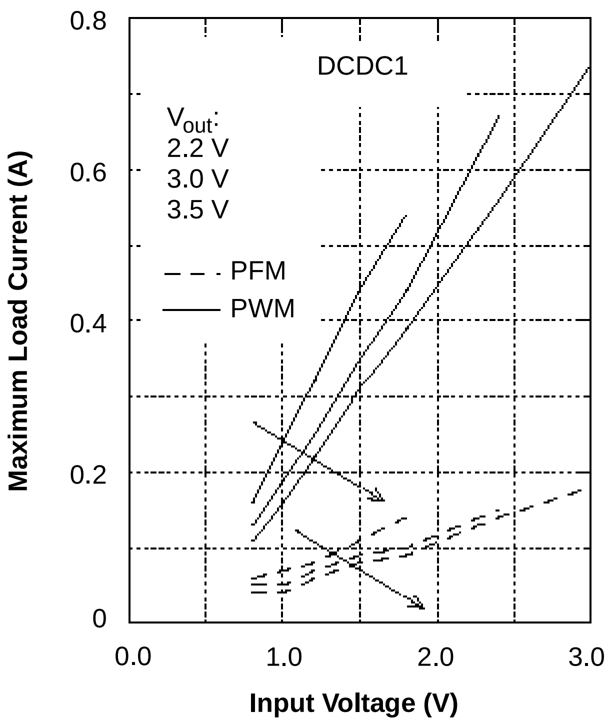


Efficiency vs. Load Current

DCDC2 (V_{OUT} = 2.2 V)



Maximum Load Current vs. Input Voltage



Maximum Load Current vs. Input Voltage

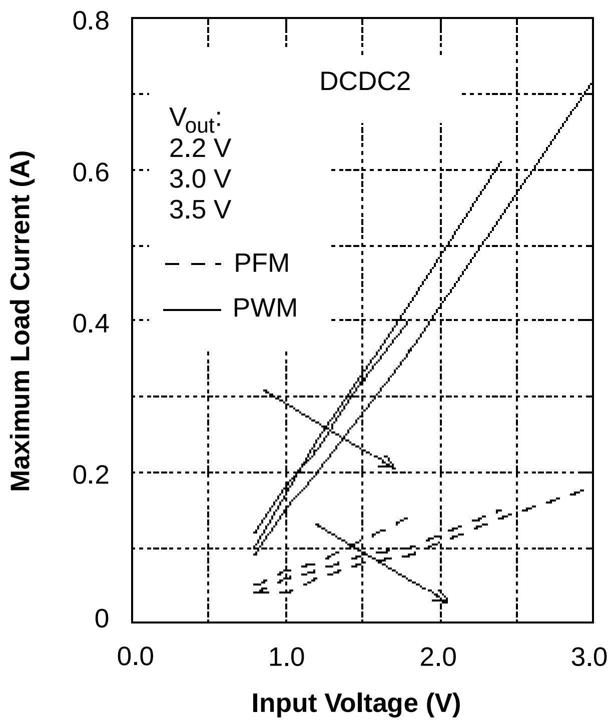


Fig. 4–31: Maximum Load Current vs. Input Voltage

Note: Efficiency is measured as $V_{SENSn} \times I_{LOAD} / (V_{in} \times I_{in})$.
I_{AVDD} is not included (Oscillator current)

4.7. Typical Application in a Portable Player

– MMC/SDI-Card or SMC/CF2+ used as storage media
– Dashed lines show optional (external) devices

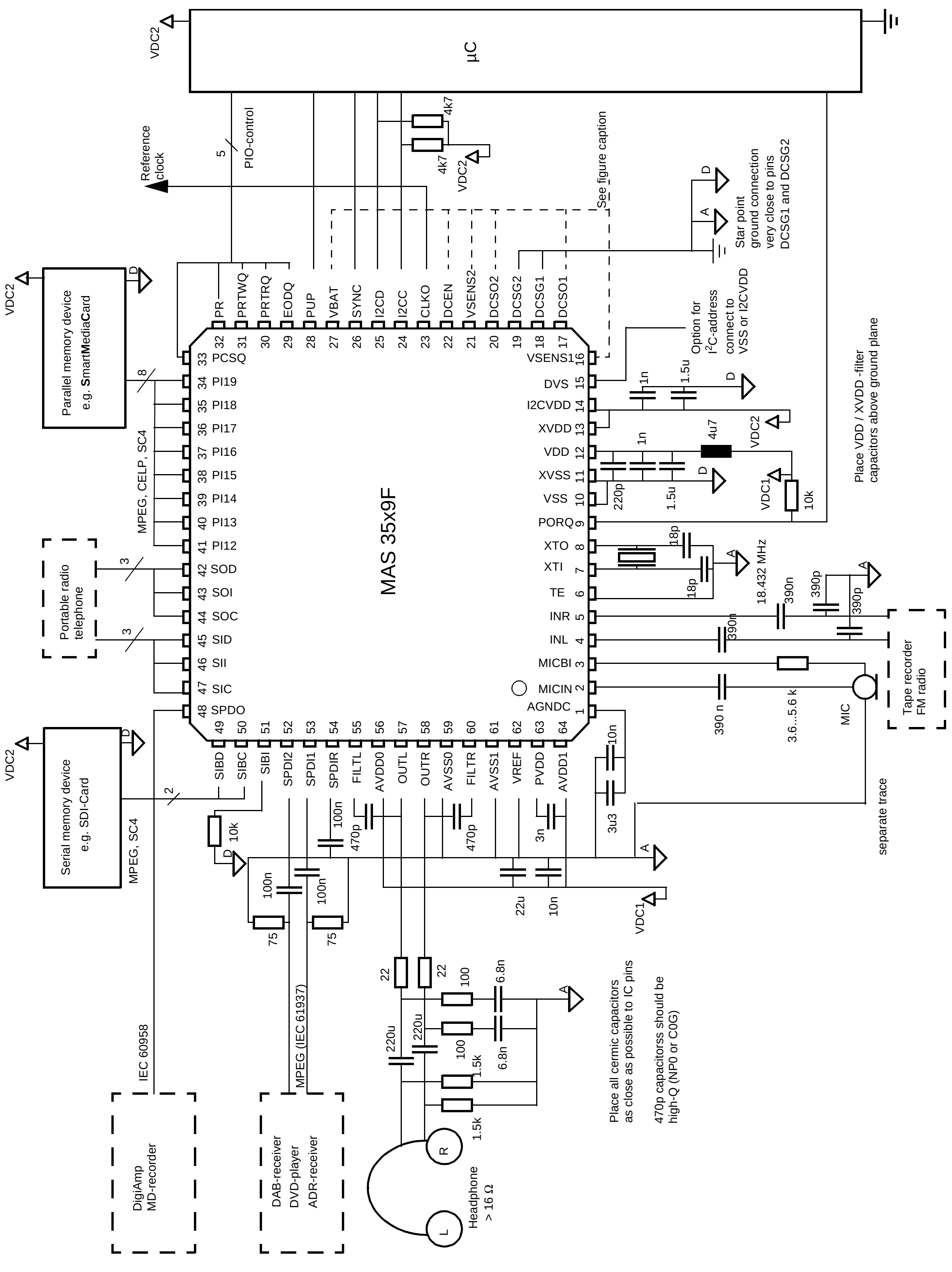


Fig. 4–32: Application circuit of the MAS 35x9F. For connections of the DC/DC converters, please refer to Fig. 4–33.

4.8. Recommended DC/DC Converter Application Circuit

(Power optimized szenario, (see Fig. 2–5 on page 13))

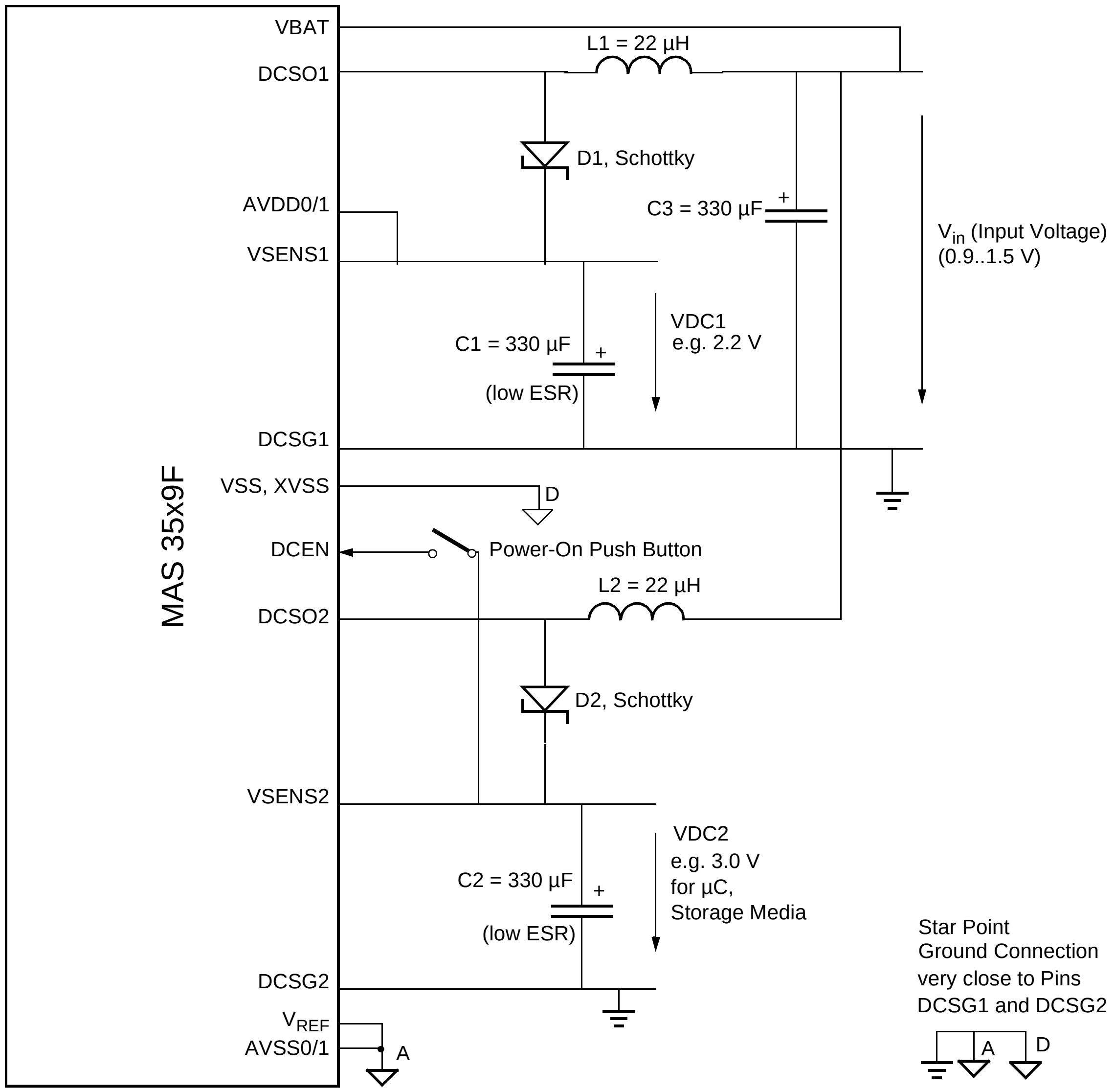


Fig. 4–33: External circuitry for the DC/DC converters

5. Data Sheet History

1. Advance Information: “MAS 3509F, MPEG Layer 2/ 3, AAC Audio Decoder, G.729 Annex A Codec”, August 04, 2000, 6251-505-1AI. First release of the advance information.

2. Advance Information: “MAS 35x9F, MPEG Layer 2/ 3, AAC Audio Decoder, G.729 Annex A Codec”, October 31, 20000, 6251-505-2AI. Second release of the advance information.
Major changes:
This data sheet applies to MAS 3509F version A2 .

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Printed in Germany
Order No. 6251-505-2AI