PRELIMINARY DATA SHEET

SDA 5650/X
VPS/PDC-Plus Decoder

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MICRONAS

SDA 5650/X **Revision History:**		**Current Version: 02.97**
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Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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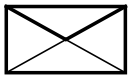

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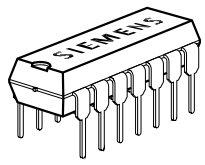
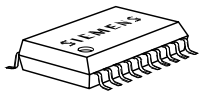
CMOS

1 General Description

The PDC plus SDA 5650 decoder chip receives all VPS and 8/30 Format 1 and 2 data together with the teletext header information for easy identification of broadcast transmitter. The SDA 5650 includes a storage capacity of 16 bytes which can be used in different ways depending on selected modes.



P-DIP-14-1



P-DSO-20-1 /-6 /-7

1.1 Features

- **Single chip receiver for PDC data for Broadcast Data Service Packet (BDSP 8/30/2)**
  according to CCIR teletext system B.
  VPS Data in dedicated line no. 16 of the vertical blanking interval (VBI)
- **Reception of BDSP packet 8/30/1**
  Unified Date and Time (UDT)
  Network indentification code (NIC)
  Short program label (SPL)
- **Reception of teletext header row**
  Bytes no. 14 - 45 containing date, clock time and identification
- **On chip data slicer**
- **Low external component count**
- **I^2C-Bus interface**
  Communication with external microcontroller
- **PDC/VPS operation mode selectable via I^2C-Bus register**
- **Pin and software compatible to PDC/VPS decoder SDA 5649**
- **5 V supply voltage**
- **Video input signal level: 0.7 Vpp to 2.0 Vpp**
- **Technology: CMOS**
- **P-DIP-14-1 and P-DSO-20-1 package**

Type	Ordering Code	Package
SDA 5650	Q67100-H5164	P-DIP-14-1
SDA 5650X	Q67106-H5163	P-DSO-20-1 (SMD)

1.2 Pin Configurations

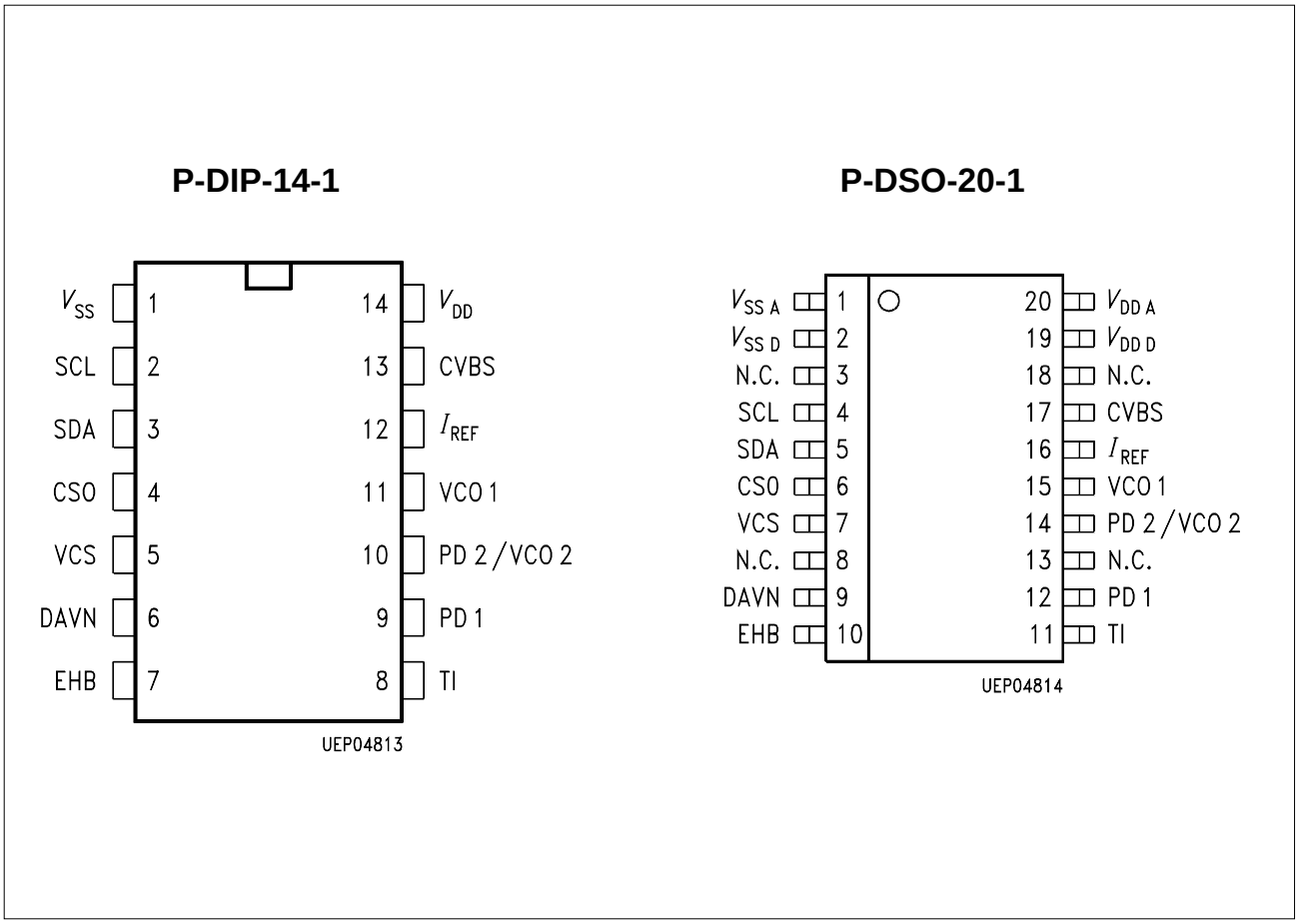


Figure 1

1.3 Pin Description

Pin No.		Symbol	Function
P-DIP-14-1	P-DSO-20-1		
1		V_{SS}	Ground (0 V)
	1	V_{SSA}	Analog ground (0 V)
	2	V_{SSD}	Digital ground (0 V)
	3, 8, 13, 18	N.C.	Not connected
2	4	SCL	Serial clock input of I^2C Bus.
3	5	SDA	Serial data input of I^2C Bus.
4	6	CS0	Chip select input determining the I^2C-Bus addresses: 20_H / 21_H, when pulled low 22_H / 23_H, when pulled high.
5	7	VCS	Video Composite Sync output from sync slicer used for PLL based clock generation.
6	9	DAVN	Data available output active low, when VPS data is received.
7	10	EHB	Output signaling the presence of the first field active high.
8	11	TI	Test input; activates test mode when pulled high. Connect to ground for operating mode.
9	12	PD1	Phase detector/charge pump output of data PLL (DAPLL).
10	14	PD2/ VCO2	Connector of the loop filter for the SYSPLL.
11	15	VCO1	Input to the voltage controlled oscillator #1 of the DAPLL.
12	16	I_{REF}	Reference current input for the on-chip analog circuit.
13	17	CVBS	Composite video signal input.
14		V_{DD}	Positive supply voltage (+ 5 V nom.).
	19	V_{DDD}	Positive supply voltage for the digital circuits (+ 5 V nom.).
	20	V_{DDA}	Positive supply voltage for the analog circuits (+ 5 V nom.).

Block Diagram

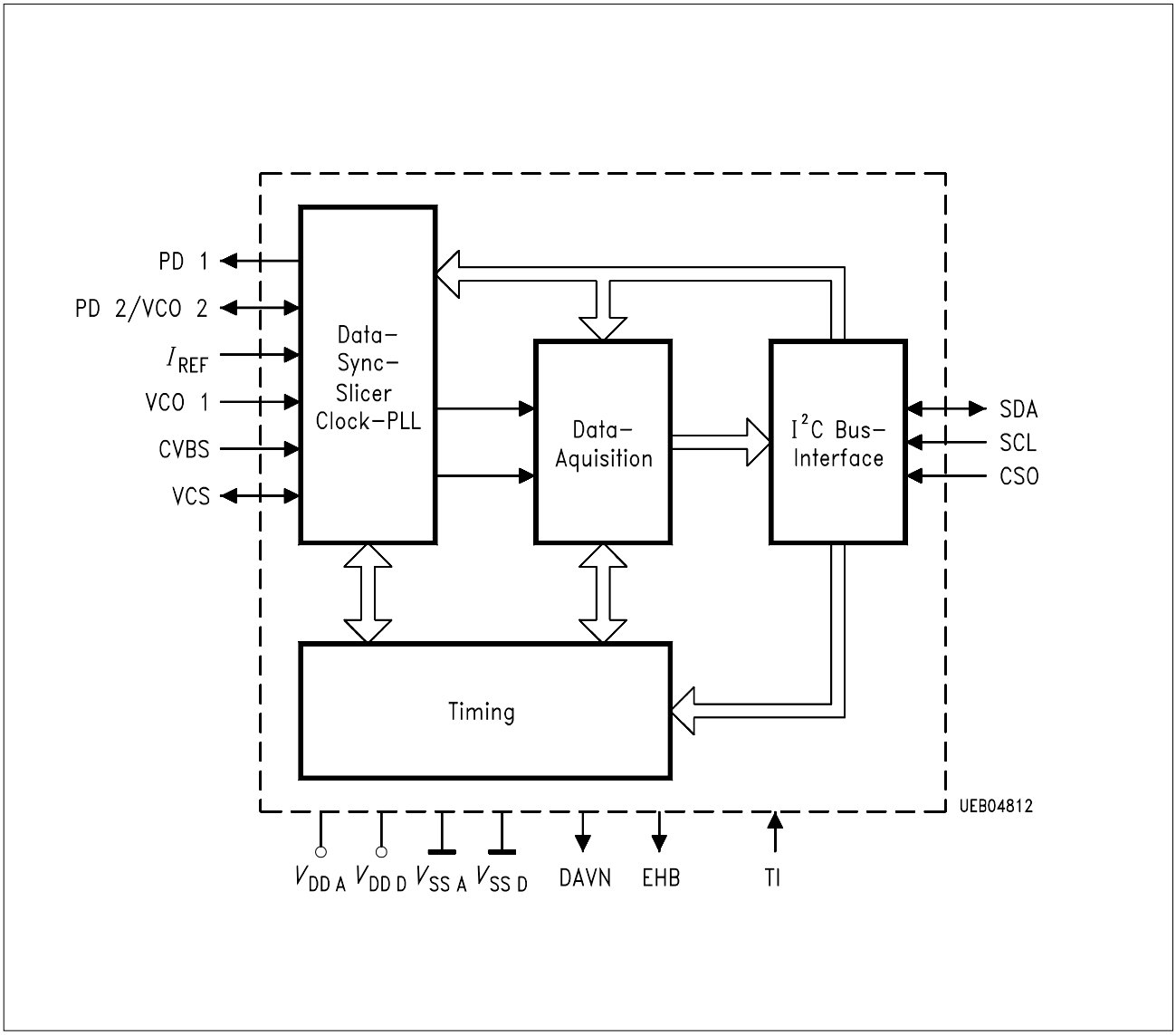


Figure 2

2 System Description

2.1 Functions

Referring to the functional block diagram of the PDC / VPS decoder, the composite video signal with negative going sync pulses is coupled to the pin CVBS through a capacitor which is used for clamping the bottom of the sync pulses to an internally fixed level. The signal is passed on to the slicer, an analogue circuitry separating the sync and the data parts of the CVBS signal, thus yielding the digital composite sync signal VCS and a digital data signal for further processing by comparing those signals to internally generated slicing levels.

The output of the sync separator is forwarded, on one hand, to the output pin VCS, and on the other hand, to the clock generator and the timing block. The VCS signal represents a key signal that is used for deriving a system clock signal by means of a PLL and all other timing signal.

The data slicer separates the data signal from the CVBS signal by comparing the video voltage to an internally generated slicing level which is found by averaging the data signal during TV line no. 16 in the VPS mode or by averaging the data signal during the clock run-in period of the teletext lines during the data entry window (DEW) in PDC mode.

The clock generator delivers the system clock needed for the basic timing as well as for the regeneraton of the dataclock. It is based on two phase locked loops (PLL's) all parts of which are integrated on chip with the exception of the loop filter components. Each of the PLL's is composed of a voltage controlled relaxation oscillator (VCO), a phase/ frequency detector (PFD), and a charge pump which converts the digital output signals of the PFD to an analogue current. That current is transformed to a control voltage for the VCO by the off-chip loop filter. The generated VCO frequencies are 10 MHz and 13.875 MHz for VPS mode and PDC mode, respectively.

All signals necessary for the control of sync and data slicing as well as for the data acquisition are generated by the Timing block.

The SDA 5650 can be operated in three different modes: Depending on the selected operating mode, either teletext lines carrying 8/30 packages, the dedicated TV line no. 16 (VPS) or the teletext header bytes 38-45, 30-37, 22-29 and 14-21 are acquired.

In PDC mode, only teletext rows 8/30 containing Broadcast Data Service Package (BDSP) information are acquired. The relevant bytes of 8/30 format 1 (8/30/1) and 8/30 format 2 (8/30/2) are extracted. The 8/30/1-bytes are stored in the acquisition register in a transparent way without any bit manipulation, whereas the Hamming coded bytes of packet 8/30/2 are Hamming-checked and bytes with one bit error are corrected. The storage of error free or corrected 8/30/2-data bytes in the transfer register to the I^2C Bus is signalled by the DAVN output going low.

In VPS mode, the extracted data bits of TV line no. 16 are checked for biphase errors. With no biphase errors encountered, the acquired bytes are stored in the transfer register to the I²C Bus. That transfer is signalled by a H/L transition of the DAVN output, as well.

In TTX header mode A bytes 38-45 and 30-37 are accessed in this order. This assures software compatibility to the SDA 5649. In mode B bytes 22-29 and 14-21 are accessed in this order.

In all three operating modes data are updated when a new data line has been received, provided that the chip is not accessed via the I²C Bus at the same time.

A micro controller can read the stored bytes via the I²C-Bus interface at any time. However, one must be aware that the storage of new data from the acquisition interface is inhibited as long as the PDC decoder is being accessed via the I²C Bus.

Note: In order to achieve maximum system performance it is recommended to start the SDA 5650 in VPS mode (state after power on) and read the register to check whether line 16 is received. After reception of VPS data inline 16 the SDA 5650 can be switched to 8/30 mode and waiting for packet 8/30 data. Since VPS data in line 16 is transmitted every frame and PDC data in packet 8/30 is transmitted nearly every second the recognition of both VPS and 8/30 packets can be done within PDC-system constraints (about 1 sec).

2.2 I²C Bus

2.2.1 General Information

The I²C-Bus interface implemented on the PDC decoder is a slave transmitter/receiver, i. e., both reading from and writing to the PDC / VPS decoder is possible. The clock line SCL is controlled only by the bus master usually being a micro controller, whereas the SDA line is controlled either by the master or by the slave. A data transfer can only be initiated by the bus master when the bus is free, i. e., both SDA and SCL lines are in a high state. As a general rule for the I²C Bus, the SDA line changes state only when the SCL line is low. The only exception to that rule are the Start Condition and the Stop Condition. Further Details are given below. The following abbreviations are used:

START:	Start Condition generated by master
AS:	Acknowledge by slave
AM:	Acknowledge by master
NAM:	No Acknowledge by master
STOP:	Stop condition generated by master

2.2.2 Chip Address

There are two pairs of chip addresses, which are selected by the CS0-input pin according to the following table:

CS0 Input	Write Mode	Read Mode
Low	20 (hex)	21 (hex)
High	22 (hex)	23 (hex)

2.2.3 Write Mode

For writing to the PDC decoder, the following format has to be used:

Start	Chipaddress and Write Mode	AS	Byte to set Control Register	AS	Stop

Description of Data Transfer (Write Mode)

Step1: In order to start a data transfer the master generates a Start Condition on the bus by pulling the SDA line low while the SCL line is held high.

Step 2: The bus master puts the chip address on the SDA line during the next eight SCL pulses.

Step 3: The master releases the SDA line during the ninth clock pulse. Thus the slave can generate an acknowledge (AS) by pulling the SDA line to a low level.

Step 4: The controller transmits the data byte to set the Control register

Step 5: The slave acknowledges the reception of the byte.

Step 6: The master concludes the data communication by generating a Stop Condition.

The write mode is used to set the I^2C-Bus control register which determines the operating mode:

Control Register:

Bit Number:	7	6	5	4	3	2	1	0
	T4	T3	T2	T1	MAB	HDT	PDC/ $\overline{\text{VPS}}$	FOR1/ $\overline{\text{FOR2}}$

Default: All bits are set to 0 on power-up.

Bits 4 through 7 are used for test purposes and must not be changed for normal operation by user software!

Bit 0: determines, which kind of data is accessed via the I^2C Bus when PDC mode is active:

Value	
0	1
BDSP 8/ 30/ 2 data accessible	BDSP 8/ 30/ 1 or header row data accessible (refer to description of Bit 2)

Bit 1: determines the operating mode:

Value	
0	1
VPS mode active	PDC mode active

Bit 2: determines whether BDSP 8/30/1-data or header row data is accessible:

Value	
0	1
BDSP 8/30/1 data accessible	Bytes of teletext header in mode A or B (see Bit 3)

Bit 3: determines mode of teletext header access:

Value	
0	1
Mode A: header bytes in order 38-45, 30-37	Mode B: header bytes in order 22-29, 14-21

2.2.4 Read Mode

For reading from the PDC decoder, the following format has to be used

Start	Chipaddress Read Mode	AS	1st Byte	AM	.....	Last Byte	NAM	Stop

The contents of up to 16 registers (bytes) can be read starting with byte 1 bit 7 (refer to the table **Order of Data Output on the I²C Bus and...**) depending on the selected operating mode.

Description of Data Transfer (Read Mode)

Step1: To start a data transfer the master generates a Start Condition on the bus by pulling the SDA line low while the SCL line is held high. The byte address counter in the decoder is reset and points to the first byte to be output.

Step 2: The bus master puts the chip address on the SDA line during the next eight SCL pulses.

Step 3: The master releases the SDA line during the ninth clock pulse. Thus the slave can generate an acknowledge (AS) by pulling the SDA line to a low level. At this moment, the slave switches to transmitting mode.

Step 4: During the next eight clock pulses the slave puts the addressed data byte onto the SDA line.

Step 5: The reception of the byte is acknowledged by the master device which, in turn, pulls down the SDA line during the next SCL clock pulse. By acknowledging a byte, the master prompts the slave to increment its internal address counter and to provide the output of the next data byte.

Step 6: Steps no. 4 and no. 5 are repeated, until the desired amount of bytes have been read.

Step 7: The last byte is output by the slave since it will not be acknowledged by the master.

Step 8: To conclude the read operation, the master doesn’t acknowledge the last byte to be received. A No Acknowledge by the master (NAM) causes the slave to switch from transmitting to receiving mode. Note that the master can prematurely cease any reading operation by not acknowledging a byte.

Step 9: The master gains control over the SDA line and concludes the data transfer by generating a Stop Condition on the bus, i. e., by producing a low/high transition on the SDA line while the SCL line is in a high state. With the SDA and the SCL lines being both in a high state, the I²C Bus is free and ready for another data transfer to be started.

2.3 Order of Data Output on the I²C Bus and Bit Allocation of PDC/VPS Operating Modes

t ↓

I²C Bus		PDC Packet 8/30				VPS Mode	
		Format 1		Format 2			
Byte 1	bit 7	byte 15	bit 0[2)]	byte 16	bit 0[1)]	byte 11	bit 0[2)]
	6		1		1		1
	5		2		2		2
	4		3		3		3
	3		4	byte 17	bit 0		4
	2		5		1		5
	1		6		2		6
	0		7		3		7
Byte 2	bit 7	byte 16	bit 0	byte 18	bit 0	byte 12	bit 0
	6		1		1		1
	5		2		2		2
	4		3		3		3
	3		4	byte 19	bit 0		4
	2		5		1		5
	1		6		2		6
	0		7		3		7
Byte 3	bit 7	byte 17	bit 0	byte 20	bit 0	byte 13	bit 0
	6		1		1		1
	5		2		2		2
	4		3		3		3
	3		4	byte 21	bit 0		4
	2		5		1		5
	1		6		2		6
	0		7		3		7
Byte 4	bit 7	byte 18	bit 0	byte 22	bit 0	byte 14	bit 0
	6		1		1		1
	5		2		2		2
	4		3		3		3
	3		4	byte 23	bit 0		4
	2		5		1		5
	1		6		2		6
	0		7		3		7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.3 Order of Data Output on the I²C Bus and Bit Allocation of PDC/VPS Operating Modes (cont'd)

I²C Bus		PDC Packet 8/30				VPS Mode	
		Format 1		Format 2			
Byte 5	bit 7	byte 19	bit 0	byte 14	bit 0	byte 5	bit 0
	6		1		1		1
	5		2		2		2
	4		3		3		3
	3		4	byte 15	bit 0		4
	2		5		1		5
	1		6		2		6
	0		7		3		7
Byte 6	bit 7	byte 20	bit 0	byte 24	bit 0	byte 15	bit 0
	6		1		1		1
	5		2		2		2
	4		3		3		3
	3		4	byte 25	bit 0		4
	2		5		1		5
	1		6		2		6
	0		7		3		7
Byte 7	bit 7	byte 21	bit 0	byte 13	bit 0	– set to "1"	
	6		1		1	– set to "1"	
	5		2		2	– set to "1"	
	4		3		3	– set to "1"	
	3		4	– set to "1"		– set to "1"	
	2		5	– set to "1"		– set to "1"	
	1		6	– set to "1"		– set to "1"	
	0		7	– set to "1"		– set to "1"	
Byte 8	bit 7	byte 13	bit 0				
	6		1				
	5		2				
	4		3				
	3		4				
	2		5				
	1		6				
	0		7				

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.3 Order of Data Output on the I²C Bus and Bit Allocation of PDC/VPS Operating Modes (cont'd)

I²C Bus		PDC Packet 8/30		VPS Mode
		Format 1	Format 2	
Byte 9	bit 7	byte 14 bit 0		
	6	1		
	5	2		
	4	3		
	3	4		
	2	5		
	1	6		
	0	7		
Byte 10	bit 7	byte 22 bit 0		
	6	1		
	5	2		
	4	3		
	3	4		
	2	5		
	1	6		
	0	7		
Byte 11	bit 7	byte 23 bit 0		
	6	1		
	5	2		
	4	3		
	3	4		
	2	5		
	1	6		
	0	7		

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.3 Order of Data Output on the I²C Bus and Bit Allocation of PDC/VPS Operating Modes (cont'd)

I²C Bus		PDC Packet 8/30			VPS Mode
		Format 1		Format 2	
Byte 12	bit 7	byte 24	bit 0		
	6		1		
	5		2		
	4		3		
	3		4		
	2		5		
	1		6		
	0		7		
Byte 13	bit7	byte 25	bit 0		
	6		1		
	5		2		
	4		3		
	3		4		
	2		5		
	1		6		
	0		7		

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.4 Order of Data Output on the I²C Bus and Bit Allocation for the Header Time Mode (MAB = 0)

t ↓

I²C Bus		Header Time Mode	
Byte 1	bit 7	byte 38	bit 0[2)]
	6		1
	5		2
	4		3
	3		4
	2		5
	1		6
	0		7
Byte 2	bit 7	byte 39	bit 0
	6		1
	5		2
	4		3
	3		4
	2		5
	1		6
	0		7
Byte 3	bit 7	byte 40	bit 0
	6		1
	5		2
	4		3
	3		4
	2		5
	1		6
	0		7
Byte 4	bit 7	byte 41	bit 0
	6		1
	5		2
	4		3
	3		4
	2		5
	1		6
	0		7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.4 Order of Data Output on the I²C Bus and Bit Allocation for the Header Time Mode (MAB = 0) (cont'd)

t ↓

I²C Bus			Header Time Mode		
Byte 5	bit	7	byte 42	bit	0[2)]
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 6	bit	7	byte 43	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 7	bit	7	byte 44	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 8	bit	7	byte 45	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.4 Order of Data Output on the I²C Bus and Bit Allocation for the Header Time Mode (MAB = 0) (cont'd)

t ↓

I²C Bus			Header Time Mode		
Byte 9	bit	7	byte 30	bit	0[2)]
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 10	bit	7	byte 31	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 11	bit	7	byte 32	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 12	bit	7	byte 33	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.4 Order of Data Output on the I²C Bus and Bit Allocation for the Header Time Mode (MAB = 0) (cont'd)

t ↓

I²C Bus			Header Time Mode		
Byte 13	bit	7	byte 34	bit	0[2)]
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 14	bit	7	byte 35	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 15	bit	7	byte 36	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 16	bit	7	byte 37	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.4 Order of Data Output on the I²C Bus and Bit Allocation for the Header Time Mode (MAB = 0) (cont'd)

t ↓

I²C Bus			Header Time Mode		
Byte 1	bit	7	byte 22	bit	0[2)]
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 2	bit	7	byte 23	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 3	bit	7	byte 24	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 4	bit	7	byte 25	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.4 Order of Data Output on the I²C Bus and Bit Allocation for the Header Time Mode (MAB = 0) (cont'd)

t ↓

I²C Bus			Header Time Mode		
Byte 5	bit	7	byte 26	bit	0[2)]
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 6	bit	7	byte 27	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 7	bit	7	byte 28	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 8	bit	7	byte 29	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.4 Order of Data Output on the I²C Bus and Bit Allocation for the Header Time Mode (MAB = 0) (cont'd)

t ↓

I²C Bus			Header Time Mode		
Byte 9	bit	7	byte 14	bit	0[2)]
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 10	bit	7	byte 15	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 11	bit	7	byte 16	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 12	bit	7	byte 17	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.4 Order of Data Output on the I²C Bus and Bit Allocation for the Header Time Mode (MAB = 0) (cont'd)

t ↓

I²C Bus			Header Time Mode		
Byte 13	bit	7	byte 18	bit	0[2)]
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 14	bit	7	byte 19	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 15	bit	7	byte 20	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7
Byte 16	bit	7	byte 21	bit	0
		6			1
		5			2
		4			3
		3			4
		2			5
		1			6
		0			7

1) Message bit numbers according to EBU specification of PDC system.
2) Transmission bit number.

2.5 Description of DAVN and EHB Outputs

DAVN (Data Valid active low)
EHB (First Field active high)

Signal Output	VPS Mode	PDC Mode		
		8/30/2 Mode	8/30/1 Mode	Header Time
DAVN				
H/L-transition (set low)	in line 16 when valid VPS data is received	in the line carrying valid 8/30/2 data	in the line carrying valid 8/30/1 data	in the line carrying valid header row X/0 data
L/H-transition (set high)	at the start of line 16	at the beginning of the next field i.e., at the start of the next data entry window		
always set high	on power-up or during I^2C-Bus accesses when the bus master doesn't acknowledge in order to generate the stop condition			
EHB				
L/H-transition	at the beginning of the first field			
H/L-transition	at the beginning of the second field			

In test mode (i.e. TI = high), both DAVN and EHB are controlled by the CS0 pin and reproduce the state of the CS0 input.

3 Electrical Characteristics

Absolute Maximum Ratings

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Ambient temperature	T_A	0		70	°C	in operation
Storage temperature	T_{stg}	– 40		125	°C	by storage
Total power dissipation	P_{tot}			300	mW	
Power dissipation per output	P_{DQ}			10	mW	
Input voltage	V_{IM}	– 0.3		6	V	
Supply voltage	V_{DD}	– 0.3		6	V	
Thermal resistance	$R_{th\ SU}$			80	K/W	

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V	
Supply current	I_{DD}		5	15	mA	
Ambient temperature range	T_A	0		70	°C	

Note: In the operating range the functions given in the circuit description are fulfilled.

Electrical Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signals SDA, SCL, CS0						
H-input voltage	V_{IH}	$0.7 \times V_{DD}$		V_{DD}	V	
L-input voltage	V_{IL}	0		$0.3 \times V_{DD}$	V	
Input capacitance	C_I			10	pF	
Input current	I_{IM}			10	µA	
Input Signal TI						
H-input voltage	V_{IH}	$0.9 \times V_{DD}$		V_{DD}	V	
L-input voltage	V_{IL}	0		$0.1 \times V_{DD}$	V	
Input capacitance	C_I			10	pF	
Input current	I_{IM}			10	µA	
Input Signals CVBS (pos. Video, neg. Sync)						
Video input signal level	V_{CVBS}	0.7	1.0	2.0	V	2 Vpp with 0.8 V V_{SYNC} and 1.2 V V_{DAT}
Synchron signal amplitude	V_{SYNC}	0.15	0.3	0.8 (1.0)	V	1.0 V only related to VCS signal generation
Data amplitude	V_{DAT}	0.25 $1.5 \times V_{SYNC}$	0.5	1.2	V	
Coupling capacitor	C_C		33		nF	
H-input current	I_{IH}			10	µA	V_I = 5 V
L-input current	I_{IL}	– 1000	– 400	– 100	µA	V_I = 0 V
Source impedance	R_S			250	Ω	
Leakage resistance at coupling capacitor	R_C	0.91	1	1.2	MΩ	

Electrical Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signals DAVN, EHB, VCS						
H-output voltage	V_{QH}	V_{DD} – 0.5			V	I_Q = – 100 µA
L-output voltage	V_{QL}			0.4	V	I_Q = 1.6 mA
Output Signals SDA (Open-Drain-Stage)						
L-output voltage	V_{QL}			0.4	V	I_Q = 3.0 mA
Permissible output voltage				5.5	V	
PLL-Loop Filter Components (see application circuit)						
Resistance at PD2/ VCO2	R_1		6.8		kΩ	
Resistance at VCO1	R_2		1200		kΩ	
Attenuation resistance	R_3		6.8		kΩ	
Resistance at PD2/ VCO2	R_5		1200		kΩ	
Integration capacitor	C_1		2.2		nF	
Integration capacitor	C_3		33		nF	
VCO – Frequence Range Adjustment						
Resistance at IREF (for bias current adjustment)	R_4		100		kΩ	

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

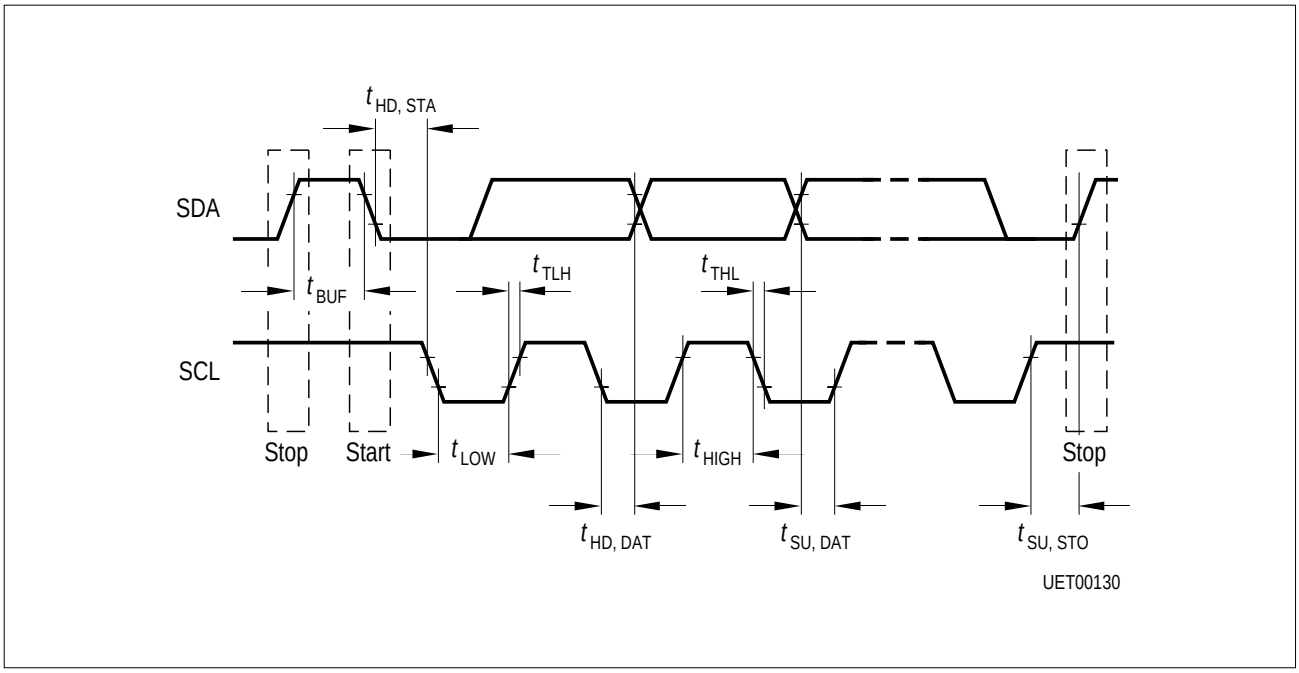


Figure 3
I²C-Bus Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Inactive time prior to new transmission start-up	t_{BUF}	4.7		µs
Hold time during start condition	$t_{HD; STA}$	4.0		µs
Low-period of clock	t_{LOW}	4.7		µs
High-period of clock	t_{HIGH}	4.0		µs
Set-up time for data	$t_{SU;DAT}$	250		ns
Rise time for SDA and SCL signal	t_{TLH}		1	µs
Fall time for SDA and SCL signal	t_{THL}		300	ns
Set-up time for SCL clock during stop condition	$t_{SU; STO}$	4.7		µs

All values referred to V_{IH} and V_{IL} levels.

4 PDC/VPS-Receiver

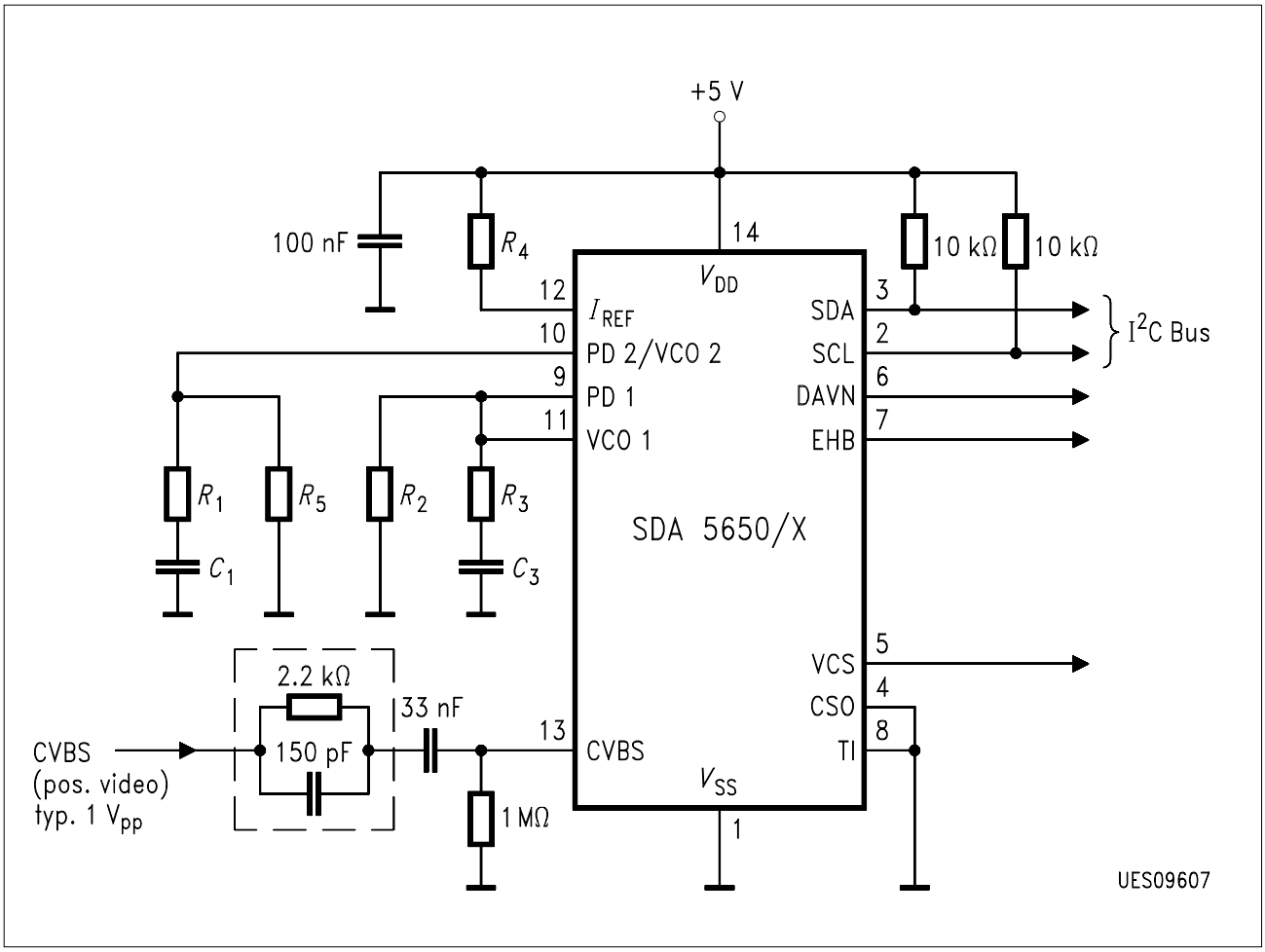
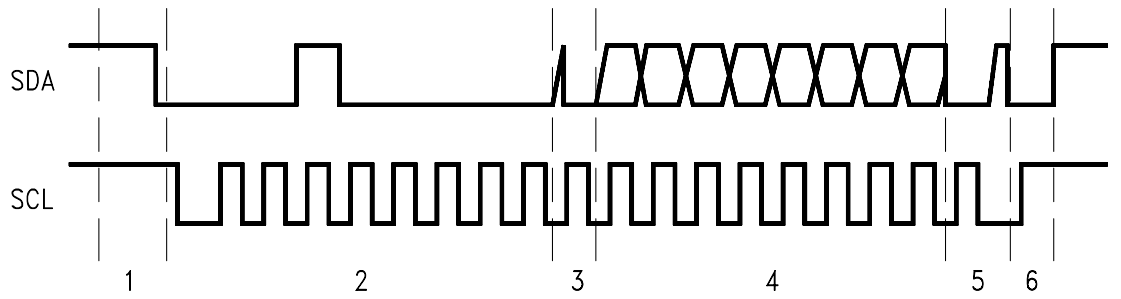


Figure 4

5 Appendix

5.1 Control Register Write (I^2C-Bus Write)

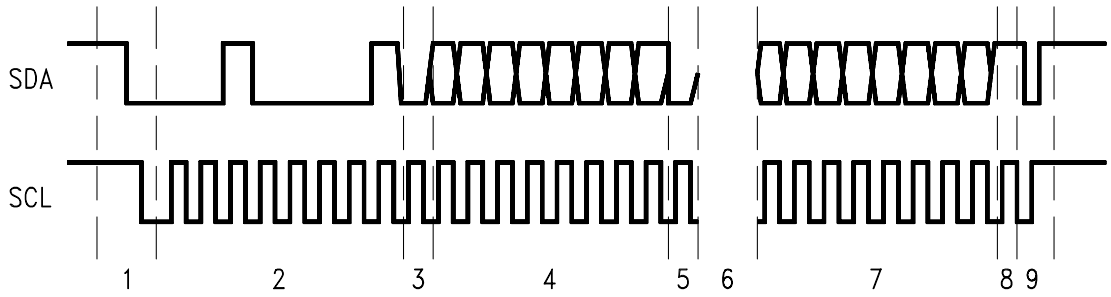


1 Start Condition
2 Chip Address Write mode
3 Acknowledge by slave
4 Data byte for Control Register
5 Acknowledge by slave
6 Stop Condition

UED09416

Figure 5

5.2 Data Register Read (I^2C-Bus Read)



1 Start Condition
2 Chip Address
3 Acknowledge by slave
4 Output of 1st data byte from slave to master
5 Acknowledge by master
6 Output of further bytes
7 Output of last byte
8 No Acknowledge by master
9 Stop Condition

UED09417

Figure 6

5.3 DAVN and EHB Timing

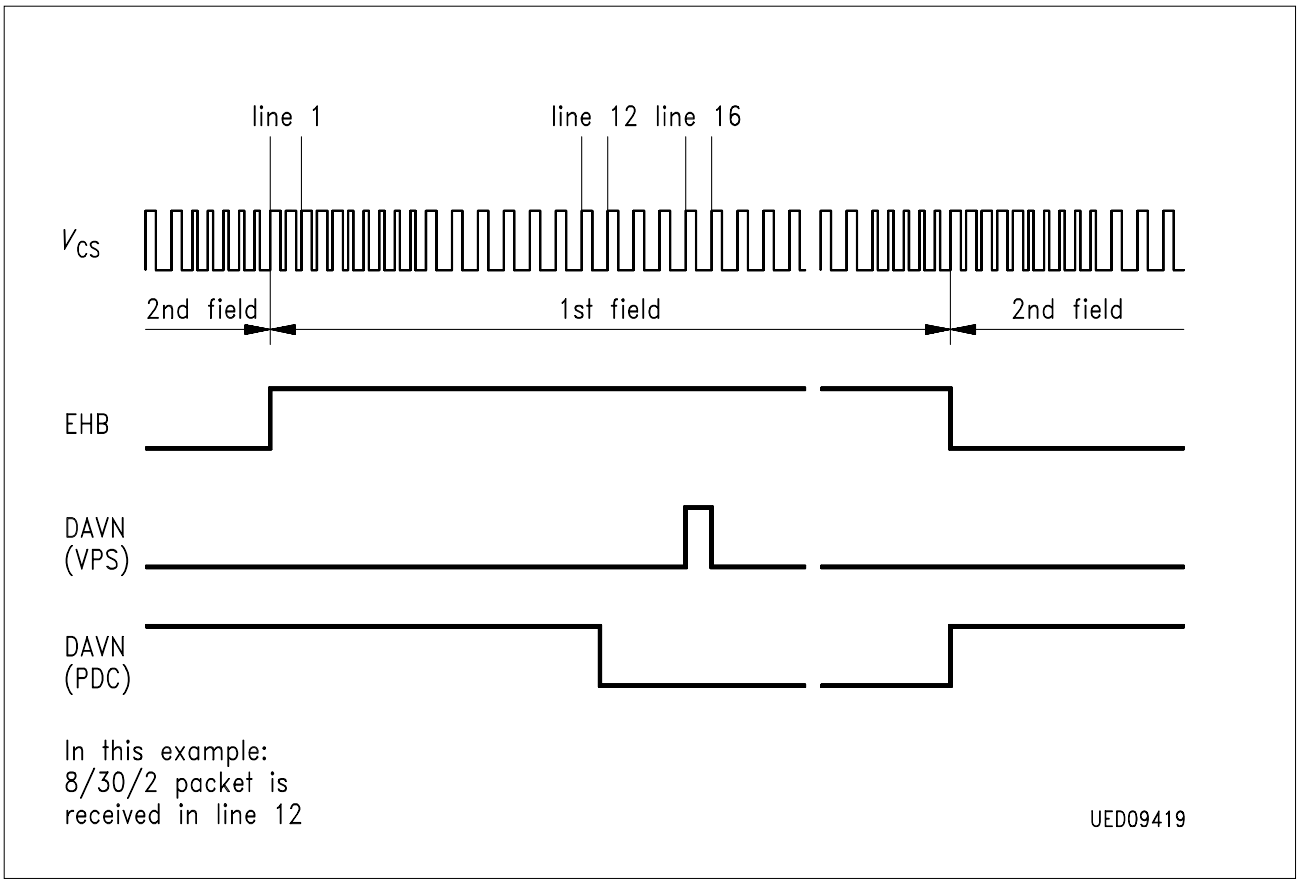


Figure 7

5.4 Position of Teletext and VPS Data Lines within the Vertical Blanking Interval

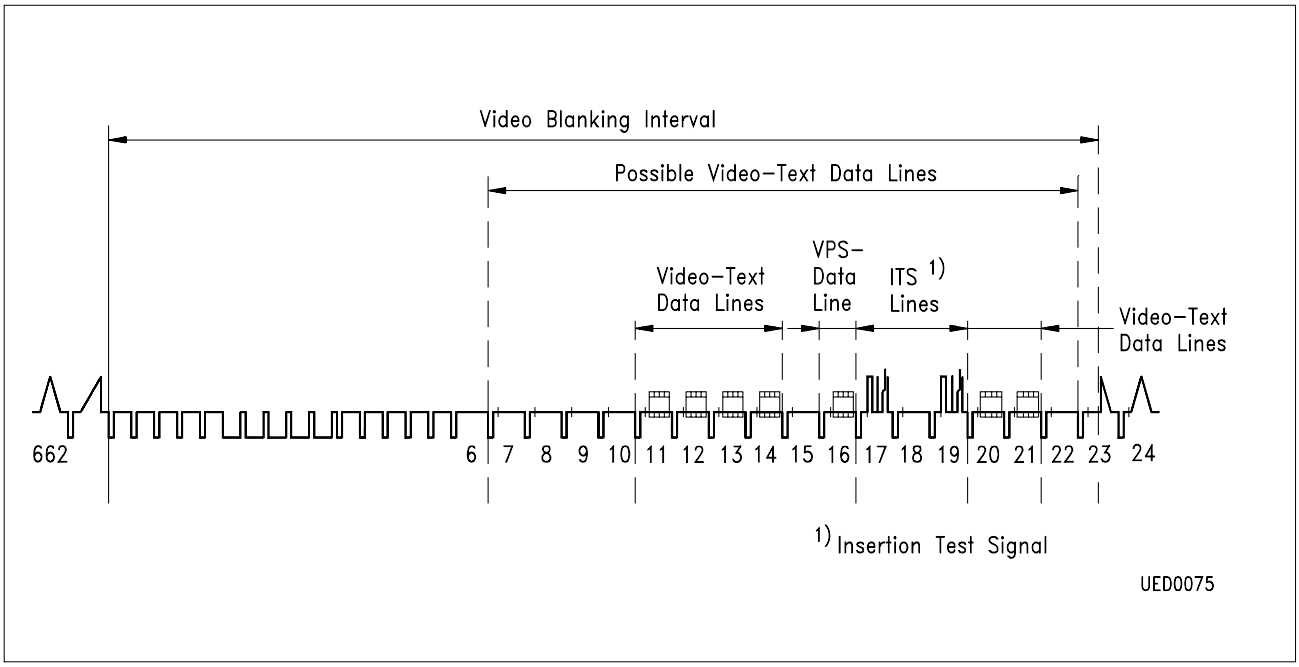


Figure 8

5.5 Definition of Voltage Levels for VPS Data Line

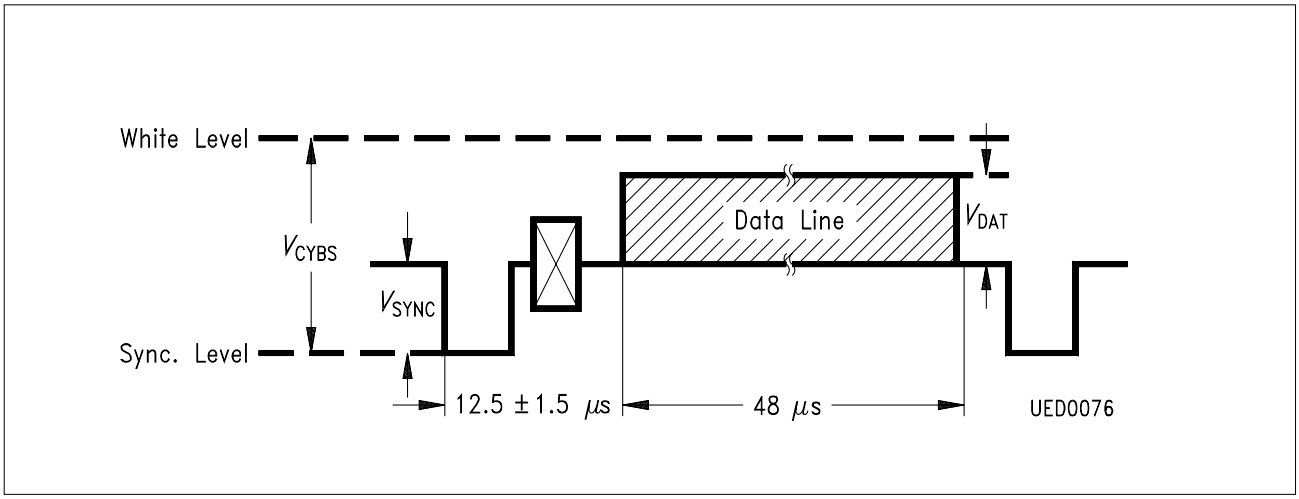


Figure 9

5.6 BDSP 8/30 Format 1 Bit Allocation

Byte No.	Bit No.								Contents
	0	1	2	3	4	5	6	7	
13									Network Identification 1. Byte
14									Network Identification 2. Byte
15	Weight			Weight			Sign		Time Offset Code
	2^{-2}	2^{-1}	2^{0}	2^{1}	2^{2}	2^{3}	0 1		
16	MJD Digit Weight 10^4				1	1	1	1	Modified Julian Date (MJD) 1. Byte
17	MJD Digit Weight 10^2				MJD Digit Weight 10^3				Modified Julian Date 2. Byte
18	MJD Digit Weight 10^0				MJD Digit Weight 10^1				Modified Julian Date (MJD) 3. Byte
19	UTC Hours Units				UTC Hours Tens				Universal Time Coordinated (UTC) 1. Byte
20	UTC Minutes Units				UTC Minutes Tens				Universal Time Coordinated 2. Byte
21	UTC Seconds Units				UTC Seconds Tens				Universal Time Coordinated 3. Byte
22									Short Programme Label 1. Byte
23									Short Programme Label 2. Byte
24									Short Programme Label 3. Byte
25									Short Programme Label 4. Byte

Note: This corresponds to the coding adopted in CCIR teletext system B BDSP 8/30 format 1.
NB: The received bytes are output on the I^2C Bus in a transparent way, i.e., on a bit-first-in-first-out basis. No bit manipulation is performed on the chip in this operating mode.
Concerning bytes no. 16 through 21: When evaluating the numbers, note that each 4-bit-digit has been incremented by one prior to transmission, and the least significant bits are transmitted first.

5.7 Structure of the Teletext Data Packet 8/30 Format 2

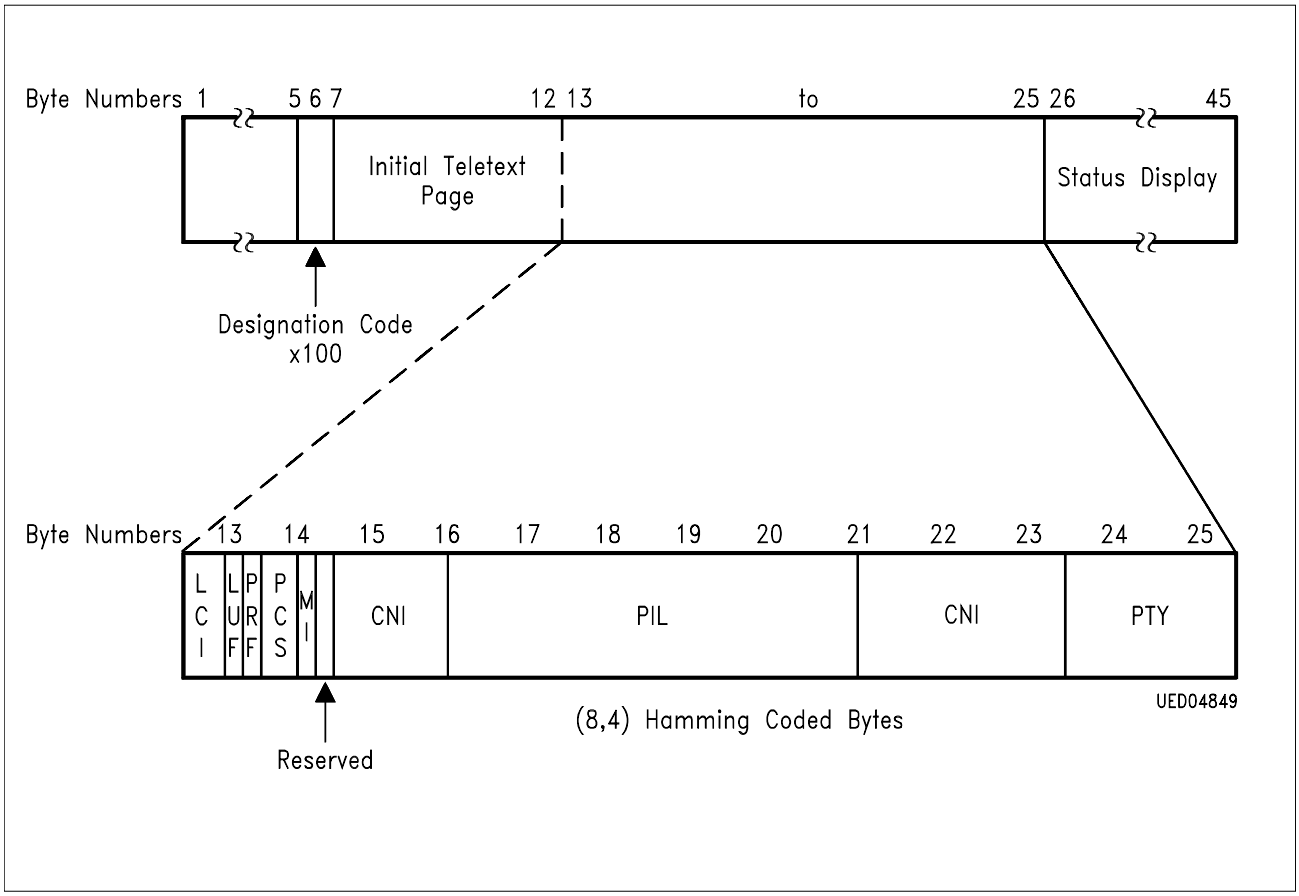


Figure 10

5.8 BDSP 8/30 Format 2 Bit Allocation

The four message bits of byte 13 are used as follows

byte 13	bit	0 – LCI	b_1	label channel identifier
		1 – LCI	b_2	
		2 – LUF		label update flag
		3 – reserved but as yet undefined		

5.8 BDSP 8/30 Format 2 Bit Allocation (cont'd)

The message bits of bytes 14-25 are used in a way similar to the coding of the label in the dedicated television line as follows:

byte 14	bit	0 PCS	b_1	status of analogue sound
		1 PCS	b_2	
		2		reserved but yet
		3		undefined
byte 15	bit	0 CNI	b_1	country
		1 CNI	b_2	
		2 CNI	b_3	
		3 CNI	b_4	
byte 16	bit	0 CNI	b_9	network (or programme provider)
		1 CNI	b_{10}	
		2 PIL	b_1	day
		3 PIL	b_2	
byte 17	bit	0 PIL	b_3	
		1 PIL	b_4	
		2 PIL	b_5	
		3 PIL	b_6	month
byte 18	bit	0 PIL	b_7	
		1 PIL	b_8	
		2 PIL	b_9	
		3 PIL	b_{10}	hour
byte 19	bit	0 PIL	b_{11}	
		1 PIL	b_{12}	
		2 PIL	b_{13}	
		3 PIL	b_{14}	

5.8 BDSP 8/30 Format 2 Bit Allocation (cont'd)

byte 20	bit	0 PIL	b_{15}	minute
		1 PIL	b_{16}	
		2 PIL	b_{17}	
		3 PIL	b_{18}	
byte 21	bit	0 PIL	b_{19}	
		1 PIL	b_{20}	
		2 CNI	b_5	country
		3 CNI	b_6	
byte 22	bit	0 CNI	b_7	
		1 CNI	b_8	
		2 CNI	b_{11}	network (or programme provider)
		3 CNI	b_{12}	
byte 23	bit	0 CNI	b_{13}	
		1 CNI	b_{14}	
		2 CNI	b_{15}	
		3 CNI	b_{16}	
byte 24	bit	0 PTY	b_1	programme type
		1 PTY	b_2	
		2 PTY	b_3	
		3 PTY	b_4	
byte 25	bit	0 PTY	b_5	
		1 PTY	b_6	
		2 PTY	b_7	
		3 PTY	b_8	

5.9 Data Format of Programme Delivery Data in the Dedicated TV Line (VPS)

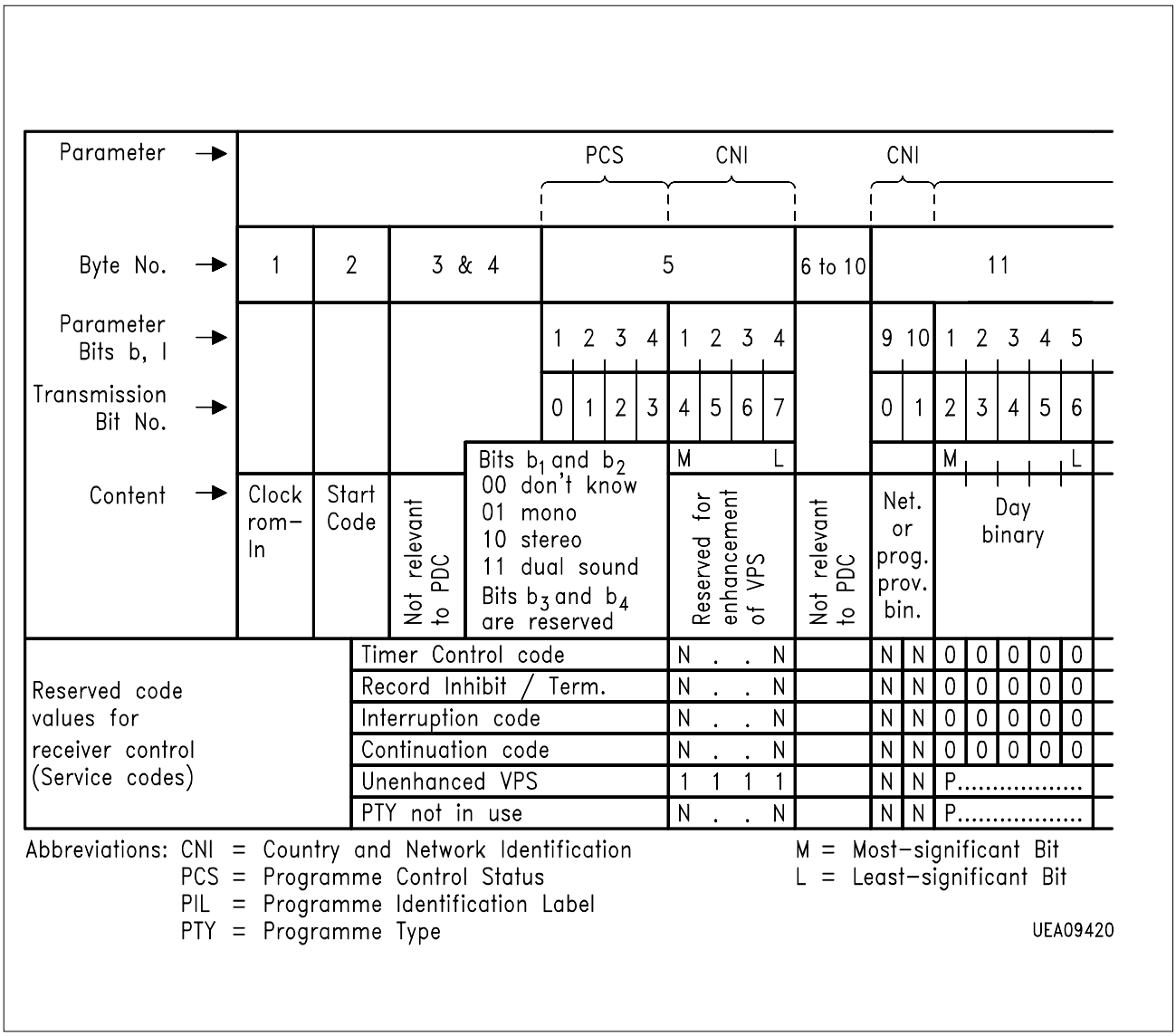


Figure 11

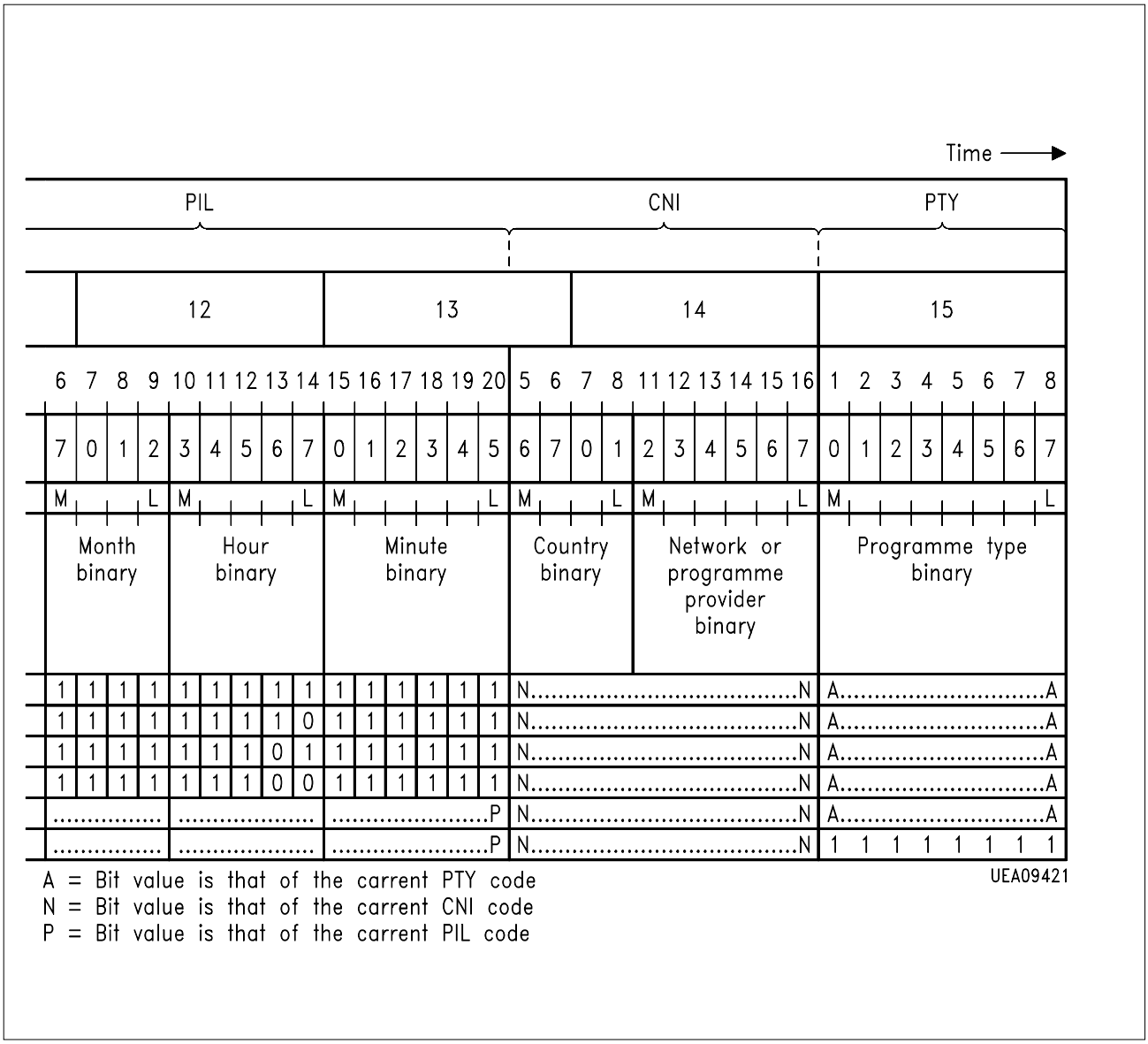
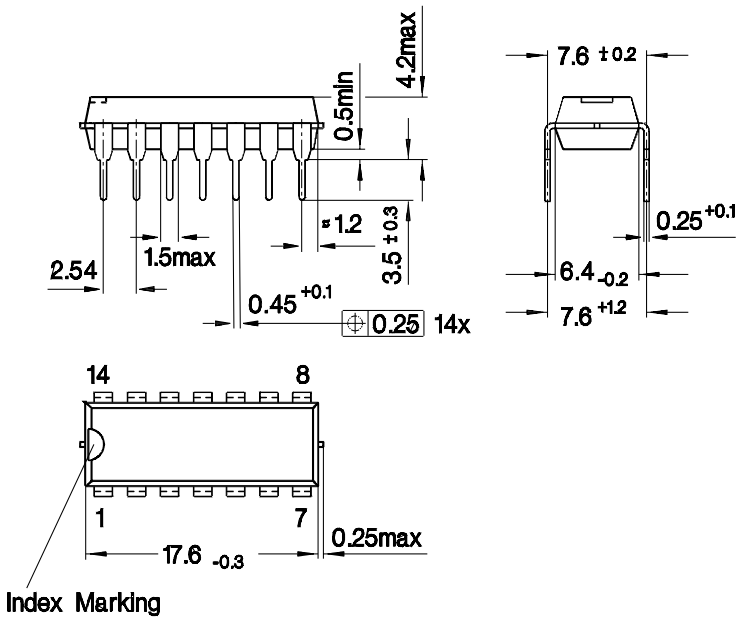

Time
PIL
CNI
PTY
12
13
14
15
6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 5 6 7 8 11 12 13 14 15 16 1 2 3 4 5 6 7 8
7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
M L M L M L M L M L M L
Month binary
Hour binary
Minute binary
Country binary
Network or programme provider binary
Programme type binary
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 N.....N A.....A
1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 N.....N A.....A
1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 N.....N A.....A
1 1 1 1 1 1 1 0 0 1 1 1 1 1 1 N.....N A.....A
....P N.....N A.....A
....P N.....N 1 1 1 1 1 1 1 1
A = Bit value is that of the carrent PTY code
N = Bit value is that of the carrent CNI code
P = Bit value is that of the carrent PIL code
UEA09421

Figure 12

6 Package Outlines

P-DIP-14-1
(Plastic Dual In-line Package)

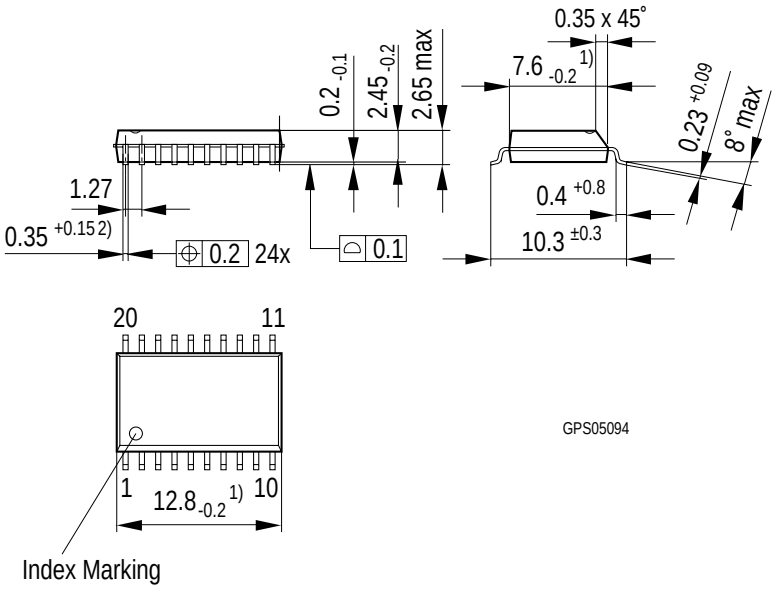


GPD05005

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

P-DSO-20-1
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

GPS05094

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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