Semiconductor, Inc.

Ei68C681
Ei88C681
DUAL UART

FEATURES

- Full duplex, dual channel asynchronous receiver and transmitter
- Quadruple-buffered receiver and transmitter
- Stop bits programmable in 1/16-bit increments
- Internal bit rate generator with 23 bit rates
- Independent bit rate selection for each Rx and Tx
- Maximum bit rate: 1 x clock - 2 Mb/sec., 16 x clock- 250 Kb/sec.
- Normal, auto-echo, local loop-back and remote loop-back modes
- Multi-function 16-bit counter/timer
- Interrupt output with 8 maskable interrupt ing conditions
- Interrupt vector output on acknowledge
- Programmable interrupt daisy chain
- Up to 15 I/O pins (depending on package and version)
- Multidrop mode compatible with 8051 nine-bit mode
- On-chip oscillator for crystal
- Stand-by mode to reduce operating power
- Advanced CMOS low power technology

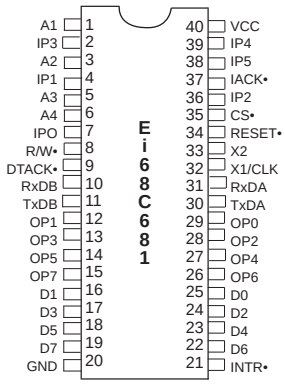
DESCRIPTION

The Epic Ei88C681/Ei68C681 DUART Dual Universal Asynchronous Receiver and Transmitter is a data communication device that provides two fully independent full duplex asynchronous communication channels in a single package. The DUART is designed for use in microprocessor based systems and may be used in a polled or interrupt driven environment.

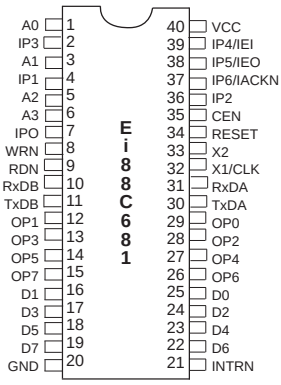
Two basic versions of the DUART are available, each optimized for use with various microprocessor families: the 88C81 for 8085/85, 8080/88, Z80, Z8000, 68XX and 65XX family based systems., and the 68C681 for 68000 family based systems. A programmable mode of the Ei88C681 versions provides an interrupt daisy chain for use in Z80 and Z8000 based systems. The bus interfaces are however general enough to allow interfacing with other microprocessors and microcontrollers. The 88C681 and 68C681 are enhanced versions of the Signetics 2681 and the Motorola 68681, and are pin and function compatible with those devices. Each channel of the DUART may be independently programmed for operating mode and data format. The operating speed of each receiver and transmitter can beselected from baud rate generator, from the multi-purpose on chip counter/timer or from an external 1 x or 16 x clock.The bit rate generator can operate directly from a crystal connected across two pins or from an external clock. The ability to independently program the operating speed of the receiver and transmitter of each channel makes the DUART attractive for split-speed channel application such as clustered terminal systems. Both receive and transmit data is quadruple-buffered in on-chip FIFO to minimize the risk of receiver overrun or to reduce overhead in interrupt-drive applications.

PIN CONFIGURATION

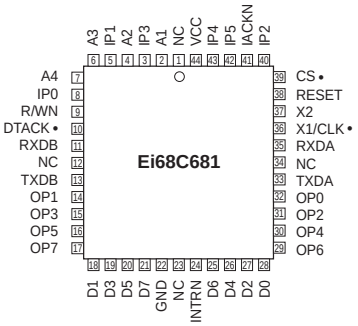
Part Numbers May Be Marked With "IMP" or "Ei."



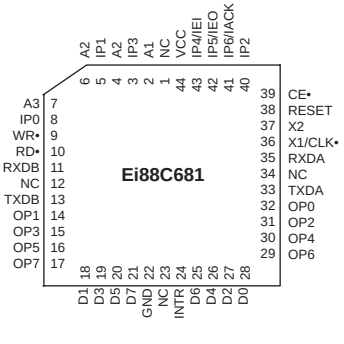
40-PIN DIP



40-PIN DIP



44-PIN PLCC



44-PIN PLCC

The DUART provides a flow control capability to inhibit transmission from a remote device when the buffer of the receiving DUART is full, thus preventing loss of data. The DUART also provides a general purpose 16-bit counter/timer (which may also be used as a programmable bit rate generator), a multipurpose input port and a multipurpose output port.

These ports can be used as general purpose I/O ports or can be assigned specific functions such as clock inputs or status/interrupt outputs under program control.

The Ei68C681 are fabricated using Epic's advanced CMOS process to provide high performance and low power consumption.

BLOCK DIAGRAM