ILC1832

Preliminary

µP Supervisory Circuit

POWER POWERED BY IMPALA ON THE GO

General Description

The ILC1832 is a multifunction circuit which monitors microprocessor activity, external reset and power supplies in microprocessor based systems. Ths circuit functions include a watchdog timer, power supply monitor, microprocessor reset, and manual pushbutton reset input.

The power supply line is monitored with a comparator and an internal voltage reference. $\overline{RST}$ is forced low when an out-of-tolerance condition exists and remains asserted for at least 250ms after V_{CC} rises above the threshold voltage (2.55V or 2.88V). The $\overline{RST}$ pin will remain logic low with V_{CC} as low as 1.4V.

The Watchdog input ($\overline{ST}$) monitors µP activity and will assert $\overline{RST}$ if no µP activity has occurred within the watchdog time-out period. The watchdog timeout period is selectable with nominal periods of 150, 600, or 1200 milliseconds.

Features

- Power OK/Reset Time Delay, 250ms min.
- Watchdog Timer, 150 ms, 600ms, or 1.2s Typical
- Precision Supply Voltage Monitor, Select Between 5% or 10% of Supply Voltage
- 18µA Supply Current
- Debounced External Reset Input
- 8-Pin SOIC or DIP Package

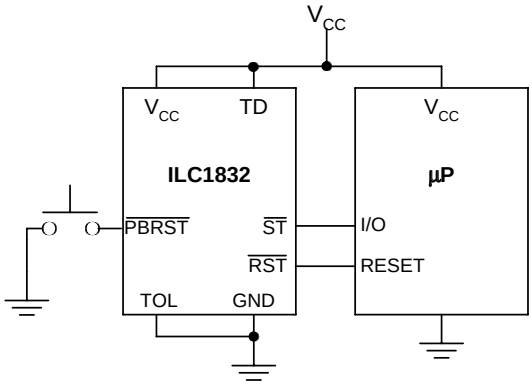
Applications

- Computers
- Controllers
- Critical Microprocessor Power Monitoring
- Intelligent Instruments
- Portable Equipment

Ordering Information

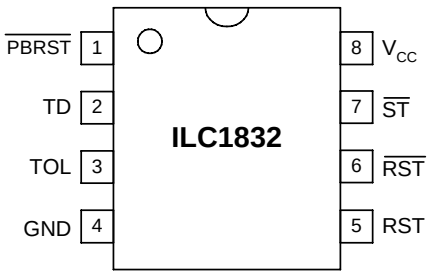
Part	Package	Temp. Range
ILC1832N	8-Lead PDIP	-40°C to +85°C
ILC1832M	8-Lead SOIC	-40°C to +85°C

Typical Circuit



Pin-Package Configurations

Top View



ETC1832N - 8 Lead Plastic DIP Package
ETC1832M - 8 Lead Plastic SOIC Package

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Terminal Voltage	V_{CC}	-0.3 to 7.0	V
	All other inputs	-0.3 to (V_{CC} + 0.3)	V
Input Current	V_{CC}	250	mA
	GND All other inputs	25	mA
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range		-65 to +150	°C
Lead Temperature (Soldering, 10 sec.)		300	°C
Power Dissipation		700	mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability. Operating ranges define those limits between which the functionality of the device is guaranteed.

Electrical Characteristics

V_{CC} = 3 to 5.5V, T_A = Operating Temperature Range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range, V_{CC}				5.5	V
Supply Current, I_{CC}	V_{CC} = 5V (See Note 1) V_{CC} = 3.3V (See Note 1)		18 15	30 25	µA
$\overline{ST}$ and $\overline{PBRST}$ Input Levels	V_{IH}, $V_{CC} \geq$ 2.7V V_{IH}, V_{CC} < 2.7V V_{IL}	2.0 V_{CC} –0.4 -0.3		V_{CC} + 0.3 V_{CC} + 0.3 0.5	V
Input Leakage $\overline{PBRST}$, I_{IL}	(See Note 2)			±1	µA
Output Voltage, $\overline{RST}$, RST	I_{SOURCE} = 350µA, V_{CC} = 3.3V	2.4			V
Output Voltage, $\overline{RST}$, RST	I_{SINK} = 10mA, V_{CC} = 3.3V			0.4	V
Output Voltage, $\overline{RST}$	I_{SINK} = 50µA, V_{CC} = 1.4V			0.3	V
V_{CC} 5% Trip Point (Reset Threshold Voltage)	TOL= GND	2.80	2.88	2.97	V
V_{CC} 10% Trip Point (Reset Threshold Voltage)	TOL= V_{CC}	2.47	2.55	2.64	V
Input Capacitance, $\overline{ST}$, TOL	C_{IN} (See Note 3)			5	pF
Output Capacitance, $\overline{RST}$, RST	C_{OUT} (See Note 3)			7	pF
$\overline{PBRST}$ Min. Pulse Width, t_{PB}	$\overline{PBRST}$ = V_{IL} (See note 4)	20			ms
$\overline{PBRST}$ Delay, t_{PBD}		1	4	20	ms
Reset Active Time, t_{RST}		250	610	1000	ms
$\overline{ST}$ Pulse Width, t_{ST}		20			ns
$\overline{ST}$ Timeout Period, t_{TD}	TD = 0V TD = Open TD = V_{CC}	62.5 250 500	150 600 1200	250 1000 2000	ms
V_{CC} Fall Time, t_F		40			µs
V_{CC} Rise Time, t_R		0			ns
V_{CC} Detect to RST Low and RST High, tRPD	V_{CC} Falling at 1.66 mV/µs		5	8	µs
V_{CC} Detect to RST Open and RST Low, tRPU	V_{CC} Rising	250	610	1000	ms

Note 1: I_{CC} is measured with $\overline{PBRST}$ and all outputs open and inputs within 0.5V of supply rails.

Note 2: $\overline{PBRST}$ has an internal 40kΩ (typical) pull-up resistor to V_{CC}.

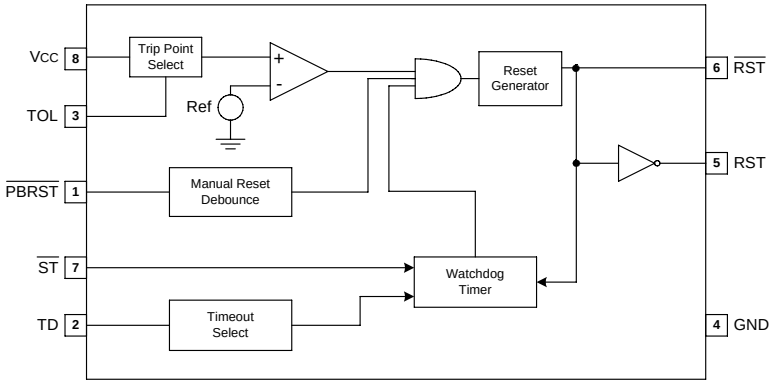
Note 3: Guaranteed by design at T_A = 25°C.

Note 4: $\overline{PBRST}$ must be held low for a minimum of 20ms to guarantee a reset.

Pin Functions

Pin Number	Pin Name	Description
1	$\overline{\text{PBRST}}$	Pushbutton reset input. This input is debounced and can be driven with external logic signals or a mechanical pushbutton to actively force a reset. All pulses less than 1ms in duration on the $\overline{\text{PBRST}}$ pin are ignored. Any pulse with a duration of 20ms or greater is guaranteed to cause a reset. $\overline{\text{PBRST}}$ has an internal 40kΩ (typical) pull-up resistor to V_{CC}.
2	TD	Time delay input. This input selects the timebase used by the watchdog timer. When TD = 0V, the watchdog timeout period is set to a nominal value of 150ms, when TD = open, the watchdog timeout period is set to a nominal value of 600ms and when TD = V_{CC}, the watchdog timeout period is 1.2 sec nominally.
3	TOL	Tolerance select input. Selects whether 5% or 10% of V_{CC} is used as the reset threshold voltage. When TOL = 0V, the 5% tolerance level is selected and when TOL = V_{CC}, a 10% tolerance level is selected.
4	GND	Ground pin, 0V reference.
5	RST	RST is asserted high if either V_{CC} goes below the reset threshold, the watchdog times out or $\overline{\text{PBRST}}$ is pulled low for a minimum of 20ms. RST remains asserted for one reset timeout period after V_{CC} exceeds the reset threshold or after the watchdog times out or after $\overline{\text{PBRST}}$ goes high.
6	$\overline{\text{RST}}$	$\overline{\text{RST}}$ is asserted low if either V_{CC} goes below the reset threshold, the watchdog times out or $\overline{\text{PBRST}}$ is pulled low for a minimum of 20ms. $\overline{\text{RST}}$ remains asserted for one reset timeout period after V_{CC} exceeds the reset threshold or after the watchdog times out or after $\overline{\text{PBRST}}$ goes high. Open-drain output.
7	ST	Input to the watchdog timer. If ST does not see a transition from high to low within the watchdog timeout period, RST and RST will be asserted.
8	V_{CC}	Power supply input.

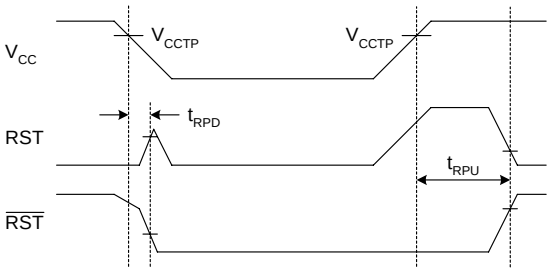
Block Diagram



Circuit Description

Power Monitor

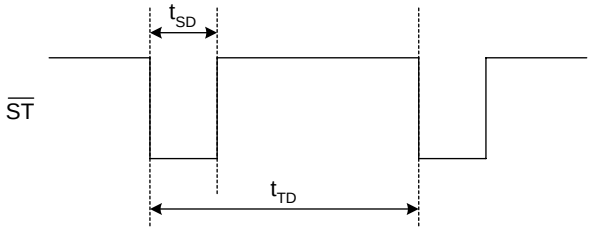
The RST and $\overline{RST}$ pins are asserted whenever V_{CC} falls below the reset threshold voltage set by the TOL pin. A 5% tolerance level (2.88V reset threshold voltage) can be selected by connecting the TOL pin to ground or a 10% tolerance (2.55V reset threshold voltage) can be selected by connecting the TOL pin to V_{CC}. The reset pins will remain asserted for a period of 250ms after V_{CC} has resen above the reset threshold voltage. The reset function ensures the microprocessor is properly reset and powers up into a known condition after a power failure. $\overline{RST}$ will remain valid with V_{CC} as low as 1.4V.



Power-Up/Power-Down Sequence

Watchdog Timer

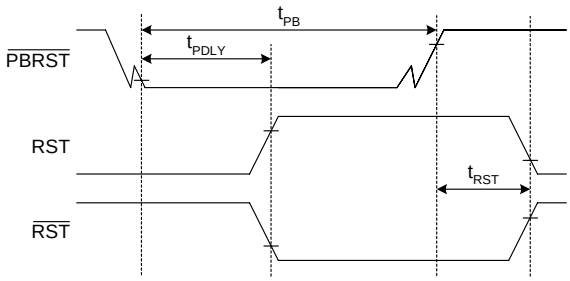
The microprocessor can be monitored by connecting the $\overline{ST}$ pin (watchdog input) to a bus line or I/O line. If a high-to-low transition does not occur on the $\overline{ST}$ pin within the watchdog timeout period set by the TD pin (see Table 1), the RST and $\overline{RST}$ pins will be asserted rsulting in a microprocessor reset. RST and $\overline{RST}$ will remain asserted for 250ms when this occurs. A minimum pulse of 75ns or any transition high-to-low on the $\overline{ST}$ pin will reset the watchdog timer. The watchdog timer will be reset if $\overline{ST}$ sees a valid transition within the watchdog timeout period.



Watchdog Input

Pushbutton Reset Input

The $\overline{PBRST}$ input can be driven with a manual pushbutton switch or with external logic signals. The input is internally debounced and requires an active low signal to force the reset outputs into their active states. The $\overline{PBRST}$ input will recognize any pulse that is 20ms in duration or greater and will ignore all pulses that are less than 1ms in duration.



Pushbutton Reset

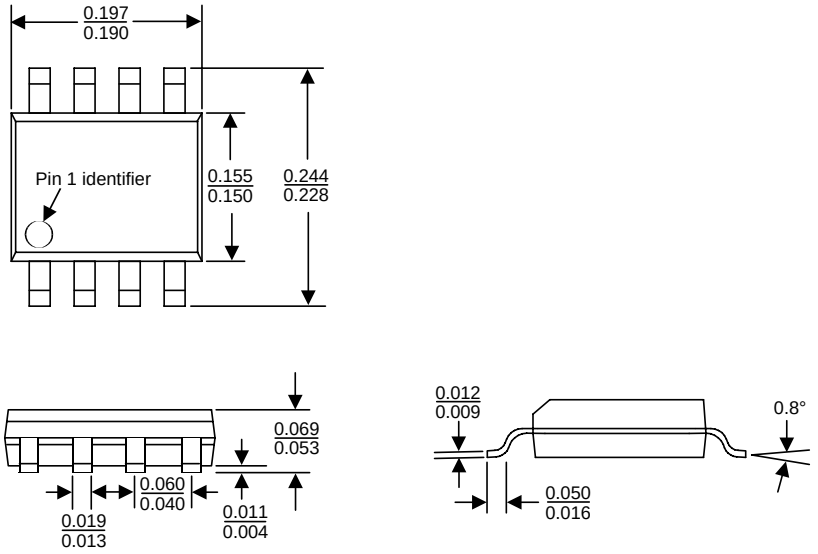
TD Pin	t_{TD}		
	Min.	Typ.	Max.
GND	62.5 ms	150 ms	250 ms
Open	250 ms	600 ms	1000 ms
V_{CC}	500 ms	1200 ms	2000 ms

Alternate Source Reference Guide

Industry P/N	ILC Direct Replacement
DS1832	ILC1832N
DS1832S	ILC1832M

Packaging Information

M Package, 8-Pin Small-Outline



N Package, 8-Pin Plastic Dual In-Line