PRODUCT PREVIEW

T-52-33-15

80C51SL-BG
KEYBOARD CONTROLLER

- Superset of 80C51 Architecture
- Complete 8042 Keyboard Controller Functionality
- 8042-Style Host Interface
- Optional Hardware Speed-Up of Gate A20 and RCL
- Local 16 x 8 Keyboard Switch Matrix Support
- Two Industry-Standard Serial Keyboard Interfaces; Supported via Four High-Drive Outputs
- 5 LED Drivers
- Low Power CHMOS Technology
- Power Management
- 4-Channel, 8-Bit A/D
- Interface for up to 32 Kbytes of External Memory
- Slew-Rate-Controlled I/O Buffers Used to Minimize Noise
- 256 Bytes Data RAM
- 8 Kbytes Factory-Programmable Mask ROM Available
- Three Multifunction I/O Ports
- 10 Interrupt Sources with 6 User-Definable External Interrupts
- 2 MHz–16 MHz Clock Frequency, V_{CC} = 5V ±10%
- 100-Pin PQFP
- Customizable to Specific Application Requirements
- Pre-Programmed Keyboard Controller/ Scanner Firmware Available

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The 80C51SL-BG, based on Intel's industry-standard MCS®-51 microcontroller family, is designed for keyboard control in laptop and notebook PCs. The highly integrated keyboard controller incorporates an 8042-style host interface with expanded memory, keyboard-scan, and power management. The 80C51SL supports both serial and scanned keyboard interfaces and is available in pre-programmed versions to reduce time to market.

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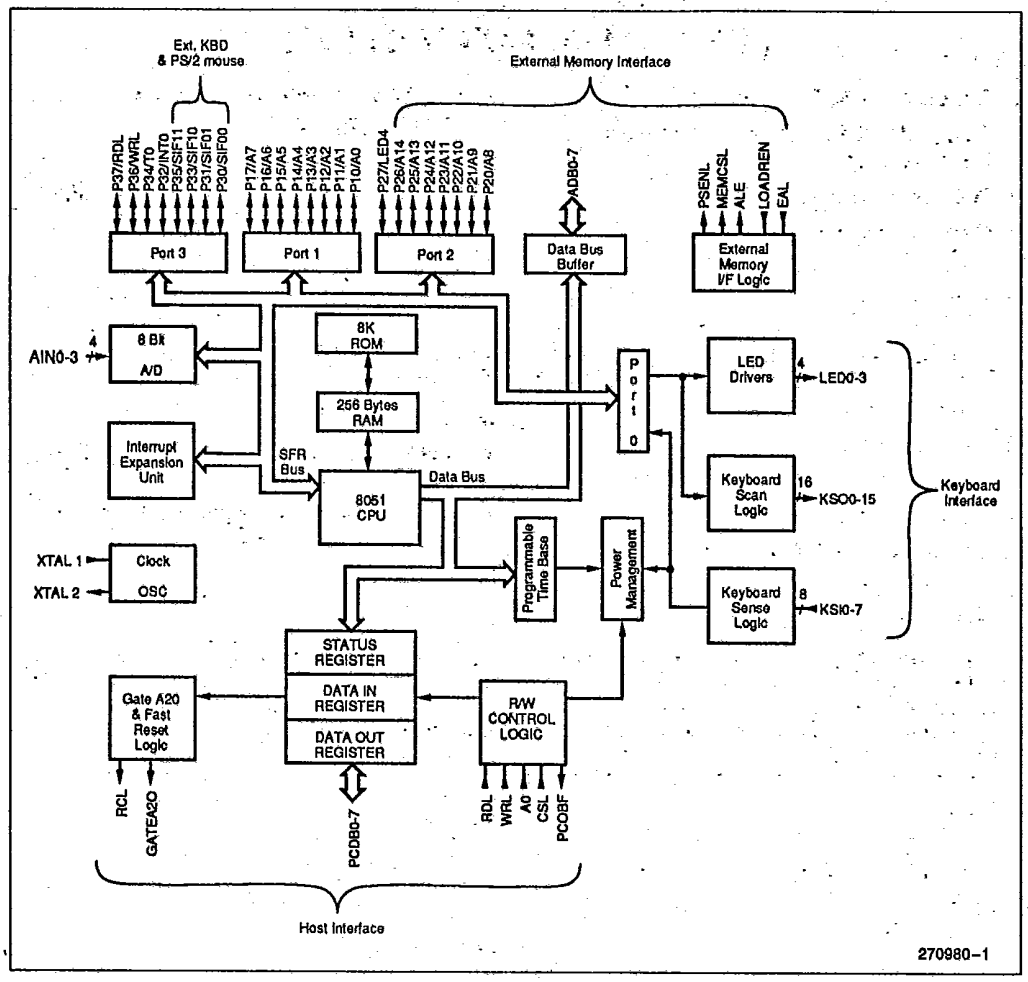
Ext. KBD & PS/2 mouse
External Memory Interface
P37/RDL
P36/WRL
P34/T0
P32/INT0
P35/SIF11
P33/SIF10
P31/SIF01
P30/SIF00
P17/A7
P16/A6
P15/A5
P14/A4
P13/A3
P12/A2
P11/A1
P10/A0
P27/LED4
P26/A14
P25/A13
P24/A12
P23/A11
P22/A10
P21/A9
P20/A8
ADB0-7
PSENL
MEMCSL
ALE
LOADREN
EAL
Port 3
Port 1
Port 2
Data Bus Buffer
External Memory I/F Logic
AIN0-3
4
8 Bit A/D
8K ROM
256 Bytes RAM
Interrupt Expansion Unit
SFR Bus
8051 CPU
Data Bus
Port 0
LED Drivers
LED0-3
Keyboard Scan Logic
KSO0-15
Keyboard Interface
Keyboard Sense Logic
KSI0-7
XTAL 1
XTAL 2
Clock OSC
Programmable Time Base
Power Management
STATUS REGISTER
DATA IN REGISTER
DATA OUT REGISTER
R/W CONTROL LOGIC
Gate A20 & Fast Reset Logic
RCL
GATEA20
PCDB0-7
RDL
WRL
A0
CSL
PCOBF
Host Interface
270980-1

FUNCTIONAL DESCRIPTION

The 80C51SL is a universal keyboard controller that is designed for intelligent keyboard management in laptop and notebook computer applications. It uses an 80C51 microcontroller CPU core to produce a superset of the features provided by the industry-standard 8042 keyboard controller. Added features include two high-drive serial keyboard interfaces, on-chip optional hardware speedup for both GATEA20 and RCL, five LED drivers, a four-channel, eight-bit A/D converter and ten interface sources.

This data sheet concentrates on the 80C51SL enhancements to the 80C51. For general information about the 80C51SL, refer to the "Hardware Description of the 8051, 8052 and 80C51" and the "80C51BH-1/80C51BH-2 CHMOS Single-Chip 8-Bit Microcomputer with Factory Mask-Programmable ROM" data sheet in the *Embedded Microcontroller and Processor Handbook*.

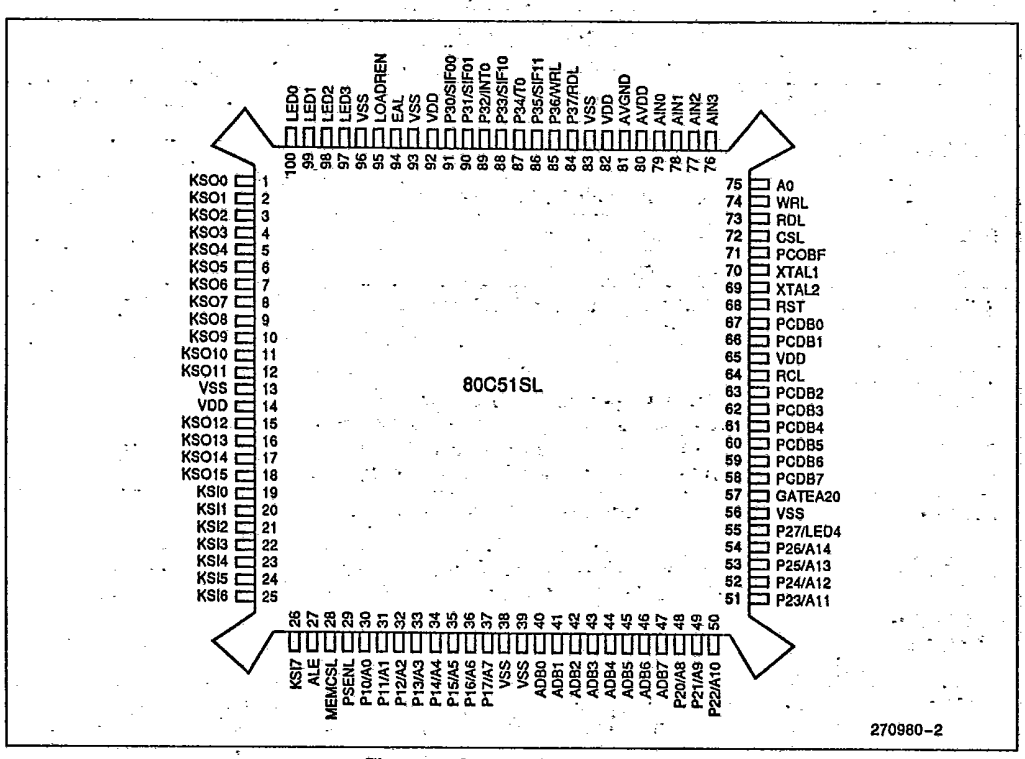

Figure 2. Connection Diagram

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Symbol	Type	Description
V_{SS}		Circuit ground potential.
V_{DD}		Supply voltage during normal, Idle, and Power-Down operation; nominally +5V ±10%.
PCDB0–7	I/O	Host interface data bus. An 8-bit, bidirectional port for data transfers between the host processor and the keyboard controller.
WRL	I	The active-low, host-interface write signal.
RDL	I	The active-low, host-interface read signal.
CSL	I	The active-low, host-interface chip select.
A0	I	Host-Interface Address select input. When high, it selects the command/status register; when low it selects the data registers.
PCOBF	O	The active-high, host-interface Output Buffer Full interrupt.
GATEA20	O	Gate A20 control signal output.
RCL	O	Host reset — active low.
LED0–3	O	LED output drivers.
KSI0–7	I	Keyboard input scan lines (input Port 0). Schmitt inputs with 5K–20K pull-up resistors.
KSO0–15	O	Keyboard output scan lines.
PORT 1	I/O	Port 1 is a general-purpose, 8-bit bidirectional port with internal pull-ups. It also supports the following user-selectable functions:
P10/A0–P17/A7		P10–P16 are available for connection to dedicated keyboard inputs. A0–A7 output the low-order address byte (refer to LOADREN signal).
LOADREN	I	Low address enable. When set high, address bits A0–A7 are output on P10–P17.
PORT 2	I/O	Port 2 is a general-purpose, 8-bit bidirectional port with internal pull-ups on P20–6/A8–14. It also supports the following user-selectable functions:
P20–6/A8–14		P20–6/A8–14 output the high-order address byte.
P27/LED4		P27/LED4 is available as a fifth LED output driver (by writing to the port bit 7).
PORT 3	I/O	Port 3 is a general-purpose, 8-bit bidirectional port. P32/INT0, P34/T0, P36/WRL, and P37/RDL have internal pull-ups. P30/SIF00, P31/SIF01, P33/SIF10, and P35/SIF11 are high-drive open-drain outputs. It also supports the following user-selectable functions:
P30/SIF00		A high-drive, open-drain output to support an external serial keyboard interface (typically CLK); RXD (8051 UART serial input port); SIF0INTL (serial interface interrupt 0).
P31/SIF01		A high-drive, open-drain output to support an external serial keyboard interface (typically DATA); TXD (8051 UART serial output port).
P32/INT0		INT0L (external interrupt 0).
P33/SIF10		A high-drive, open-drain output to support an external serial keyboard interface (typically mouse CLK); SIF1INTL (external interrupt 1).
P34/T0		AUXOBF1 (output buffer full — mouse support); T0 (Timer/Counter 0 external input).
P35/SIF11		A high-drive, open-drain output to support an external serial keyboard interface (typically mouse DATA); T1 (Timer/Counter 1 external input).

PIN DESCRIPTIONS (Continued)

Table 1. Pin Descriptions (Continued)

Symbol	Type	Description
PORT 3 (Continued)		
P36/WRL		WRL (external data memory write strobe); inactive at addresses 7FF0–7FFFH.
P37/RDL		AUXOBF2 (output buffer full interrupt); INT2L (external interrupt); RDL (external data memory read strobe); inactive at addresses 7FF0–FFFFH.
XTAL1	I	Input to the on-chip oscillator.
XTAL2	O	Output from the on-chip oscillator.
AVGND		Analog ground potential.
AVDD		Analog supply voltage; nominally +5V ±10%.
AIN0–3	I	A/D Analog input channels.
ADB0–7	I/O	External address/data bus. Multiplexes the low-address byte and data during external memory accesses.
EAL	I	External address input. When held high, the 80C51SL CPU executes out of internal Program Memory unless the program counter exceeds 1FFFH. When held low, the 80C51SL CPU always executes out of external memory. EAL is latched on the falling edge of RST.
ALE	O	Address Latch Enable output pulse latches the low address byte during external memory access. ALE is output at a constant rate of 1/6 the oscillator frequency, whether or not there are accesses to external memory. One ALE pulse is skipped during the execution of a MOVX instruction. ALE is disabled during Idle mode and can also be disabled via Configuration register 1 control.
PSENL	O	Program Store Enable is the read strobe to external program memory. PSENL is qualified with RDL and A15 for use with an external Flash memory. PSENL is not active when the device executes out of internal program memory.
MEMCSL	I/O	External Memory Chip Select for code space address 8000H and above, when EAL is inactive (i.e., high). For EAL low, MEMCSL is active. Goes inactive during Idle mode and Power-Down mode. If external memory interfacing is not required, MEMCSL can be configured as a general purpose I/O (controlled via Configuration register 1).
RST	I	Resets the keyboard controller. Hold RST high for two machine cycles.

HOST INTERFACE

The 80C51SL host interface is functionally compatible with the 8042-style host interface. It consists of the PCDB0–7 data bus; the RDL, WRL, A0 and CSL control signals; and the Status register, Input Data register, and Output Data register. Table 2 shows how the interface decodes the control signals. In addition to the above signals, the host interface includes PCOBF, GATEA20, RCL, and the optional AUXOBF1 and AUXOBF2 signals available through firmware configuration of P34/T0 and P37/RDL, respectively.

Table 2. Control Signal Decode (Host Interface)

WRL	RDL	CSL	A0	Operation
0	1	0	0	Write Data to Input Data Register
0	1	0	1	Write Command to Input Data Register
1	0	0	0	Read the Output Data Register
1	0	0	1	Read the Status Register

Host-Interface Registers

The Input Data register, Output Data register, and Status register are each 8 bits wide. Table 3 lists the addresses of the host-interface registers. Figure 3 shows the contents of the Status register.

Table 3. 80C51SL Memory Map for Host-Interface Registers

Register	Address	80C51SL CPU Access
Input and Output Data Registers(1)	7FF1H	R/W
Status Register	7FF2H	R/W(2)
Auxiliary Output Data Register #1(3)	7FF6H	Write Only
Auxiliary Output Data Register #2(3)	7FF7H	Write Only

NOTES:
1. Although the Input and Output Data registers are physically separate, they share address 7FF1H.
2. The 80C51SL CPU cannot write to bits 0, 1 or 3 of the Status register.
3. Alternate Output Data register function.

(MSB) (LSB)

UD	UD	UD	UD	C/D	UD	IBF	OBF
7	6	5	4	3	2	1	0

UD are user-definable.

C/D (Command Data)—This bit specifies whether the input data register contains data or a command (0 = data, 1 = command). During a host write operation, this bit is set to "1" if A0 = 1 or reset to "0" if A0 = 0.

IBF (Input Buffer Full)—This flag is set to 1 whenever the host system writes data into the input data register. Setting this flag activates the 80C51SL CPU's KDINTL interrupt. When the 80C51SL CPU reads the input data register, this bit is automatically reset and the interrupt is cleared.

OBF (Output Buffer Full)—This flag is set to 1 whenever the 80C51SL CPU writes into the data register using one of three addresses: 7FF1H, 7FF6H or 7FF7H. When the host system reads the output data register, the bit is automatically reset.

Figure 3. Status Register

80C51SL-to-Host Communication

The 80C51SL CPU can write to the Output Data register via any of the following addresses: 7FF1H, 7FF6H, or 7FF7H. A write to any of the three addresses automatically sets Bit 0 (OBF) in the Status register. In addition, a unique output flag differentiates the three addresses. Table 4 lists the signal that corresponds to each flag. Each flag is automatically set when data is written to the corresponding address.

Table 4. Host-Interface Flags

Address	Flag
7FF1H	PCOBF output signal goes high if, and only if, bit 4 of Configuration register 1 equals 0.
7FF6H	Port 3, pin 4 output (P34) goes high if, and only if, bit 5 of Configuration register 0 equals 1.
7FF7H	Port 3, pin 8 output (P37) goes high if, and only if, bit 6 of Configuration register 0 equals 1.

Host-to-80C51SL Communication

The host system can send both commands and data to the Input Data register. The 80C51SL differentiates between commands and data by reading the value of Bit 3 of the Status register. When bit 3 is "1", the 80C51SL interprets the register contents as a command. When Bit 3 is "0", the 80C51SL interprets the register contents as data. During a host write operation, Bit 3 is set to "1" if A0 = 1 or reset to "0" if A0 = 0.

Host-Interface Dedicated Outputs

The 80C51SL host-interface provides three dedicated output signals: Output-Buffer Full (PCOBF), GATEA20, and the host "fast" reset, RCL.

PCOBF

The PCOBF signal is an active-high system interrupt which signifies that the 80C51SL CPU has written to the output data register via address 7FF1H. On power-up, after a valid RST pulse has been delivered to the device, PCOBF is reset to 0. PCOBF will normally reflect the status of writes to 7FF1H, if bit 4 of Configuration register 1 equals 0.

Additional flexibility has been added which allows firmware to directly control the PCOBF output signal, independent of data transfers to the host-interface data output register. This feature allows the 80C51SL to be operated via the host "polled" mode. This firmware control is active when PCOBFEN is high and firmware can then bring PCOBF high by writing a "1" to the LSB of the 1-bit data register allocated at 7FFDH.

This register is also readable; residual bits 1–7 will return a "0" on the readback. The value read back on bit 0 of the register always reflects the present value of the PCOBF output. If PCOBFEN = 1, then this value reflects the output of the firmware latch at 7FFDH. If PCOBFEN = 0, then the value read back reflects the in-process status of write cycles to 7FF1H (i.e., if the value read back is high, the host interface output data register has just been written to).

GATEA20 HARDWARE SPEED-UP

The 80C51SL contains on-chip logic support for the GATEA20 hardware speed-up feature. GATEA20 from the 80C51SL is part of the control required to mask address line A20 to emulate 8086 addressing.

In addition to the ability for the host to control the GATEA20 output signal directly, a configuration bit called "SAEN" (Software Assist Enable, bit 7 of Configuration register 0) is provided; when set, SAEN allows firmware to control the GATEA20 output.

When SAEN is set, a 1-bit register assigned to address 7FFBH controls the GATEA20 output. The register bit allocation is shown in Figure 4.

D7							D0
x	x	x	x	x	x	x	GATEA20

Figure 4. Register Bit Allocation

Writing a "0" into location D0 causes the GATEA20 output to go low, and vice versa. When the register at location 7FFBH is read, all unused bits (D7–D1) are tied low.

Host control and firmware control of GATEA20 affect two separate register elements. Readback of

GATEA20 through the use of 7FFBH reflects the present state of the GATEA20 output signal: if SAEN is set, the value read back corresponds to the last firmware-initiated control of GATEA20; if SAEN is reset, the value read back corresponds to the last host-initiated control of GATEA20.

Host control of the GATEA20 output is provided by the hardware interpretation of the "GATEA20 sequence" (see Table 5). The foregoing description assumes that the SAEN configuration bit is reset.

When the 80C51SL receives a "D1" command followed by data (via the host interface), the on-chip hardware copies the value of data bit 1 in the received data field to the GATEA20 host latch. At no time during this host-interface transaction will PCOBF or the IBF flag (bit 1) in the Status register be activated; i.e., this host control of GATEA20 is transparent to firmware, with no consequent degradation of overall system performance. Table 5 details the possible GATEA20 sequences and the 80C51SL responses.

On receiving an external hardware reset via the RST pin or a soft reset via the dedicated address 7FF0H (see the "Soft Reset" section), GATEA20 will be set. Internally sourced resets, such as those initiated by a host write sequence during Power-Down mode, will have no effect on the GATEA20 output.

An additional level of control flexibility is offered via a memory-mapped asynchronous set and reset capability. Any data written to 7FFEH causes the GATEA20 host latch to be set, while any data written to 7FFFH causes it to be reset. This control mechanism should be used with caution. It was added to augment the "normal" control flow as described above—not to replace it. Since the host and the firmware have asynchronous control capability of the host latch via this mechanism, a potential conflict could arise. Therefore, after using the 7FFEH and 7FFFH addresses, firmware should read back the GATEA20 status via 7FFBH (with SAEN = 0) to confirm the actual GATEA20 response.

Table 5. GATEA20 Command/Data Sequence Examples

A0	R/W	PCDB0-7	IBF Flag	GATEA20	Comments
1	W	D1	0	Q	Valid GATEA20
0	W	DF	0	1	Turn-on Sequence
1	W	FF	0	Q	
1	W	D1	0	Q	Valid GATEA20
0	W	DD	0	0	Turn-off Sequence
1	W	FF	0	Q	
1	W	D1	0	Q	Multiple D1 Trigger
1	W	D1	0	Q	Turn-on Sequence*
0	W	DF	0	1	
1	W	FF	0	Q	
1	W	D1	0	Q	Multiple D1 Trigger
1	W	D1	0	Q	Turn-off Sequence*
0	W	DD	0	1	
1	W	FF	0	Q	
1	W	D1	0	Q	Invalid Sequence
1	W	*XX***	1	Q	
1	W	FF	1	Q	

NOTES:
All examples assume that the SAEN configuration bit is 0.
"Q" indicates the bit remains set at the previous state.
*Not a standard sequence.
***XX* = Anything except D1.

RCL HARDWARE SPEED-UP

RCL is the system reset output. In a similar manner to the GATEA20 control structure, RCL may be controlled via firmware or via direct hardware interpretation of the host reset command (FE). A dedicated, programmable counter is provided in hardware, which allows the RCL active pulse width to be correctly sized. This 7-bit down counter is allocated to address 7FF9H within the 80C51SL memory map.

If the 80C51SL receives an FE command byte over the host interface, one of two responses can be configured via firmware to occur:

1. If bit 1 in Configuration register 1 (HARSTEN) is set, then immediately on receiving the FE command, the 80C51SL output RCL will go active. PCOBF and the IBF status flag (bit 1 of the Status register) will remain unaffected by the transaction; i.e., when HARSTEN is set, the FE command is transparent to firmware. RCL will remain low until the pre-programmed 7-bit counter times out, at which point RCL will return to its inactive high state.
2. If HARSTEN is reset, then the FE command will be processed in the conventional way; i.e., IBF status flag and PCOBF(1) will both be automatically forced high, and it is up to firmware to control the RCL response via the 1-bit register element allocated to address 7FFA within the 80C51SL memory map. The bit assignment for this register is shown in Figure 5.

Bit 7 ... Bit 0

X	X	X	X	X	X	X	RCL

Figure 5. Register Bit Allocation

If bit 0 is set, then RCL = 1 and vice versa. The register is also readable, and any read cycle will show the unused bits (7–1) tied low. The value read back on bit 0 is determined by the state of HARSTEN: if HARSTEN is high, the value read back will reflect the status of hardware FE interpretation; if the HARSTEN bit is low, the value read back will reflect the present status of the firmware-controlled register at 7FFAH. In either case, the value read back on bit 0 corresponds to the present value on RCL.

When HARSTEN is low, it is firmware's responsibility to time the RCL pulse width; i.e., when HARSTEN is low, the RCL active low pulse width is independent of the programmable 7-bit counter. When HARSTEN is high, however, the active low pulse width on RCL is dependent on the data loaded into the counter before the FE command is received. The following calculation may be used to determine the pre-load value for a given desired output pulse width.

$$\text{Load Value} = \frac{\text{Desired Pulse Width}}{T}$$

where T = clock or external crystal period.

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For example, assuming a 16 MHz external crystal (or clock source) and assuming we require the nominal 6 μs pulse width:

$$\text{Load Value} = \frac{6 \times 10^{-6}}{62.5 \times 10^{-9}} = 96 \text{ DEC} = 60 \text{ HEX}$$

The down counter is set when the 80C51SL receives an active RST or firmware-initiated reset via an active write cycle to 7FF0H.

When HARSTEN is set and the 7-bit counter times out, the counter is automatically reloaded with the pre-loaded data that was written to 7FF9H prior to the FE transaction. If the RCL output is therefore to be controlled by this mechanism, the firmware **must** pre-load the counter to the desired value at least once prior to any reception of the FE command. Further loads are not then required unless the 80C51SL receives an active reset via RST or a software-initiated reset.

KEYBOARD SCAN

The interface to the keyboard scan logic includes 16 slew-rate-controlled, open-drain scan-out lines (KSO0–15) and eight Schmitt Trigger sense lines (KSI0–7) with internal pull-up resistors. KSI0–7 connect directly to Port 0 of the 80C51SL CPU. The 16 scan-out lines are controlled by the four low-order bits of Port 0 (see Table 6). Together KSO0–15 and KSI0–7 form a keyboard matrix.

NOTE:
1. Bit 4 of Configuration register 1 (PCOBFEN) must be set for this to occur.

Table 6. Keyboard Matrix Decode

Port 0				Keyboard Scan Out Lines KSO15–KSO0
P03	P02	P01	P00	
0	0	0	0	1111111111111110
0	0	0	1	1111111111111101
0	0	1	0	1111111111111011
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1	1	1	0	1011111111111111
1	1	1	1	0111111111111111

Since the KSO0–15 outputs are a decode of the low order Port 0 nibble, the outputs can be expected to glitch during a normal binary code control sequence. In the pre-programmed part, however, the firmware uses a "grey" code sequence, thus effectively eliminating this potential noise source. Because of this strategy, however, the part will follow a non-standard matrix sequence when viewed at the KSO15–0 outputs in normal operation. Table 7 shows the sequence of activated KSO output lines in normal operation for the 80C51SL.

Table 7. KSO Output Line Sequence

KSO0	followed by KSO13
followed by KSO1	followed by KSO15
followed by KSO3	followed by KSO14
followed by KSO2	followed by KSO10
followed by KSO6	followed by KSO11
followed by KSO7	followed by KSO9
followed by KSO5	followed by KSO8
followed by KSO4	followed by KSO0
followed by KSO12	etc.

Keyboard Interrupt Logic

If Bit 1 of the Configuration register 0 is set to "1", the KSO0–15 lines are simultaneously driven low and the Keyboard Scan Logic will generate the KDINTL interrupt if one or more of the KSI0–7 lines goes low. If Bit 1 is reset to "0", then a low level on KSI0–7 will not generate an interrupt and a firmware service routine can poll the KSI0–7 lines to detect a transition.

DEDICATED INPUT KEYS

Bits 0–6 of Port 1 are available as inputs for dedicated keys. The keyboard interrupt logic can be configured to generate the KDINTL interrupt whenever a key depression is detected on one of these dedicated keys. To enable this interrupt feature, set Bit 2 of the Configuration 0 register to "1". The KSO15–0 outputs are unaffected by the state of this configuration bit. KDINTL is configured as an edge-sensitive interrupt. Any falling edge on either KSI7–0 or P16–0, assuming correct setting of the configuration bits as explained earlier, will cause the 80C51SL core to receive the active KDINTL interrupt.

LED DRIVERS

The 80C51SL has four dedicated high-drive, open-drain, LED drivers (LED0–3). These drivers connect to Bits 4–7 of the 80C51SL internal Port 0.

Bit 7 of Port 2 can be configured as a fifth high-drive, open-drain LED driver. Writing a 0 to the appropriate port bit will cause the associated LED output to go low. During and after an external or firmware-initiated reset, the LED outputs (including P27) will be high until firmware writes to the appropriate port.

EXTERNAL KEYBOARD AND MOUSE INTERFACE

Industry-standard PC-AT-compatible keyboards employ a two-wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the 80C51SL provides four signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The 80C51SL has four high-drive, open-drain output(1), bidirectional port pins that can be used for external serial interfaces, such as ISA external keyboard and PS/2-type mouse interfaces. They are P30/SIF00, P31/SIF01, P33/SIF10, and P35/SIF11. P33/SIF10 is connected to the firmware-configurable level/edge sensitive INTL interrupt pin of the 80C51SL CPU. P30/SIF00 is connected to the edge-sensitive SIF0INTL interrupt pin of the 80C51SL CPU.

NOTE:
1. External pull-ups may be required.

The serial clock lines, P30/SIF00 and P33/SIF10, are inhibited (driven low) by hardware during and immediately after an external or firmware-initiated reset. This is so that any power-on self-test completion code transmitted from the serial keyboard will not be missed by the 80C51SL due to power-up timing mismatches. It is however, necessary to write a "0" to these pins immediately after power-up in order to release the hardware inhibit function. If the external keyboard or mouse is not required, P30/SIF00, P31/SIF01, P33/SIF10, and P35/SIF11 can be used as general-purpose I/O pins.

PORT STRUCTURES AND OPERATION

All three 80C51SL ports are bidirectional. Each consists of a latch (Special Function Registers P1 through P3), an output driver, and an input buffer. Port 0 of the 80C51SL CPU does not connect to the package pins. It is used internally to drive the keyboard scan logic.

The output drivers of Ports 1 and 2 can be used in accesses to external memory. The 80C51SL provides the LOADREN signal to facilitate external memory interfaces. When the LOADREN signal is high, Port 1 outputs the low byte of the external memory address. If LOADREN is tied low, then the Port 1 signals continue to emit the P1 SFR content. Port 2 outputs the upper seven bits of the high byte of the external address when the address is 15 bits wide and either EAL is tied low or EAL is tied high and Bit 0 (ADDREN) of Configuration register 1 is set. Otherwise, the Port 2 pins continue to emit the P2 SFR content.

During external memory access, the ADB0–7 lines also provide the low byte of the address, time-multiplexed with the data being written or read.

Many of the port pins are multifunctional. In addition to the standard 80C51 alternate functions, the 80C51SL port pins provide additional alternate functions (see Table 8). The alternate functions can be activated only by writing a "1" to the corresponding port bit.

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I/O Configurations

All port pins with the exception of P27/LED4, P30/SIF00, P31/SIF01, P33/SIF10, P35/SIF11 have fixed internal pull-ups and are therefore called "quasi-bidirectional" ports. When configured as inputs, the pins are pulled high by the internal pull-ups and will source current when externally pulled low.

NOTE:
During a 16-bit external Program Memory access, Port 2 outputs the high address byte. In the 80C51, the Port 2 drivers use the strong pull-up during the entire time that they are emitting a "1" on a Port 2 bit. In this instance, the 80C51 weak quasi-bidirectional pull-up condition that normally occurs after two oscillator periods does not occur. Port 1 of the 80C51SL emulates the quasi-bidirectional pull-up condition, not this extended strong pull-up condition.

Table 8. Port Pin Alternate Functions

Port Pin	80C51 Alternate Function	80C51SL Alternate Function
P10–6/A0–6		Output A0–6 Address Bits or Dedicated Keyboard Inputs
P17/A7		Output A7 Address Bit
P20–6/A8–14		Output A8–14 Address Bits
P27/LED4		LED4 Output Driver
P30/SIF00	RXD (Serial Input Port)	SIF00, External Keyboard CLK/SIF0INTL
P31/SIF01	TXD (Serial Output Port)	SIF01, External Keyboard Data
P32/INT0	INT0L (External Interrupt 0)	
P33/SIF10	INT1L (External Interrupt 1)	SIF10, External Auxiliary Mouse CLK/SIF1INTL
P34/T0	T0 (Timer 0 External Input)	AUXOBF1, Auxiliary Output Buffer Full 1
P35/SIF11	T1 (Timer 1 External Input)	SIF11, External Auxiliary Mouse Data
P36/WRL	WRL (External Data Memory Write Strobe)	
P37/RDL	RDL (External Data Memory Read Strobe)	AUXOBF2, Auxiliary Output Buffer Full 2, INT2L (External Interrupt 2)

80C51SL POWER MANAGEMENT

The 80C51SL uses low power CHMOS and provides support for two further power-saving modes, available when inactive: Idle mode, typically between keystrokes; and Power-Down mode, upon command from the host. A four-channel, eight-bit A/D converter is also included for power management (i.e., battery voltage monitoring, etc.).

Idle Mode

Idle mode is initiated by an instruction that sets the PCON.0 bit (SFR address 87H) in the 80C51SL. In Idle mode, the internal clock signal to the 80C51SL CPU is gated off, but not to the Interrupt Timer and Serial Port functions. The 80C51SL CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data. The port pins hold the logical levels they had when Idle mode was activated. ALE and PSENL are held high. If an A/D conversion is in process when Idle mode is entered, any conversion results may contain erroneous data.

There are two ways to terminate Idle mode. First, activation of any enabled interrupt will cause the PCON.0 bit to be cleared by hardware. The interrupt will be serviced and, following the RETI, the CPU will resume operation by executing the instruction following the one that put the CPU into Idle mode.

The second way to terminate the Idle mode is with a hardware reset. Note that in the 80C51SL, a hardware reset will clear the registers. The 80C51SL CPU will not resume program execution from where it left off.

During Idle mode, MEMCSL, ALE, and PSENL will all be forced high. MEMCSL will not go high if MEMCSL is being used as a general-purpose I/O (i.e., if bit 2 or 3 in Configuration register 1 is high).

Power-Down Mode

Power-Down mode is initiated by an instruction that sets bit PCON.1 in the 80C51SL CPU. When the 80C51SL enters Power-Down mode, all internal clocks, including the 80C51SL core clock, are turned off. If an external crystal is used, the internal oscillator is turned off. MEMCSL, the external memory select signal, goes inactive (high) unless it is configured as a general-purpose I/O (i.e., unless bit 3 of Configuration register 1 is "1"). ALE and PSENL are both forced low. RAM contents are preserved.

PROGRAMMABLE RESET TIMER

The on-chip oscillator (if used with an external crystal) requires at least 10 ms to stabilize after initial power-up or when exiting the Power-Down mode. Even if the 80C51SL is driven from an external clock source (i.e., no crystal) the 80C51SL core specifies the minimum pulse width duration of a reset to be ≥ 24 clock cycles.

The 80C51SL includes a fully programmable reset counter which, when correctly configured, ensures that any internally sourced reset signal delivered to the 80C51SL core is at least 10 ms in duration. It is the user's responsibility to ensure that any externally sourced reset signal (via the RST pin) also meets the 10 ms pulse width specification on power-up or when exiting the Power-Down mode.

The 80C51 CPU drives a divide-by-32 pre-scaler, which in turn drives the Programmable Reset counter.(1) The firmware must preload the program counter with a 16-bit value before invoking the Power-Down mode. The counter resides at the following addresses: Low Byte, 7FF3H; High Byte, 7FF4H. The preload value depends upon the clock frequency and clock source, as explained below.

EXITING POWER-DOWN MODE

If the Programmable Reset counter is correctly configured and if Configuration register 0 is prefigured properly (i.e., if bits 1–4 are set as described in figure 12 in the "Configuration Registers" section), the following situations will automatically terminate Power-Down mode.(2)

NOTES:
1. The divide-by-32 pre-scaler ensures that even with the programmable reset counter loaded with 0000H, the reset delivered to the 80C51SL core is at least 24 clock cycles wide. (Due to the nature of the internal hardware, the actual pulse width of the reset pulse delivered to the 80C51SL is 34 clock cycles wide.)
2. Only the 80C51SL core processor and its SFR peripherals will receive the reset pulse thus generated; on-chip logic, such as the configuration registers, host registers, GATEA20, and fast reset (RCL) logic will remain unaffected.

- A host data/command Write sequence to the Host Interface.(1)
- An input key depression sensed via KSI0-7 or P10-6/A0-6.
- A high to low transition on P32/INT0 while EXTINTEN (config. reg. 0, bit 4) is set. P32/INT0 must be high before entering Power-Down mode.

The 80C51SL device outputs will respond in the following manner on exiting the Power-Down mode:

GATEA20	= Q(3)
RCL	= Q
PCOBF	= Q
MEMCSL	= Q, if MEMCSL is used as a general-purpose I/O = 0, otherwise
KSO15	= 0
KSO0-14	= high impedance (open drain)
P27	= high impedance
LED0-3	= high impedance
P20-6	= high order address, if EAL = 0 = weak high, if EAL = 1
P30/SIF00	= open drain
P33/SIF01	= open drain
P31/SIF01	= open drain
P35/SIF11	= open drain
P32/INT0	= weak high
P34/T0	= weak high
P36/WRL	= weak high
P37/RDL	= weak high
PCDB0-7	= high impedance
P10-7	= weak high, if LOADREN = 0 = low order address, if LOADREN = 1

A Power-Down status flag (PDFLAG) on Bit 0 of the Configuration register 0 can be set by firmware before entering Power-Down mode. Only an externally generated reset pulse on the RST input or a firmware "soft" reset will reset the PDFLAG bit; an internally-sourced reset signal from the Programmable Reset counter has no effect on the PDFLAG bit. After a reset occurs, the 80C51SL CPU can read the value of the PDFLAG bit to determine whether the reset source was internal or external.

NOTES:
1. There are two important exceptions to this. If the SAEN bit in Configuration register 0 is reset to "0", the device will ignore the "D1" GATEA20 sequence with respect to exiting power-down mode. Similarly, if the HARSTEN bit in Configuration register 1 is set to "1", the device will ignore an "FE" command with respect to exiting power-down mode.
2. Bit 4 of Configuration Register 0 must be "1" for this to occur.
3. Where Q = Quiescent; i.e., no change as a result of exiting power-down mode.
4. All inputs without internal pull-ups and floating I/Os must be driven to a known state.

External Crystal Oscillator

When an external crystal is the clock source for the 80C51SL, the reset pulse width must be 10 ms or greater to allow the internal oscillator to stabilize. The pulse-width requirement applies to both internally and externally generated reset signals.

10

Use the following formula to calcuate the appropriate preload value for the Programmable Reset counter:

Preload value = $[(10 \times 10^6)/32]/TPERIOD$

The following examples calculate the Programmable Reset counter preload value for two different clock frequencies.

EXAMPLE 1

Assume that the clock frequency = 2 MHz.

TPERIOD = 1/2M = 500 ns

preload value = $[(10 \times 10^6)/32]/500$
= 625 DEC
= 0271 HEX

EXAMPLE 2

Assume that the clock frequency = 16 MHz.

TPERIOD = 1/16M = 62.5 ns

preload value = $[(10 \times 10^6)/32]/62.5$
= 5000 DEC
= 1388 HEX

External Clock Signal

The 80C51SL clock source can be an externally generated clock signal instead of a crystal oscillator. Connect the clock signal to the XTAL1 input. When an external clock signal is the clock source for the 80C51SL, the reset pulse must last for at least 24 clock periods. The pulse-width requirement applies to both internally and externally generated reset signals. Preload 0000H into the Programmable Reset counter before entering Power-Down mode. This value will cause the Programmable Reset counter to deliver a 34-clock-period reset pulse to the 80C51SL core.

Interrupts

The 80C51SL provides the five standard 8051 interrupts (Group 0) and five expansion interrupts (Group 1). Three of the five expansion interrupts are dedicated to internal functions. Two are available for serial interface interrupt sources. Table 9 describes the interrupts.

The Group 0 interrupts use the standard 8051 interrupt enable and priority structures. Each interrupt is individually enabled or disabled by setting or clearing a bit in the Interrupt Enable (IE) register (SFR location A8H). Each interrupt is programmed to one of two priority levels by setting or clearing a bit in the Interrupt Priority (IP) register (SFR location B8H). See the "Hardware Description of the 8051, 8052, and 80C51" in the *8-Bit Embedded Controller Handbook* for more details.

Group 0 interrupts (which are identical to the standard 80C51 interrupts) are configurable as either level- or edge-sensitive. Consult the *Embedded Microcontroller and Processor Handbook* for a full description.

The Group 1 Interrupt Enable register (IE1) is a bit-addressable Special Function Register that resides at SFR address 0E8H. Bits 0 through 4 are the individual enable bits for the Group 1 Interrupts. Bit 7 is the global enable bit for the group. Figure 6 shows the contents of the IE1 register.

The Group 1 Priority Register (IP1) is a bit-addressable Special Function Register that occupies SFR address 0F8H. Setting or clearing individual bits in the IP1 register selects the priority level of each Group 1 interrupt source. Figure 7 shows the contents of the IP1 register.

KDINTL and SIF0INTL have been configured in hardware as edge-sensitive interrupts. A falling edge on any of the KSI7–0 or P10–6 inputs (assuming an appropriate configuration register setup) will cause KDINTL to go active. Similarly, a falling edge on P3.0 will cause SIF0INTL to go active. The other interrupts in Group 1 are configured as level-sensitive interrupts.

For those users who intend to generate their own 80C51SL firmware, care should be taken to ensure that all interrupts remain disabled during the "configuration setup," as spurious interrupts may be generated when Port 3 is configured.

Table 9. Interrupt Sources

Interrupt	Description	Pin(1)	Vector Address	Polling Order	Active
Group 1					
KDINTL	Keystroke Detect	—	0043H	1	E
IBFINTL	Input Buffer Full	—	004BH	2	L
ADINTL	A/D Conversion Complete	—	0053H	3	L
SIF0INTL	Serial Interface	P30	005BH	4	E
INT2L	External Interrupt	P37	0063H	5	L
Group 0					
INT0L	External Interrupt (EI0)	P32	0003H	6	L/E
T0IINTL	Timer 0 Interrupt (TF0)	P34	000BH	7	—
SIF1INTL	Serial Interface (EI1)	P33	0013H	8	L/E
T1INTL	Timer 1 Interrupt (TF1)	P35	001BH	9	—
SCIINTL	Serial Port Interrupt (RI + TI)	—	0023H	10	E

NOTES:
L = Level-sensitive, E = Edge-sensitive
Timer interrupts occur when the count rolls over from all 1's to all 0's.

(1)These pins are mapped directly to the corresponding core input pins. For example, a negative edge on pin P32 will cause a negative edge on the core interrupt pin, INT0L.

INTERRUPT POLLING SEQUENCE

When two or more interrupts with the same priority level become active during the same machine cycle, the 80C51SL's internal polling sequence determines the service order. If all ten interrupts are set to the same priority level, and all interrupts become active during the same machine cycle, the 80C51SL CPU services the interrupts in the order shown in Table 9. When Group 0 and 1 interrupts are assigned to the same priority, Group 1 interrupts have priority.

(MSB) (LSB)

EA1	x	x	IN4	IN3	IN2	IN1	IN0
7	6	5	4	3	2	1	0

EA1 is the global enable bit
- EA1 = 0 disables all five additional interrupts (IN0–IN4)
- EA1 = 1 setting or clearing the appropriate IN*x* bit individually enables or disables each Group 1 interrupt

x not implemented, reserved for future use.*

IN4 enables or disables the INT2L interrupt
- IN4 = 1 enables INT2L
- IN4 = 0 disables INT2L

IN3 enables or disables the SIF0INTL interrupt
- IN3 = 1 enables SIF0INTL
- IN3 = 0 disables SIF0INTL

IN2 enables or disables the ADINTL interrupt
- IN2 = 1 enables ADINTL
- IN2 = 0 disables ADINTL

IN1 enables or disables the IBFINTL interrupt
- IN1 = 1 enables IBFINTL
- IN1 = 0 disables IBFINTL

IN0 enables or disables the KDINTL interrupt
- IN0 = 1 enables KDINTL
- IN0 = 0 disables KDINTL

NOTE:
*User software should not write 1's to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and it's active value will be 1. The value read from a reserved bit is indeterminate.

Figure 6. IE1—Group 1 Interrupt Enable Register

(MSB)							(LSB)
x	x	x	PN4	PN3	PN2	PN1	PN0
7	6	5	4	3	2	1	0

x not implemented, reserved for future use.*

PN4 defines the INT2L interrupt priority level
PN4 = 1 programs INT2L to the high priority level
PN4 = 0 programs INT2L to the low priority level

PN3 defines the SIF0INTL interrupt
PN3 = 1 programs SIF0INTL to the high priority level
PN3 = 0 programs SIF0INTL to the low priority level

PN2 defines the ADINTL interrupt
PN2 = 1 programs ADINTL to the high priority level
PN2 = 0 programs ADINTL to the low priority level

PN1 defines the IBFINTL interrupt
PN1 = 1 programs IBFINTL to the high priority level
PN1 = 0 programs IBFINTL to the low priority level

PN0 defines the KDINTL interrupt
PN0 = 1 programs KDINTL to the high priority level
PN0 = 0 programs KDINTL to the low priority level

NOTE:
*User software should not write 1's to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and it's active value will be 1. The value read from a reserved bit is indeterminate.

Figure 7. IP1—Group 1 Interrupt Priority Register

A/D Converter

The 80C51SL includes a four-channel, eight-bit analog-to-digital converter. This A/D, with eight bits of accuracy, uses successive approximation with a switch capacitor comparator(1). It is designed to be used for sampling static analog signals (i.e., ideally suited for power management tasks, such as battery voltage monitoring, etc.). Differential nonlinearity is specified at ±0.5 LSB, with an integral nonlinearity of ±1.0 LSB. The nominal conversion rate is 20 μs at 16 MHz. The analog, high and low voltage references are connected to AVDD and AVGND, respectively. The four input channels, AIN0–3 are connected from the package pins, unbuffered, to an analog multiplexer (on-chip). Thus, the input leakage is low (<10 μA) and the input impedance is high.

A/D SFR REGISTERS

The A/D has three internal registers: ADCON, ADRES, and ADLSB. The registers map into SFR addresses C8H, C9H, and CAH.

ADCON Register—The ADCON register functions as both a write-only control register (see Figure 8) and a read-only status register. The A/D transfers information to the Status register at the start of a conversion. When you **read** the ADCON register, the A/D supplies the status of the current conversion (see Figure 9). If a conversion is not currently in progress, the register contains the status of the last conversion.

(1)The 80C51SL A/D is based upon the 80C196KB's on-chip A/D converter.

(MSB)							(LSB)
x	x	x	RCS	GO	CH2	CH1	CH0
7	6	5	4	3	2	1	0

x not implemented, reserved for future use.*

RCS determines the number of conversion states (see "Selecting a Conversion Mode")
RCS = 0 normal number of conversion states
RCS = 1 reduced number of conversion states

GO determines whether an A/D conversion can begin
GO = 0 prevents an A/D conversion from taking place
GO = 1 starts an A/D conversion immediately

CH2–CH0 are the channel selection bits. (Select a channel by writing the channel number, in binary, to these bits. Channels 000-011H are available; channels 100–111H are **not** available.)

Figure 8. ADCON—A/D Control Register (Write-Only)

(MSB)							(LSB)
x	x	x	RCS	STA	CH2	CH1	CH0
7	6	5	4	3	2	1	0

x not implemented, reserved for future use.*

RCS contains the current status for the number of conversion states
RCS = 0 normal number of conversion states selected
RCS = 1 reduced number of conversion states selected

STA Is the A/D status bit
STA = 0 A/D is idle
STA = 1 an A/D conversion is in progress

CH2–CH0 contain the current channel selection

NOTE:
*User software should not write 1's to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and it's active value will be 1. The value read from a reserved bit is indeterminate.

Figure 9. ADCON—A/D Status Register (Read-Only)

ADRES Register—The ADRES register contains the result of the most recently completed A/D conversion. After valid data is written to this register, the A/D converter sets the interrupt flag in the ADLSB register (see Figure 10). The results remain valid until the next conversion process begins.

ADLSB Register—The ADLSB register contains the A/D interrupt flag (see Figure 10). At the completion of an A/D conversion, the A/D converter sets the interrupt flag (AIF) in the ADLSB register to "1", which causes the interrupt request line (ADINTL) to go low. Writing to the ADLSB register clears the AIF flag.

(MSB) (LSB)

x	x	x	x	x	x	TST	AIF
7	6	5	4	3	2	1	0

x not implemented, reserved for future use.*

x not implemented, reserved for future use.*

TST is reserved for Intel test purposes

AIF is the A/D interrupt flag
AIF = 0 indicates that a conversion is in progress or the A/D is idle
AIF = 1 is an interrupt request indicating that the A/D conversion is complete

NOTE:
*User software should not write 1's to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and it's active value will be 1. The value read from a reserved bit is indeterminate.

Figure 10. ADLSB—A/D Least Significant Bits Register

SELECTING A CONVERSION MODE

The A/D supports two conversion modes: normal conversion states or reduced conversion states (see Table 10). The conversion mode is selected by programming the Reduced Conversion States (RCS) bit in the ADCON control register (see Figure 8).

Table 10. Conversion Options

Description	Total Conversion Time*	Aperture(1) Time*
Normal Conversion States (RCS = 0)	158	15
Reduced Conversion States (RCS = 1)	91	8

*In 80C51SL states (6 states = 1 machine cycle)

NOTE:
1. The aperture time is the time that the A/D samples AVIN.
AVIN must not vary more than ±0.5 LSB during the aperture time.
1 LSB = VREF/256

Reduced Conversion States—The operating frequency of the 80C51SL determines the proper setting for the RCS bit. When the system clock is 7.5 MHz or greater, **clear** the RCS bit (RCS = 0). When the clock is less than 7.5 MHz, **set** the RCS bit (RCS = 1).

The RCS bit determines the number of aperture time states and the total conversion time states. For designs with slow system clocks, the RCS makes it possible to produce an aperture time and total conversion time that are comparable to those of a system operating at twice the frequency.

The A/D samples the analog input voltage during the aperture time. The longer the aperture time, the lower the maximum allowable frequency of the analog input voltage.

NOTE:
To guarantee accuracy, the analog input voltage must not vary more than ±0.5 LSB during the aperture time.

A design that uses a slow system clock would have an unacceptably long aperture time if the number of sampling states remained constant. Setting the RCS bit reduces the number of aperture states from 15 to 8, which enables the A/D to support a greater maximum analog input frequency.

The total conversion time impacts the accuracy of the conversion because the holding capacitor must retain its charge during the entire conversion time. Setting the RCS bit reduces the total number of conversion states from 158 to 91.

The formulas and example below illustrate the calculations for aperture time, conversion time, and maximum analog input frequency.

Aperture Time Formula

$$\frac{1}{\text{system clock frequency}} \times 2^* \times \text{aperture states}$$

Total Conversion Time Formula

$$\frac{1}{\text{system clock frequency}} \times 2^* \times \text{conversion states}$$

Maximum Analog Input Frequency Formula

$$\frac{(3.9 \times 10^{-3})}{(\text{aperture time} \times \pi)}$$

Example

This example shows the aperture time, conversion time, and maximum analog input frequency for a design with a 16 MHz system clock and the normal number of conversion states selected (RCS = 0).

Aperture Time

$1/16M \times 2 \times 15 = 1.88\ \mu s$

Total Conversion Time

$1/16M \times 2 \times 158 = 19.75\ \mu s$

Maximum Analog Input Frequency

$$\frac{3.9 \times 10^{-3})}{1.88 \times 10^{-6} \times \pi)} = 660\ Hz$$

*2 = periods per state

MEMORY CONFIGURATIONS

The 80C51SL provides 8K of on-chip ROM and 256 bytes of on-chip RAM. It can support up to 32 Kbytes of external data memory and 32 Kbytes of external code memory. If EAL = 1 and the memory address is greater than 8K, the Program Counter automatically switches to external memory.

NOTE:
EAL is latched on the falling edge of reset.

Port 3, Bit 6 is multiplexed with the active-low write strobe (WRL) for those data memory write cycles in the address ranges 0000–7FEFH and 8000–FFFFH. P36/WRL remains high during memory write cycles to internal registers in the address range 7FF0–7FFFH.

Port 3, Bit 7 is multiplexed with the active-low read strobe (RDL) for those data memory read cycles in the address range 0000–7FEFH. P37/RDL remains high during memory read cycles from internal registers in the address range 7FF0–7FFFH. The RDL output is ORed with A15, which assigns the 32 Kbytes of potential external RAM to the lower 32K address space.

The 80C51SL address decode logic is pre-configured to allow the memory maps shown in Figure 11.

The P36/WRL and P37/RDL output signals remain inactive during read and write operations to the memory-mapped register set.

Note that A15 is not available for external addressing. A15 is gated with MEMCSL internal to the 80C51SL, ensuring the MEMCSL is active only when either EAL is low or EAL = 1 and A15 = 1.

PSENL is gated with RDL and A15 coming out of the 80C51 CPU internal to the 80C51SL, such that PSENL will also go active if RDL = 0 and A15 = 1; this facilitates the use of external flash memory.

Refer to Figure 15 in the "Application Example" section for an example of how to connect external memory to the 80C51SL.

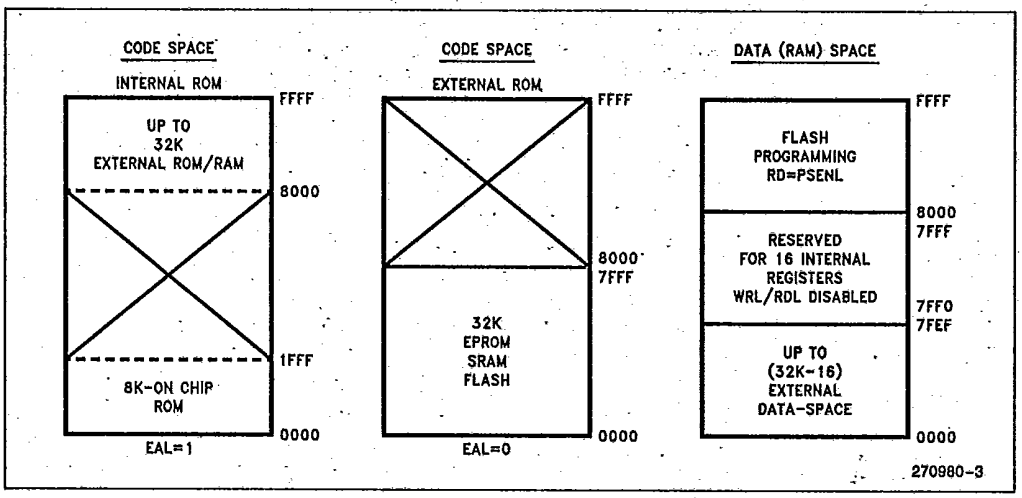

Figure 11. 80C51SL Memory Map

Internal Memory-Mapped Registers

Table 11 describes the internal memory-mapped registers.

Table 11. Internal Memory-Mapped Registers

Address	Register	Read/Write (80C51SL Core)	Comment
7FF0	Soft Reset	W Only	—
7FF1	Host I/F Data Register	R/W	8 bits
7FF2	Host I/F Status Register	R/W	Can't write to Bit 0, 1, or 3
7FF3	Prog. RST Counter Low Byte	R/W	8 bits
7FF4	Prog. RST Counter High Byte	R/W	6 bits (bits 7–6 = 0 on read)
7FF5	Configuration Register 0	R/W	8 bits
7FF6	AUXOBF1 Flag	W Only	1 bit wide
7FF7	AUXOBF2 Flag	W Only	1 bit wide
7FF8	Configuration Register 1	R/W	6 bits (bits 7–6 = 0 on read)
7FF9	System Reset Counter Load	R/W	7 bits (bits 7 = 0 on read)
7FFA	System Reset	R/W	1 bit (bits 7–1 = 0 on read)
7FFB	GATEA20	R/W	1 bit (bits 7–1 = 0 on read)
7FFC	MEMSCL (General Purpose)	R/W	1 bit (bits 7–1 = 0 on read)
7FFD	PCOBF	R/W	1 bit (bits 7–1 = 0 on read)
7FFE	SETGA20L	W Only	any data written to this address causes GATEA20 to be set
7FFF	RSTGA20L	W Only	any data written to this address causes GATEA20 to be reset

Configuration Registers

The 80C51SL has two configuration registers that control optional features. The configuration registers can be read and written by the 80C51SL CPU. Register 0 is an 8-bit wide register that resides at address 7FF5H. Register 1 is a 6-bit wide register that resides at address 7FF8H. Figures 12 and 13 describe each bit in the configuration registers.

Both configuration registers are reset to 0 by an externally applied reset or by a firmware-initiated reset. Internally generated resets (i.e., those causing an exit from Power-Down mode—see the "Power-Down Mode" section) have no effect on the configuration registers.

(MSB) (LSB)

SAEN	AUX2	AUX1	EXTINTEN	EPCIFRST	EP1TDRST	EKTDRST	PDFLAG
7	6	5	4	3	2	1	0

SAEN is the software-assist enable. When set to '1', SAEN allows control of the GATEA20 signal via firmware. If SAEN is reset to '0', GATEA20 corresponds to either the last host-initiated control of GATEA20 or the last firmware write to 7FFE or 7FFFH.

AUX2 is the auxiliary output-buffer-full enable 2. If P37/RDL is configured as an output and this bit is set to '1', then the AUXOBF2 flag is output onto P37/RDL.

AUX1 is the auxiliary output-buffer-full enable 1. If P34/T0 is configured as an output and this bit is set to '1', then the AUXOBF1 flag is output onto P34/T0.

EXTINTEN is the external-interrupt enable. If Power-Down mode is active and this bit is set to '1', the following interrupts will cause the programmable-reset counter to reset the 80C51SL CPU: P30/SIF00, P32/INT0, P33/SIF10, or P37/RDL.

EPCIFRST is the enable host-interface reset. If Power-Down mode is active and this bit is set to '1', any valid write cycle from the host will cause the programmable-reset counter to reset the 80C51SL CPU.

EP1TDRST is the enable Port 1 key-depression-detect reset. When set to '1', any P10–6/A0–6 key depression will generate a KDINTL interrupt during normal system operation or, if the 80C51SL is in Power-Down mode, will cause the programmable-reset counter to reset the 80C51SL CPU.

EKTDRST is the enable key-depression-detect reset. When set to '1', any KSI0–7 input key depression will generate a KDINTL interrupt during normal system operation or, if the 80C51SL is in Power-Down mode, will cause the programmable-reset counter to reset the 80C51SL CPU.

PDFLAG is the Power-Down reset status flag. Firmware can set this bit to '1' before entering the Power-Down mode of operation. The firmware reset routine then polls this status flag to differentiate a reset initiated by the external RST pin from a reset initiated by the programmable reset counter during power-down. Only an externally applied reset, via the RST pin, will affect the contents of this bit.

Figure 12. Configuration Register 0

(MSB) (LSB)

x	x	DISALE	PCOBFEN	MCSLINP	XMENL	HARSTEN	ADDREN
7	6	5	4	3	2	1	0

x	not implemented, reserved for future use.*
DISALE	when high, this bit inhibits ALE output; i.e., ALE will be forced low.
PCOBFEN	when high, PCOBF reflects whatever value was written to the PCOBF firmware latch assigned to 7FFDH. When low, PCOBF reflects the status of writes to 7FF1H (the output data register).
MCSLINP	when high, this allows MEMCSL to be used as a general-purpose input, assigned to bit 0 of address 7FFCH. MCSLINP must be low if external memory is used. When MCSLINP is high, the output buffer is tri-stated.
XMENL	when high, this allows MEMCSL to be used as a general-purpose output. Writing a '1' to 7FFCH wil then cause MEMCSL to go to '1', and vice versa. XMENL should be low when using the 80C51SL with external memory.
HARSTEN	when high, HARSTEN allows direct hardware interpretation of the "FE" host-interface command and allows RCL to be controlled from on-chip hardware. When low, this hardware is disabled and RCL is controlled via the 1-bit register at 7FFAH.
ADDREN	when EAL is tied high and ADDREN is set to '1', the high-order address is gated onto the P20–6 pins. When EAL is tied high and ADDREN is reset to '0', then the P20–6 pins output standard Port 2 data.

NOTE:
*User software should not write 1's to reserved bits. These bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and it's active value will be 1. The value read from a reserved bit is indeterminate.

Figure 13. Configuration Register 1

Special Function Registers

Figure 14 is a map of the on-chip Special Function Register (SFR) space. The 80C51SL provides all standard 80C51 SFRs (see the "Hardware Description of the 8051, 8052 and 80C51" in the *Embedded Microcontroller and Processor Handbook*). It also provides the IP1 and IE1 interrupt control registers and the A/D registers (ADCONA, ADRESA, and ADLSBA A/D). The interrupt control registers are described in the "Interrupts" section and the A/D registers are described in the "A/D Converter" section.

F8H	IP1*								**FFH**
F0H	B*								**F7H**
E8H	IE1*								**EFH**
E0H	ACC*								**E7H**
D8H									**DFH**
D0H	PSW*								**D7H**
C8H	ADCONA	ADRESA	ADLSBA						**CFH**
C0H									**C7H**
B8H	IP*								**BFH**
B0H	P3*								**B7H**
A8H	IE*								**AFH**
A0H	P2*								**A7H**
98H	SCON*	SBUF							**9FH**
90H	P1*								**97H**
88H	TCON*	TMOD	TL0	TL1	TH0	TH1			**8FH**
80H	P0*	SP	DPL	DPH	Res	Res	Res	PCON	**87H**

Notes: First column = Starting address Last column = Ending address
* = Bit-addressable register Res = Reserved for test

Figure 14. SFR Memory Map

DEFAULT RESET CONDITIONS

The 80C51SL has two sources of reset: an external reset via the RST pin, and a firmware-generated, or "soft" reset. An 80C51SL reset from either of these two sources will cause the hardware response shown in Table 12. Note that the values shown are those prior to any resident firmware control.

Soft Reset

For additional flexibility, a firmware-initiated reset mechanism has been added. The effect of this "soft reset" is identical to that of an external reset via the RST pin: the 80C51 core processor and on-chip logic are all reset. This soft reset is invoked by the action of any data written to location 7FF0H. The time duration of the reset pulse applied to the 80C51 core processor and surrounding logic is governed entirely by the contents of the programmable reset counter immediately prior to invocation. It is therefore important for resident firmware to load the programmable reset counter with the appropriate value before writing to address 7FF0H. Since the counter has been preconfigured in hardware to deliver a pulse width greater than 34 clock cycles at all times, it is only necessary to load the counter with 00H immediately before execution of a soft reset. Refer to the "Programmable Reset Timer" section under "80C51SL Power Management."

Table 12. Default Reset Conditions

Description	Reset Condition
Ports	
P10–7/A0–7	If LOADREN = 0, P10–7/A0–7 are driven to a weak high. If LOADREN = 1, P10–7/A0–7 output the low-order address.
P20–6/A8–14	If EAL = 0, P20–6/A8–14 output the high-order address. If EAL = 1, P20–6/A8–14 are driven to a weak high.
P27/LED4	high impedance
P32/INT0, P34/T0, P36/WRL, P37/RDL	weak high
P30/SIF00, P33/SIF10	low(1)
P31/SIF01, P35/SIF11	high impedance (open drain)
Registers	
Configuration reg 0	reset to 0 (all bits)
Configuration reg 1	reset to 0 (all bits)
ADCON	reset to 0 (all bits)
Keyboard Scan	
KSO15	active low
KSO1–14	high impedance (open drain)
LED0–LED3	high impedance (open drain)
Host Interface	
PCOBF	low
GATEA20	high
RCL	high
PCDB0–7	high impedance
External Memory Interface	
ALE	low
PSENL	high
MEMCSL	if EAL = 0, MEMCSL is low. if EAL = 1, MEMCSL is high.
ADB0–7	high impedance during active reset

NOTE:
1. The hardware effectively latches P30/SIF00 and P33/SIF10 to the zero (0) state. Resident firmware must write a '0' to the associated Port 3 output data bits immediately after reset in order to release this latching action.

APPLICATION EXAMPLE

Figure 15 shows a typical system configuration for the 80C51SL. External EPROM or Flash program memory can be used (EAL tied to VSS) until code is ready to be committed to 80C51SL ROM (EAL tied to VCC). Standard 8042 host interface signals (8042CSL, A2, $\overline{WR}$, $\overline{RD}$, and XD Bus) are shown. In addition, fast hardware KBDA20 and $\overline{RC}$ are included. KSO0–15 and KSI0–7 support scanned keyboards, and LED0–4 directly drive five LEDs.

Open drain, bidirectional port pins (AUX DATA, AUX CLK, KBD DATA, and KBD CLK) also directly support an optional, full-sized, standard AT-compatible keyboard and a PS/2-compatible AUX device (typically a mouse). Four channels of an eight-bit A/D are available for power monitoring functions, such as battery voltage monitoring. The 80C51SL is shown connected to a 16 MHz crystal, which is required if the 80C51SL is used to initiate Resume in a 386SL design (with the 80C51SL in Power-Down mode during Suspend).

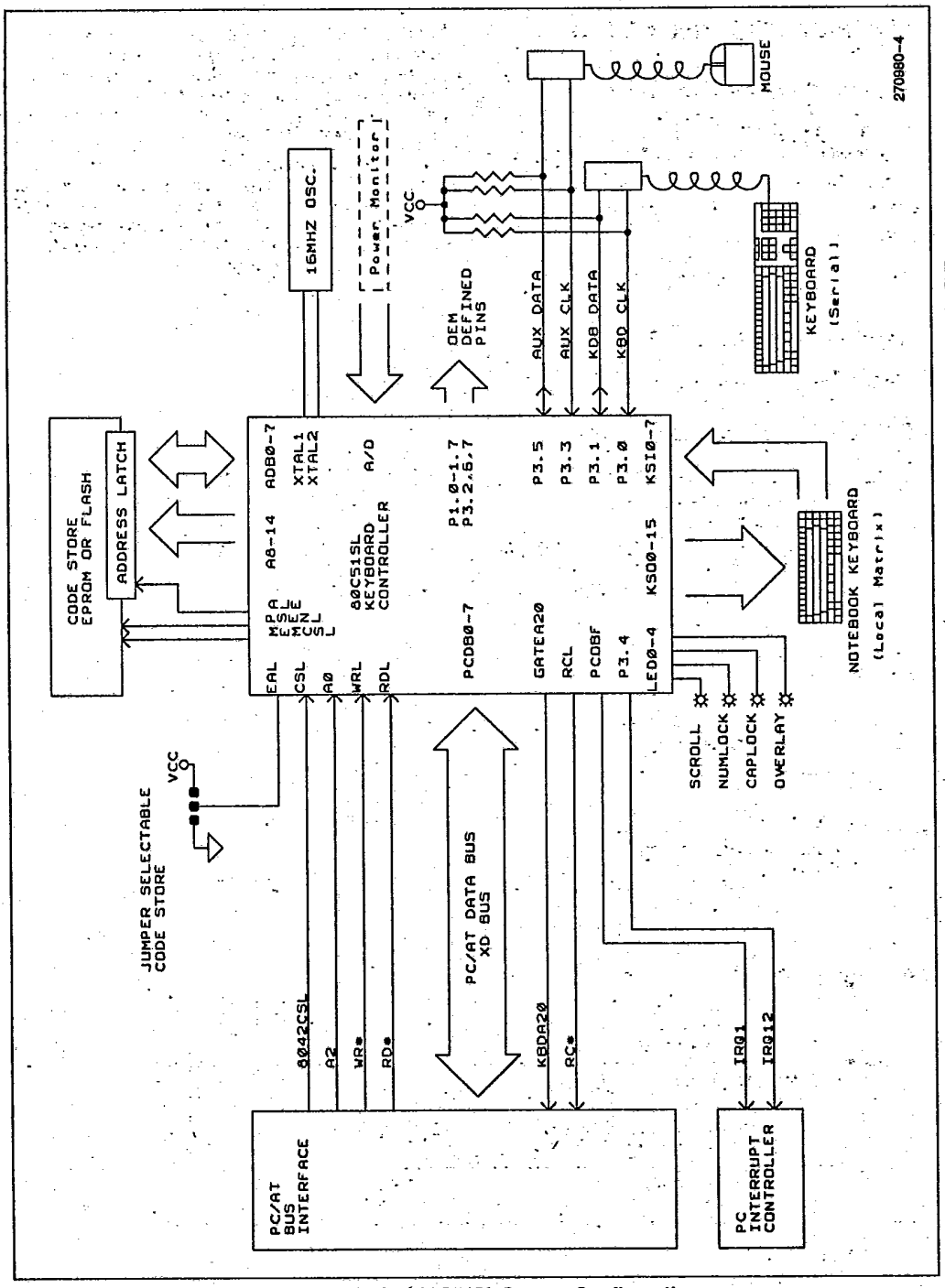

Figure 15. Typical 80C51SL System Configuration

ELECTRICAL SPECIFICATIONS

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

Absolute Maximum Ratings

Ambient Temperature
Under Bias ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin to VSS ... −0.5V to VCC + 0.5V
Power Dissipation 1.0W*
*This value is based on the maximum allowable die temperature and the thermal resistance of the package.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

TA (under Bias) = 0°C to +70°C; VCC = +5V ±10%; VSS = 0V

DC Characteristics (Under Operating Conditions)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage				
	KSI0–7	−0.5	0.8	V	
	BP Pins(1), EAL, CSL, RDL, WRL, A0, LOADREN, MEMCSL	−0.5	0.8	V	
	QB Pins(2), RST, XTAL1	−0.5	0.2 V_{CC} −0.1	V	
	ADB0–7, PCDB0–7	−0.5	1.3	V	
V_{IH}	Input High Voltage				
	KSI0–7	2.0	V_{CC} + 0.5	V	
	BP Pins(1), EAL, CSL, RDL, WRL, A0, LOADREN, MEMCSL	2.0	V_{CC} + 0.5	V	
	QB Pins(2)	0.2 V_{CC} +0.9	V_{CC} + 0.5	V	
	PCDB0–7, ADB0–7, XTAL1, RST	3.5	V_{CC} + 0.5	V	
R_P	Internal Port Resistors				
	KSI0–7	5	20	kΩ	
V_{OL}	Output Low Voltage				
	BP Pins(1) (except P27/LED4)	−0.5	0.4	V	I_{OL} = 16 mA
	P27/LED4, LED0–3	−0.5	0.8	V	I_{OL} = 12 mA
	QB Pins(2)	−0.5	0.4	V	I_{OL} = 4 mA
	ALE, PSENL, PCOBF	−0.5	0.45	V	I_{OL} = 3.2 mA
	PCDB0–7, ADB0–7, GATEA20, RCL, KSO0–15, MEMCSL	−0.5	0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage				
	PCDB0–7, ADB0–7	4.0	V_{CC} + 0.5	V	I_{OH} = −2.0 mA
	QB Pins(2), ALE, PSENL, PCOBF	2.4	V_{CC} + 0.5	V	I_{OH} = −0.08 mA
	RCL, GATEA20, MEMCSL	4.0	V_{CC} + 0.5	V	I_{OH} = −4 mA
I_{IL}	Logical 0 Input Current				
	QB Pins(2)		−50	µA	V_{IN} = 0.45V

DC Characteristics (Under Operating Conditions) (Continued)

Symbol	Parameter	Min	Max	Unit	Test Conditions
I_{LI}	Input Leakage Current All Inputs		±10	µA	$0 < V_{IN} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current QB Pins(2)		−650	µA	$V_{IN} = 2.0V$
I_{CC}	Power Supply Current (See Note 1) Running at 16 MHz Idle Mode at 16 MHz (See Note 3) Power-Down Mode		 38 10 100–150	 mA mA µA	 (See Note 4) (See Note 6) (See Note 7)

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NOTES:
1. Bidirectional (BP) pins include P27/LED4, P30/SIF00, P31/SIF01, P33/SIF10 and P35/SIF11.
2. Quasi-bidirectional (QB) pins include P20–6/A8–A14, P32/INT0, P34/T0, P36/WRL, P37/RDL and P10–7/A0–7.
3. These values are based upon the 80C52 (which is similar) and are not guaranteed.
4. I_{CC} test condition for Active mode is XTAL1 driven with a clock signal, all other inputs driven high, and all outputs disconnected. All power and ground pins are connected, including AVDD and AVGND.
5. Idle mode between keystrokes should be typical case for power consumption.
6. I_{CC} test condition for Idle mode is control signal inputs are driven inactive, ports 1 and 3 are driven low and ADB, PCDB and P27/LED4 are driven high.
7. I_{CC} test condition for Power-Down mode is the same as for Idle mode, except XTAL1 is grounded (i.e., no clock signal applied). Note that minimum V_{CC} for Power-Down mode is 2.5V.
8. P27/LED4, P30/SIF00, P31/SIF01, P33/SIF10, P35/SIF11, KSO0–15, LED0–3 are open drain outputs.
9. KSO0–15, P27/LED4, LED0–3, and MEMCSL are slew-rate-controlled outputs.

AC Characteristics

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has three or five characters. The first character is always "T" (for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. Table 13 lists the characters and their meanings.

Example

TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to PSEN Low.

Table 13. AC Symbol Characters

Char.	Meaning
A	Address
C	Clock
D	Input Data
H	Logic level HIGH
I	Instruction (program memory contents)
L	Logic level LOW, or ALE
P	PSENL
Q	Output data
R	RDL signal
T	Time
V	Valid
W	WRL signal
X	No longer a valid logic level
Z	Float

Host-Interface Timing

All outputs loaded with 100 pF

Symbol	Parameter	Min	Max	Units
TAR	CSL, A0 Setup to RDL ↓	0		ns
TRA	CSL, A0 Hold after RDL ↑	0		ns
TAD	RDL to Data Out		80	ns
TAW	CSL, A0 Setup to WRL ↓	0		ns
TWA	CSL, A0 Hold after WRL ↑	0		ns
TDW	Data Setup to WRL ↑	20		ns
TWD	Data Hold after WRL ↑	0		ns
TWW	Minimum Pulse Width of WRL	50		ns

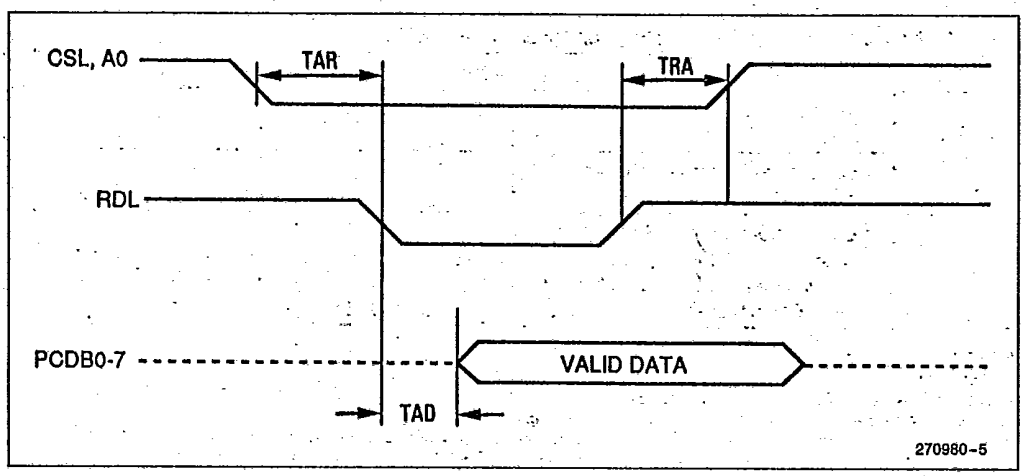

Figure 16. Host-Interface Read

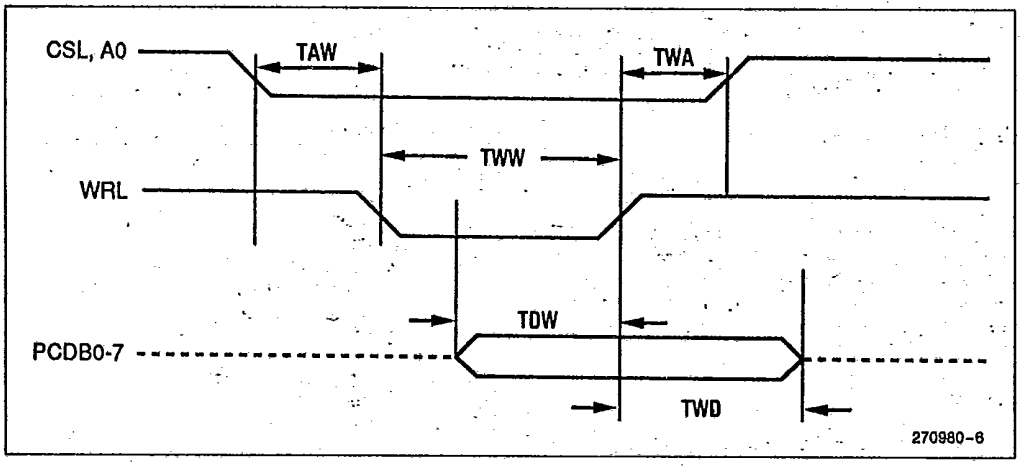

Figure 17. Host-Interface Write

External Memory Timing

TCLCL = 1 clock period
All outputs loaded with 50 pF

Symbol	Parameter	Min	Max	Units
TAVLL	Address Valid to ALE ↓	TCLCL		ns
TLLAX	Address Hold after ALE ↓	TCLCL		ns
TLLIV	ALE ↓ to Valid Instr In		4TCLCL − 50	ns
TPLIV	PSENL ↓ to Valid Instr In		3TCLCL − 50	ns
TPXIX	Input Instr Hold after PSENL ↑	0		ns
TAVIV	Address to Valid Instr In		5TCLCL − 50	ns
TWLWH	P36/WRL Pulse Width	6TCLCL		ns
TRLDV	P37/RDL ↓ to Valid Data In		5TCLCL − 50	ns
TRHDX	Data Hold after P37/RDL	0		ns
TLLDV	ALE ↓ to Valid Data In		8TCLCL − 50	ns
TAVDV	Address to Valid Data In		9TCLCL − 50	ns
TQVWX	Data Valid to P36/WRL ↓	TCLCL		ns
TWHQX	Data Hold after P36/WRL ↑	TCLCL − 20		ns
TMVDV	MEMCSL to Valid Data In		9TCLCL − 50	ns
TMVIV	MEMCSL to Valid Instr In		5TCLCL − 50	ns

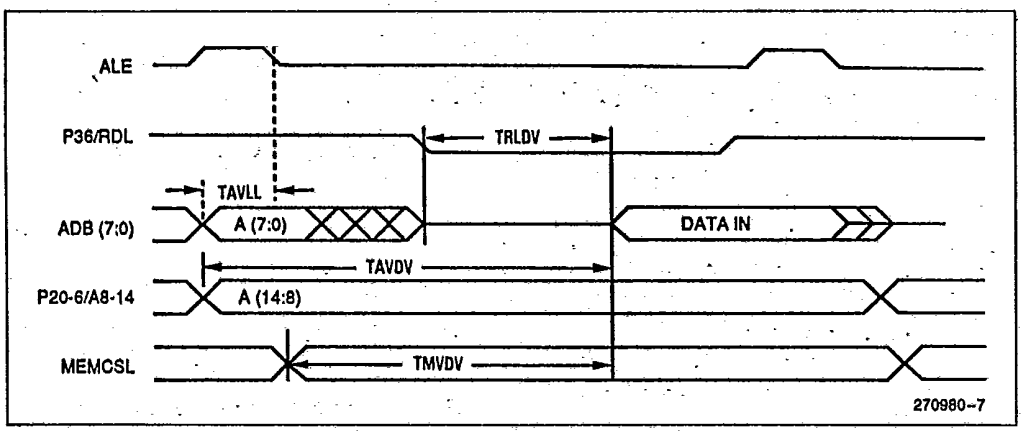

Figure 18. External Data Memory Read

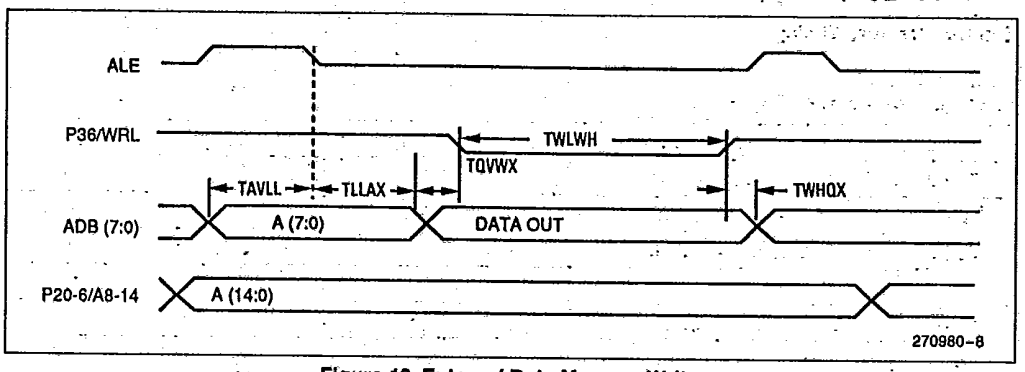

Figure 19. External Data Memory Write

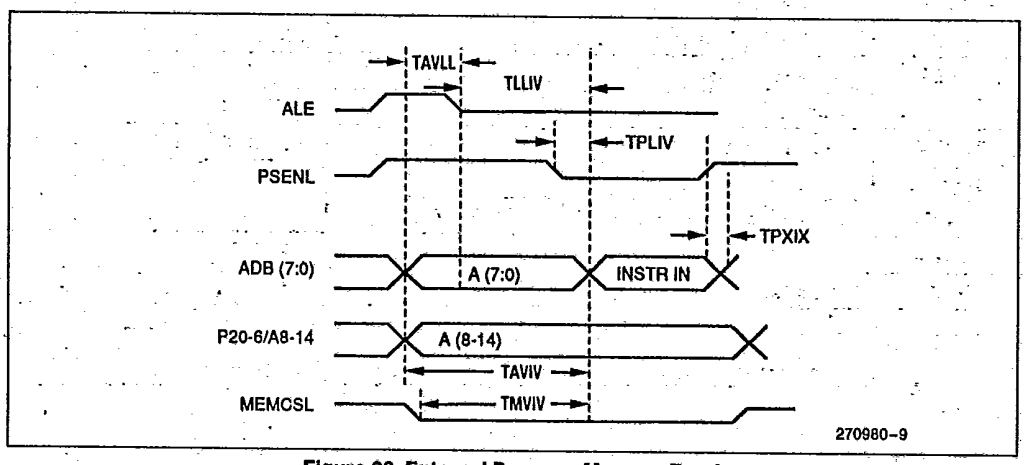

Figure 20. External Program Memory Read

80C51SL-BG ERRATA

The hardware speedup option on Pin 57 (GATEA20) and Pin 64 (RCL) causes spurious false interrupts on the PCIBF interrupt. Before processing a PCIBF the software should first check the status of the PCIBF register (Address 7FF2H, Bit 1). If this register is consecutively read active twice, continue to service the subroutine. Otherwise, do not service the subroutine.

REVISION HISTORY

The following differences exist between this data sheet and the previous version (270980-001).

1. Port 2 pin description was clarified by saying "with internal pull-ups on P20-6/A8-14".
2. The Exiting Power-Down Mode section was changed to eliminate P30, P33, and P37 as sources to exit power-down mode. Note 4 "All inputs without internal pullups and floating I/Os must be driven to a known state" was added.
3. Table 9 Interrupt sources group 0 was clarified by adding standard C51 interrupt names in parenthesis. In addition, the level/edge active states for several of the group 0 interrupts was clarified.
4. Figures 6–10 and 13 the description of the x entry in the register diagram was changed and a note added.
5. Figure 11 the 32K EPROM was changed to read 32K EPROM, SRAM, and FLASH.
6. In the Application Example the note indicating throughput times for ROM devices has been removed.
7. V_{IL} and V_{IH} specs KSI0-7 have been changed. I_{OL} and I_{OH} test conditions for V_{OL} and V_{OH} have been changed for PCDB0–7 and ADB0–7.
8. DC Characteristics notes have been renumbered.
9. Idle and Power-Down Mode test conditions have been changed.
10. Errata has been added.