80960KB
EMBEDDED 32-BIT MICROPROCESSOR WITH INTEGRATED FLOATING-POINT UNIT

- **High-Performance Embedded Architecture**
  - **— 25 MIPS Burst Execution at 25 MHz**
  - **— 9.4 MIPS* Sustained Execution at 25 MHz**
- **512-Byte On-Chip Instruction Cache**
  - **— Direct Mapped**
  - **— Parallel Load/Decode for Uncached Instructions**
- **Multiple Register Sets**
  - **— Sixteen Global 32-Bit Registers**
  - **— Sixteen Local 32-Bit Registers**
  - **— Four Local Register Sets Stored On-Chip**
  - **— Register Scoreboarding**
- **4 Gigabyte, Linear Address Space**
- **Pin Compatible with 80960KA**
- **Built-in Interrupt Controller**
  - **— 31 Priority Levels, 256 Vectors**
  - **— 3.4 µs Latency @ 25 MHz**
- **Easy to Use, High Bandwidth 32-Bit Bus**
  - **— 66.7 Mbytes/s Burst**
  - **— Up to 16 Bytes Transferred per Burst**
- **132-Lead Packages:**
  - **— Pin Grid Array (PGA)**
  - **— Plastic Quad Flat-Pack (PQFP)**
- **On-Chip Floating Point Unit**
  - **— Supports IEEE 754 Floating Point Standard**
  - **— Four 80-Bit Registers**
  - **— 13.6 Million Whetstones/s (Single Precision) at 25 MHz**

The 80960KB is a member of Intel's i960® 32-bit processor family, which is designed especially for embedded applications. It includes a 512-byte instruction cache, an integrated floating-point unit and a built-in interrupt controller. The 80960KB has a large register set, multiple parallel execution units and a high-bandwidth burst bus. Using advanced RISC technology, this high performance processor is capable of execution rates in excess of 9.4 million instructions per second*. The 80960KB is well-suited for a wide range of applications including non-impact printers, I/O control and specialty instrumentation.

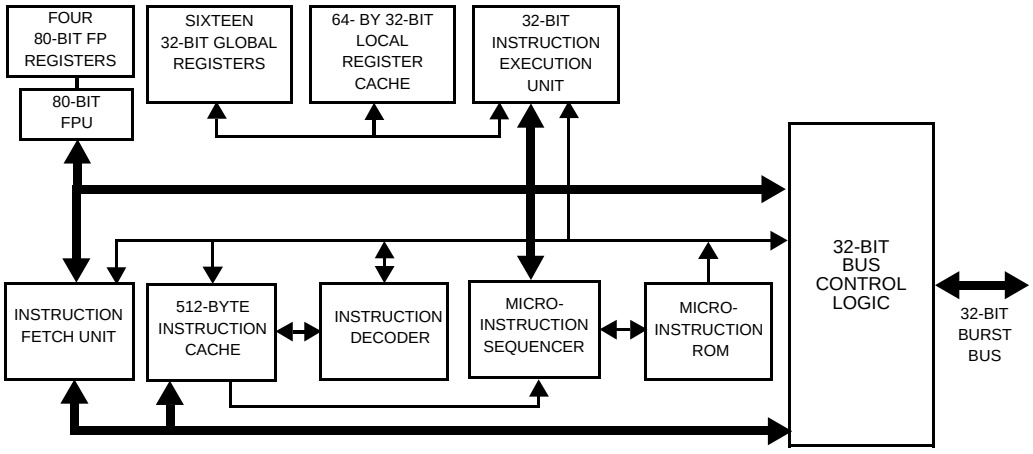


Figure 1. The 80960KB Processor's Highly Parallel Architecture

* Relative to Digital Equipment Corporation's VAX-11/780 at 1 MIPS (VAX-11™ is a trademark of Digital Equipment Corporation)

May 1993

Order Number: 270565-006

1.0 THE i960® PROCESSOR

The 80960KB is a member of the 32-bit architecture from Intel known as the i960 processor family. These were especially designed to serve the needs of embedded applications. The embedded market includes applications as diverse as industrial automation, avionics, image processing, graphics and networking. These types of applications require high integration, low power consumption, quick interrupt response times and high performance. Since time to market is critical, embedded microprocessors need to be easy to use in both hardware and software designs.

All members of the i960 processor family share a common core architecture which utilizes RISC technology so that, except for special functions, the family members are object-code compatible. Each new processor in the family adds its own special set of functions to the core to satisfy the needs of a specific application or range of applications in the embedded market.

Software written for the 80960KB will run without modification on any other member of the 80960 Family. It is also pin-compatible with the 80960KA and the 80960MC which is a military-grade version that supports multitasking, memory management, multi-processing and fault tolerance.

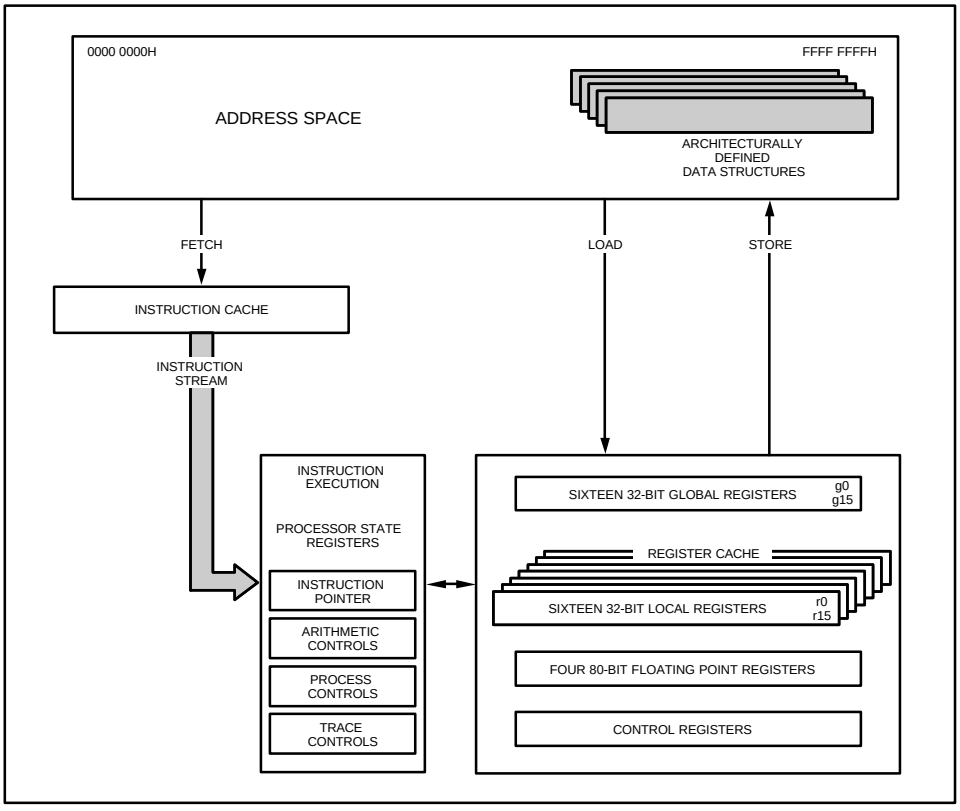


Figure 2. 80960KB Programming Environment

1.1. Key Performance Features

The 80960 architecture is based on the most recent advances in microprocessor technology and is grounded in Intel's long experience in the design and manufacture of embedded microprocessors. Many features contribute to the 80960KB's exceptional performance:

1. Large Register Set. Having a large number of registers reduces the number of times that a processor needs to access memory. Modern compilers can take advantage of this feature to optimize execution speed. For maximum flexibility, the 80960KB provides thirty-two 32-bit registers and four 80-bit floating point registers. (See Figure 2.)

2. Fast Instruction Execution. Simple functions make up the bulk of instructions in most programs so that execution speed can be improved by ensuring that these core instructions are executed as quickly as possible. The most frequently executed instructions such as register-register moves, add/subtract, logical operations and shifts execute in one to two cycles. (Table 1 contains a list of instructions.)

3. Load/Store Architecture. One way to improve execution speed is to reduce the number of times that the processor must access memory to perform an operation. As with other processors based on RISC technology, the 80960KB has a Load/Store architecture. As such, only the LOAD and STORE instructions reference memory; all other instructions operate on registers. This type of architecture simplifies instruction decoding and is used in combination with other techniques to increase parallelism.

4. Simple Instruction Formats. All instructions in the 80960KB are 32 bits long and must be aligned on word boundaries. This alignment makes it possible to eliminate the instruction alignment stage in the pipeline. To simplify the instruction decoder, there are only five instruction formats; each instruction uses only one format. (See Figure 3.)

5. Overlapped Instruction Execution. Load operations allow execution of subsequent instructions to continue before the data has been returned from memory, so that these instructions can overlap the load. The 80960KB manages this process transparently to software through the use of a register scoreboard. Conditional instructions also make use of a scoreboard so that subsequent unrelated instructions may be executed while the conditional instruction is pending.

6. Integer Execution Optimization. When the result of an arithmetic execution is used as an operand in a subsequent calculation, the value is sent immediately to its destination register. Yet at the same time, the value is put on a bypass path to the ALU, thereby saving the time that otherwise would be required to retrieve the value for the next operation.

7. Bandwidth Optimizations. The 80960KB gets optimal use of its memory bus bandwidth because the bus is tuned for use with the on-chip instruction cache: instruction cache line size matches the maximum burst size for instruction fetches. The 80960KB automatically fetches four words in a burst and stores them directly in the cache. Due to the size of the cache and the fact that it is continually filled in anticipation of needed instructions in the program flow, the 80960KB is relatively insensitive to memory wait states. The benefit is that the 80960KB delivers outstanding performance even with a low cost memory system.

8. Cache Bypass. If a cache miss occurs, the processor fetches the needed instruction then sends it on to the instruction decoder at the same time it updates the cache. Thus, no extra time is spent to load and read the cache.

Table 1. 80960KB Instruction Set

Data Movement	Arithmetic	Logical	Bit and Bit Field
Load Store Move Load Address	Add Subtract Multiply Divide Remainder Modulo Shift	And Not And And Not Or Exclusive Or Not Or Or Not Exclusive Nor Not Nand Rotate	Set Bit Clear Bit Not Bit Check Bit Alter Bit Scan For Bit Scan Over Bit Extract Modify
Comparison	**Branch**	**Call/Return**	**Fault**
Compare Conditional Compare Compare and Increment Compare and Decrement	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	**Miscellaneous**	**Decimal**	**Floating Point**
Modify Trace Controls Mark Force Mark	Atomic Add Atomic Modify Flush Local Registers Modify Arithmetic Controls Scan Byte for Equal Test Condition Code Modify Process Controls	Decimal Move Decimal Add with Carry Decimal Subtract with Carry	Move Real Add Subtract Multiply Divide Remainder Scale Round Square Root Sine Cosine Tangent Arctangent Log Log Binary Log Natural Exponent Classify Copy Real Extended Compare
		Synchronous	**Conversion**
		Synchronous Load Synchronous Move	Convert Real to Integer Convert Integer to Real

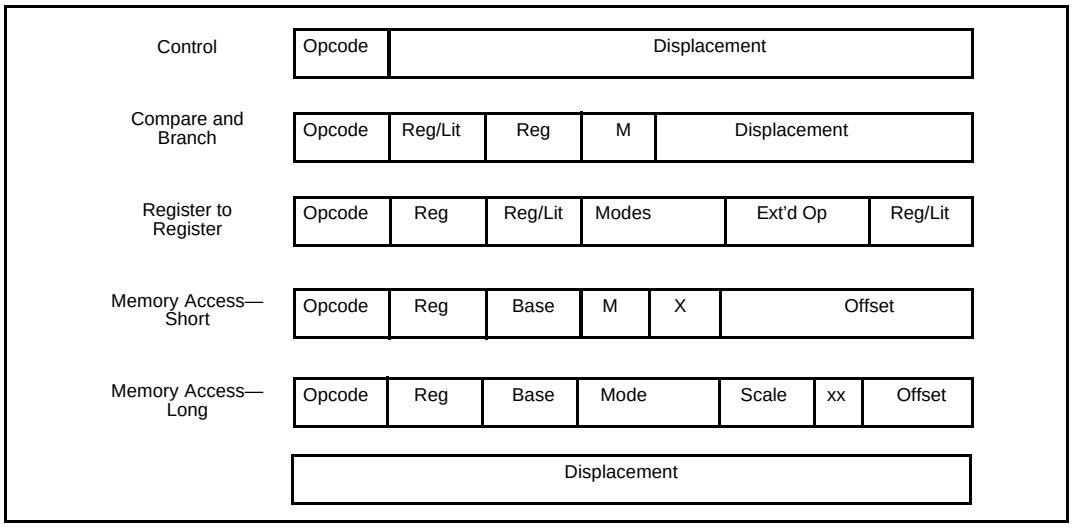


Figure 3. Instruction Formats

1.1.1. Memory Space And Addressing Modes

The 80960KB offers a linear programming environment so that all programs running on the processor are contained in a single address space. Maximum address space size is 4 Gigabytes (2^{32} bytes).

For ease of use the 80960KB has a small number of addressing modes, but includes all those necessary to ensure efficient execution of high-level languages such as C. Table 2 lists the modes.

Table 2. Memory Addressing Modes

- 12-Bit Offset
- 32-Bit Offset
- Register-Indirect
- Register + 12-Bit Offset
- Register + 32-Bit Offset
- Register + (Index-Register x Scale-Factor)
- Register x Scale Factor + 32-Bit Displacement
- Register + (Index-Register x Scale-Factor) + 32-Bit Displacement
- Scale-Factor is 1, 2, 4, 8 or 16

1.1.2. Data Types

The 80960KB recognizes the following data types:

Numeric:
- 8-, 16-, 32- and 64-bit ordinals
- 8-, 16-, 32- and 64-bit integers
- 32-, 64- and 80-bit real numbers

Non-Numeric:
- Bit
- Bit Field
- Triple Word (96 bits)
- Quad-Word (128 bits)

1.1.3. Large Register Set

The 80960KB programming environment includes a large number of registers. In fact, 32 registers are available at any time. The availability of this many registers greatly reduces the number of memory accesses required to perform algorithms, which leads to greater instruction processing speed.

There are two types of general-purpose registers: local and global. The 20 global registers consist of sixteen 32-bit registers (G0 though G15) and four

80-bit registers (FP0 through FP3). These registers perform the same function as the general-purpose registers provided in other popular microprocessors. The term global refers to the fact that these registers retain their contents across procedure calls.

The local registers, on the other hand, are procedure specific. For each procedure call, the 80960KB allocates 16 local registers (R0 through R15). Each local register is 32 bits wide. Any register can also be used for single or double-precision floating-point operations; the 80-bit floating-point registers are provided for extended precision.

1.1.4. Multiple Register Sets

To further increase the efficiency of the register set, multiple sets of local registers are stored on-chip (See Figure 4). This cache holds up to four local register frames, which means that up to three procedure calls can be made without having to access the procedure stack resident in memory.

Although programs may have procedure calls nested many calls deep, a program typically oscillates back and forth between only two to three levels. As a result, with four stack frames in the cache, the probability of having a free frame available on the cache when a call is made is very high. In fact, runs of representative C-language programs show that 80% of the calls are handled without needing to access memory.

If four or more procedures are active and a new procedure is called, the 80960KB moves the oldest local register set in the stack-frame cache to a procedure stack in memory to make room for a new set of registers. Global register G15 is the frame pointer (FP) to the procedure stack.

Global and floating point registers are not exchanged on a procedure call, but retain their contents, making them available to all procedures for fast parameter passing.

1.1.5. Instruction Cache

To further reduce memory accesses, the 80960KB includes a 512-byte on-chip instruction cache. The instruction cache is based on the concept of locality of reference; most programs are not usually executed in a steady stream but consist of many branches, loops and procedure calls that lead to jumping back and forth in the same small section of code. Thus, by maintaining a block of instructions in cache, the number of memory references required to read instructions into the processor is greatly reduced.

To load the instruction cache, instructions are fetched in 16-byte blocks; up to four instructions can be fetched at one time. An efficient prefetch algorithm increases the probability that an instruction will already be in the cache when it is needed.

Code for small loops often fits entirely within the cache, leading to a great increase in processing speed since further memory references might not be necessary until the program exits the loop. Similarly, when calling short procedures, the code for the calling procedure is likely to remain in the cache so it will be there on the procedure's return.

1.1.6. Register Scoreboarding

The instruction decoder is optimized in several ways. One optimization method is the ability to overlap instructions by using register scoreboarding.

Register scoreboarding occurs when a LOAD moves a variable from memory into a register. When the instruction initiates, a scoreboard bit on the target register is set. Once the register is loaded, the bit is reset. In between, any reference to the register contents is accompanied by a test of the scoreboard bit to ensure that the load has completed before processing continues. Since the processor does not need to wait for the LOAD to complete, it can execute additional instructions placed between the LOAD and the instruction that uses the register contents, as shown in the following example:

```
ld data_2, r4
ld data_2, r5
Unrelated instruction
Unrelated instruction
add R4, R5, R6
```

In essence, the two unrelated instructions between LOAD and ADD are executed "for free" (i.e., take no apparent time to execute) because they are executed while the register is being loaded. Up to three load instructions can be pending at one time with three corresponding scoreboard bits set. By exploiting this feature, system programmers and compiler writers have a useful tool for optimizing execution speed.

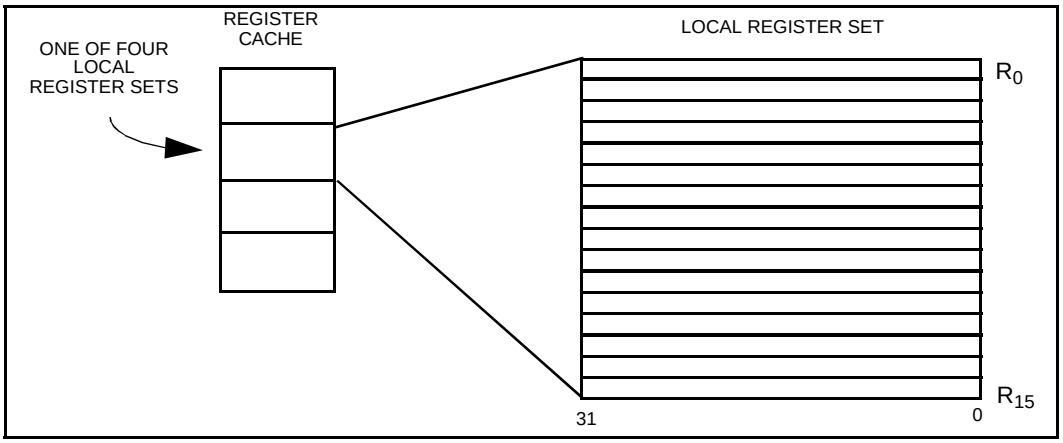


Figure 4. Multiple Register Sets Are Stored On-Chip

1.1.7. Floating-Point Arithmetic

In the 80960KB, floating-point arithmetic has been made an integral part of the architecture. Having the floating-point unit integrated on-chip provides two advantages. First, it improves the performance of the chip for floating-point applications, since no additional bus overhead is associated with floating-point calculations, thereby leaving more time for other bus operations such as I/O. Second, the cost of using floating-point operations is reduced because a separate coprocessor chip is not required.

The 80960KB floating-point (real-number) data types include single-precision (32-bit), double-precision (64-bit) and extended precision (80-bit) floating-point numbers. Any registers may be used to execute floating-point operations.

The processor provides hardware support for both mandatory and recommended portions of IEEE Standard 754 for floating-point arithmetic, including all arithmetic, exponential, logarithmic and other transcendental functions. Table 3 shows execution times for some representative instructions.

Table 3. Sample Floating-Point Execution Times (µs) at 25 MHz

Function	32-Bit	64-Bit
Add	0.4	0.5
Subtract	0.4	0.5
Multiply	0.7	1.3
Divide	1.3	2.9
Square Root	3.7	3.9
Arctangent	10.1	13.1
Exponent	11.3	12.5
Sine	15.2	16.6
Cosine	15.2	16.6

1.1.8. High Bandwidth Local Bus

The 80960KB CPU resides on a high-bandwidth address/data bus known as the local bus (L-Bus). The L-Bus provides a direct communication path between the processor and the memory and I/O subsystem interfaces. The processor uses the L-Bus to fetch instructions, manipulate memory and respond to interrupts. L-Bus features include:

- 32-bit multiplexed address/data path
- Four-word burst capability which allows transfers from 1 to 16 bytes at a time
- High bandwidth reads and writes with 66.7 MBytes/s burst (at 25 MHz)

Table 4 defines L-bus signal names and functions; Table 5 defines other component-support signals such as interrupt lines.

1.1.9. Interrupt Handling

The 80960KB can be interrupted in two ways: by the activation of one of four interrupt pins or by sending a message on the processor's data bus.

The 80960KB is unusual in that it automatically handles interrupts on a priority basis and can keep track of pending interrupts through its on-chip interrupt controller. Two of the interrupt pins can be configured to provide 8259A-style handshaking for expansion beyond four interrupt lines.

1.1.10. Debug Features

The 80960KB has built-in debug capabilities. There are two types of breakpoints and six trace modes. Debug features are controlled by two internal 32-bit registers: the Process-Controls Word and the Trace-Controls Word. By setting bits in these control words, a software debug monitor can closely control how the processor responds during program execution.

The 80960KB provides two hardware breakpoint registers on-chip which, by using a special command, can be set to any value. When the instruction pointer matches either breakpoint register value, the breakpoint handling routine is automatically called.

The 80960KB also provides software breakpoints through the use of two instructions: MARK and FMARK. These can be placed at any point in a program and cause the processor to halt execution at that point and call the breakpoint handling routine. The breakpoint mechanism is easy to use and provides a powerful debugging tool.

Tracing is available for instructions (single step execution), calls and returns and branching. Each trace type may be enabled separately by a special debug instruction. In each case, the 80960KB executes the instruction first and then calls a trace handling routine (usually part of a software debug monitor). Further program execution is halted until the routine completes, at which time execution resumes at the next instruction. The 80960KB's tracing mechanisms, implemented completely in hardware, greatly simplify the task of software test and debug.

1.1.11. Fault Detection

The 80960KB has an automatic mechanism to handle faults. Fault types include floating point, trace and arithmetic faults. When the processor detects a fault, it automatically calls the appropriate fault handling routine and saves the current instruction pointer and necessary state information to make efficient recovery possible. Like interrupt handling routines, fault handling routines are usually written to meet the needs of specific applications and are often included as part of the operating system or kernel.

For each of the fault types, there are numerous subtypes that provide specific information about a fault. For example, a floating point fault may have the subtype set to an Overflow or Zero-Divide fault. The fault handler can use this specific information to respond correctly to the fault.

1.1.12. Built-in Testability

Upon reset, the 80960KB automatically conducts an exhaustive internal test of its major blocks of logic. Then, before executing its first instruction, it does a zero check sum on the first eight words in memory to ensure that the memory image was programmed correctly. If a problem is discovered at any point during the self-test, the 80960KB asserts its $\overline{\text{FAILURE}}$ pin and will not begin program execution. Self test takes approximately 47,000 cycles to complete.

System manufacturers can use the 80960KB's self-test feature during incoming parts inspection. No special diagnostic programs need to be written. The test is both thorough and fast. The self-test capability helps ensure that defective parts are discovered before systems are shipped and, once in the field, the self-test makes it easier to distinguish between problems caused by processor failure and problems resulting from other causes.

1.1.13. CHMOS

The 80960KB is fabricated using Intel's CHMOS IV (Complementary High Speed Metal Oxide Semiconductor) process. The 80960KB is currently available in 16, 20 and 25 MHz versions.

Table 4. 80960KB Pin Description: L-Bus Signals (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CLK2	I	**SYSTEM CLOCK** provides the fundamental timing for 80960KB systems. It is divided by two inside the 80960KB and four 80-bit registers (FP0 through FP3) to generate the internal processor clock.
LAD31:0	I/O T.S.	**LOCAL ADDRESS / DATA BUS** carries 32-bit physical addresses and data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, bits 0-31 contain read or write data. These pins float to a high impedance state when not active. Bits 0-1 comprise SIZE during a T_a cycle. SIZE specifies burst transfer size in words. **LAD1 LAD0** 0 0 1 Word 0 1 2 Words 1 0 3 Words 1 1 4 Words
$\overline{ALE}$	O T.S.	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. $\overline{ALE}$ is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active LOW and floats to a high impedance state during a hold cycle (T_h).
$\overline{ADS}$	O O.D.	**ADDRESS/DATA STATUS** indicates an address state. $\overline{ADS}$ is asserted every T_a state and deasserted during the following T_d state. For a burst transaction, $\overline{ADS}$ is asserted again every T_d state where $\overline{READY}$ was asserted in the previous cycle.
W/$\overline{R}$	O O.D.	**WRITE/READ** specifies, during a T_a cycle, whether the operation is a write or read. It is latched on-chip and remains valid during T_d cycles.
DT/$\overline{R}$	O O.D.	**DATA TRANSMIT / RECEIVE** indicates the direction of data transfer to and from the L-Bus. It is low during T_a and T_d cycles for a read or interrupt acknowledgment; it is high during T_a and T_d cycles for a write. DT/$\overline{R}$ never changes state when $\overline{DEN}$ is asserted.
$\overline{READY}$	I	**READY** indicates that data on LAD lines can be sampled or removed. If $\overline{READY}$ is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting a wait state (T_w) and $\overline{ADS}$ is not asserted in the next cycle.
$\overline{LOCK}$	I/O O.D.	**BUS LOCK** prevents bus masters from gaining control of the L-Bus during Read/Modify/Write (RMW) cycles. The processor or any bus agent may assert $\overline{LOCK}$. At the start of a RMW operation, the processor examines the $\overline{LOCK}$ pin. If the pin is already asserted, the processor waits until it is not asserted. If the pin is not asserted, the processor asserts $\overline{LOCK}$ during the T_a cycle of the read transaction. The processor deasserts $\overline{LOCK}$ in the T_a cycle of the write transaction. During the time $\overline{LOCK}$ is asserted, a bus agent can perform a normal read or write but not a RMW operation. The processor also asserts $\overline{LOCK}$ during interrupt-acknowledge transactions. Do not leave $\overline{LOCK}$ unconnected. It must be pulled high for the processor to function properly.

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

Table 4. 80960KB Pin Description: L-Bus Signals (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
$\overline{BE3:0}$	O O.D.	**BYTE ENABLE LINES** specify the data bytes (up to four) on the bus which are used in the current bus cycle. $\overline{BE3}$ corresponds to LAD31:24; $\overline{BE0}$ corresponds to LAD7:0. The byte enables are provided in advance of data: • Byte enables asserted during T_a specify the bytes of the first data word. • Byte enables asserted during T_d specify the bytes of the next data word, if any (the word to be transmitted following the next assertion of $\overline{READY}$). Byte enables that occur during T_d cycles that precede the last assertion of $\overline{READY}$ are undefined. Byte enables are latched on-chip and remain constant from one T_d cycle to the next when $\overline{READY}$ is not asserted. For reads, byte enables specify the byte(s) that the processor will actually use. L-Bus agents are required to assert only adjacent byte enables (e.g., asserting just $\overline{BE0}$ and $\overline{BE2}$ is not permitted) and are required to assert at least one byte enable. Address bits A_0 and A_1 can be decoded externally from the byte enables.
HOLD	I	**HOLD**: A request from an external bus master to acquire the bus. When the processor receives HOLD and grants bus control to another master, it floats its three-state bus lines and open-drain control lines, asserts HLDA and enters the T_h state. When HOLD deasserts, the processor deasserts HLDA and enters the T_i or T_a state.
HLDA	O T.S.	**HOLD ACKNOWLEDGE**: Notifies an external bus master that the processor has relinquished control of the bus.
CACHE	O T.S.	**CACHE** indicates when an access is cacheable during a T_a cycle. It is not asserted during any synchronous access, such as a synchronous load or move instruction used for sending an IAC message. The CACHE signal floats to a high impedance state when the processor is idle.

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

Table 5. 80960KB Pin Description: Support Signals (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
$\overline{BADAC}$	I	**BAD ACCESS**, if asserted in the cycle following the one in which the last $\overline{READY}$ of a transaction is asserted, indicates that an unrecoverable error has occurred on the current bus transaction or that a synchronous load/store instruction has not been acknowledged. During system reset the $\overline{BADAC}$ signal is interpreted differently. If the signal is high, it indicates that this processor will perform system initialization. If it is low, another processor in the system will perform system initialization instead.
RESET	I	**RESET** clears the processor's internal logic and causes it to reinitialize. During RESET assertion, the input pins are ignored (except for $\overline{BADAC}$ and $\overline{IAC}/\overline{INT_0}$), the three-state output pins are placed in a high impedance state and other output pins are placed in their non-asserted states. RESET must be asserted for at least 41 CLK2 cycles for a predictable RESET. The HIGH to LOW transition of RESET should occur after the rising edge of both CLK2 and the external bus clock and before the next rising edge of CLK2.

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

Table 5. 80960KB Pin Description: Support Signals (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
$\overline{\text{FAILURE}}$	O O.D.	**INITIALIZATION FAILURE** indicates that the processor did not initialize correctly. After RESET deasserts and before the first bus transaction begins, $\overline{\text{FAILURE}}$ asserts while the processor performs a self-test. If the self-test completes successfully, then $\overline{\text{FAILURE}}$ deasserts. The processor then performs a zero checksum on the first eight words of memory. If it fails, $\overline{\text{FAILURE}}$ asserts for a second time and remains asserted. If it passes, system initialization continues and $\overline{\text{FAILURE}}$ remains deasserted.
$\overline{\text{IAC}}/\overline{\text{INT}}_0$	I	**INTERAGENT COMMUNICATION REQUEST/INTERRUPT 0** indicates an IAC message or an interrupt is pending. The bus interrupt control register determines how the signal is interpreted. To signal an interrupt or IAC request in a synchronous system, this pin — as well as the other interrupt pins — must be enabled by being deasserted for at least one bus cycle and then asserted for at least one additional bus cycle. In an asynchronous system the pin must remain deasserted for at least two bus cycles and then asserted for at least two more bus cycles. During system reset, this signal must be in the logic high condition to enable normal processor operation. The logic low condition is reserved.
INT_1	I	**INTERRUPT 1**, like $\overline{\text{INT}}_0$, provides direct interrupt signaling.
INT_2/INTR	I	**INTERRUPT2/INTERRUPT REQUEST**: The interrupt control register determines how this pin is interpreted. If INT_2, it has the same interpretation as the $\overline{\text{INT}}_0$ and INT_1 pins. If INTR, it is used to receive an interrupt request from an external interrupt controller.
$\overline{\text{INT}}_3/\overline{\text{INTA}}$	I/O O.D.	**INTERRUPT3/INTERRUPT ACKNOWLEDGE**: The bus interrupt control register determines how this pin is interpreted. If $\overline{\text{INT}}_3$, it has the same interpretation as the $\overline{\text{INT}}_0$, INT1 and INT2 pins. If $\overline{\text{INTA}}$, it is used as an output to control interrupt-acknowledge transactions. The $\overline{\text{INTA}}$ output is latched on-chip and remains valid during T_d cycles; as an output, it is open-drain.
N.C.	N/A	**NOT CONNECTED** indicates pins should not be connected. Never connect any pin marked N.C. as these pins may be reserved for factory use.

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

2.0 ELECTRICAL SPECIFICATIONS

2.1. Power and Grounding

The 80960KB is implemented in CHMOS IV technology and therefore has modest power requirements. Its high clock frequency and numerous output buffers (address/data, control, error and arbitration signals) can cause power surges as multiple output buffers simultaneously drive new signal levels. For clean on-chip power distribution, V_{CC} and V_{SS} pins separately feed the device's functional units. Power and ground connections must be made to all 80960KB power and ground pins. On the circuit board, all V_{cc} pins must be strapped closely together, preferably on a power plane; all V_{ss} pins should be strapped together, preferably on a ground plane.

2.2. Decoupling Recommendations

Place a liberal amount of decoupling capacitance near the 80960KB. When driving the L-bus the processor can cause transient power surges, particularly when connected to a large capacitive load.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance is reduced by shortening board traces between the processor and decoupling capacitors as much as possible.

2.3. Connection Recommendations

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, if one or more interrupt lines are not used, they should be pulled up. No inputs should ever be left floating.

All open-drain outputs require a pullup device. While in most cases a simple pullup resistor is adequate, a network of pullup and pulldown resistors biased to a valid V_{IH} (>3.0 V) and terminated in the characteristic impedance of the circuit board is recommended to limit noise and AC power consumption. Figure 5 and Figure 6 show recommended values for the resistor network for low and high current drive, assuming a characteristic impedance of 100 Ω. Terminating output signals in this fashion limits signal swing and reduces AC power consumption.

NOTE:
Do not connect external logic to pins marked N.C.

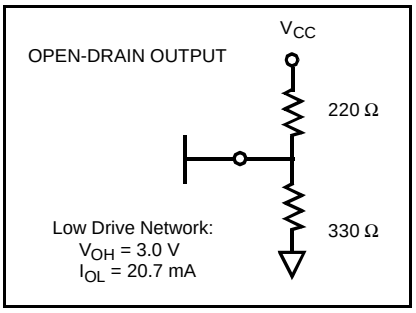


Figure 5. Connection Recommendations for Low Current Drive Network

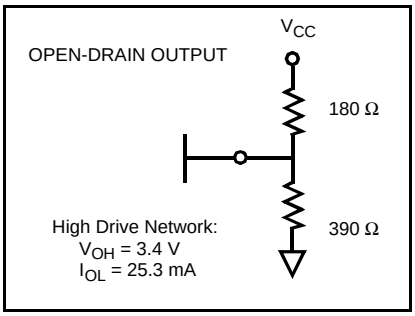


Figure 6. Connection Recommendations for High Current Drive Network

2.4. Characteristic Curves

Figure 7 shows typical supply current requirements over the operating temperature range of the processor at supply voltage (V_{CC}) of 5 V. Figure 8 and Figure 9 show the typical power supply current (I_{CC}) that the 80960KB requires at various operating frequencies when measured at three input voltage (V_{CC}) levels and two temperatures.

For a given output current (I_{OL}) the curve in Figure 10 shows the worst case output low voltage (V_{OL}). Figure 11 shows the typical capacitive derating curve for the 80960KB measured from 1.5V on the system clock (CLK) to 1.5V on the falling edge and 1.5V on the rising edge of the L-Bus address/data (LAD) signals.

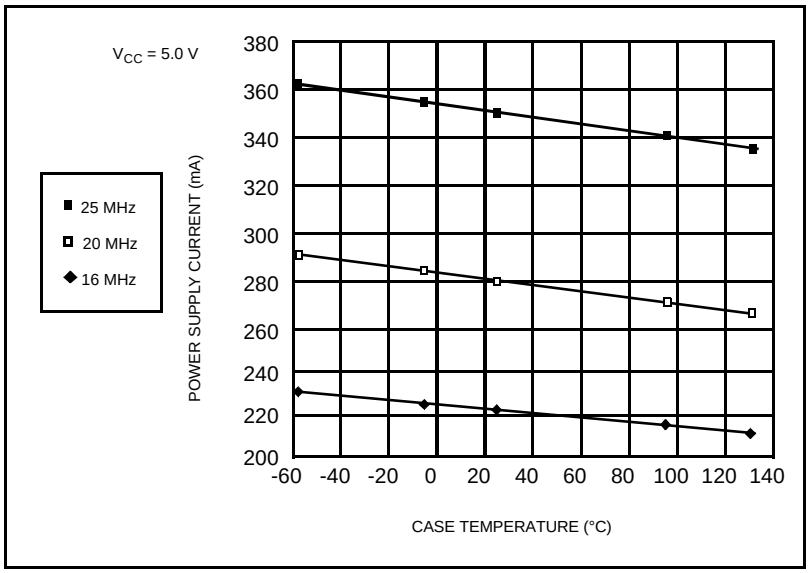


Figure 7. Typical Supply Current vs. Case Temperature

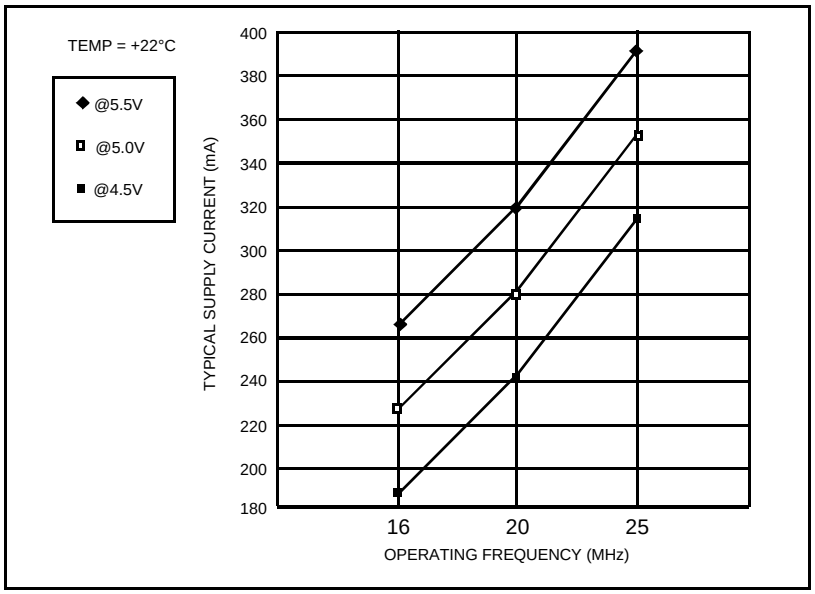


Figure 8. Typical Current vs. Frequency (Room Temp)

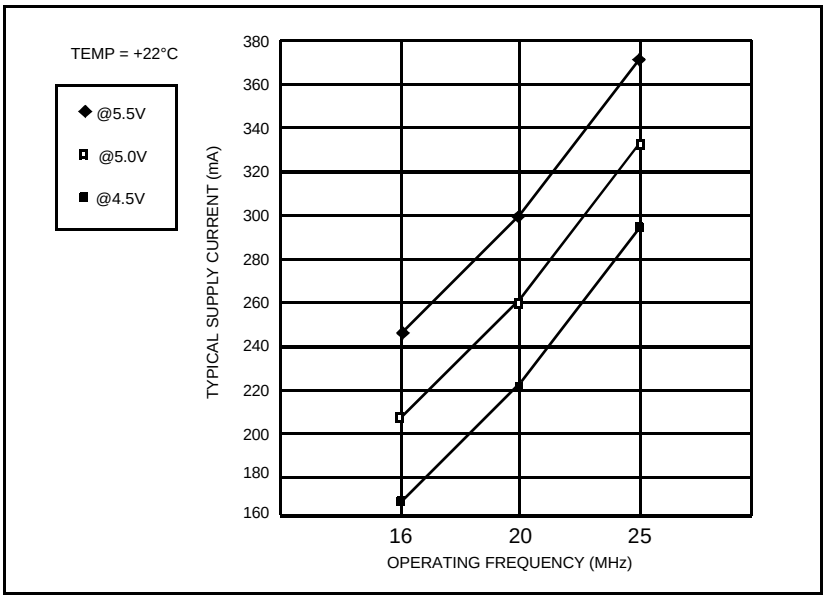


Figure 9. Typical Current vs. Frequency (Hot Temp)

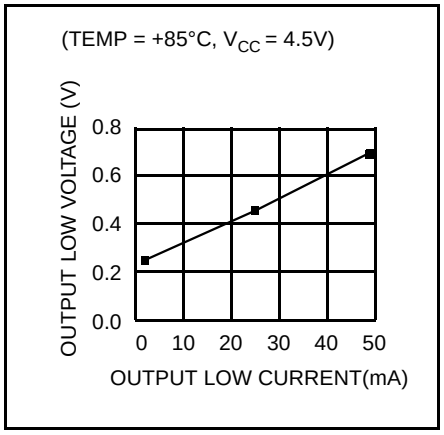


Figure 10. Worst-Case Voltage vs. Output Current on Open-Drain Pins

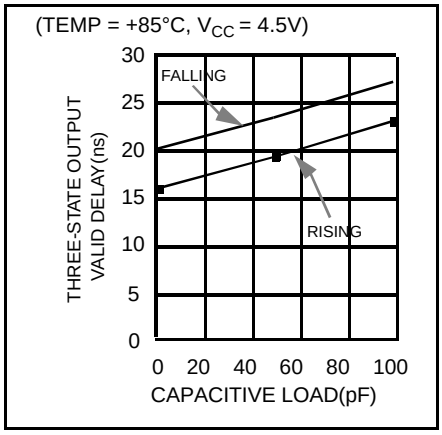


Figure 11. Capacitive Derating Curve

2.5. Test Load Circuit

Figure 12 illustrates the load circuit used to test the 80960KB's three-state pins; Figure 13 shows the load circuit used to test the open drain outputs. The open drain test uses an active load circuit in the form of a matched diode bridge. Since the open-drain outputs sink current, only the I_{OL} legs of the bridge are necessary and the I_{OH} legs are not used. When the 80960KB driver under test is turned off, the output pin is pulled up to V_{REF} (i.e., V_{OH}). Diode D_1 is turned off and the I_{OL} current source flows through diode D_2.

When the 80960KB open-drain driver under test is on, diode D_1 is also on and the voltage on the pin being tested drops to V_{OL}. Diode D_2 turns off and I_{OL} flows through diode D_1.

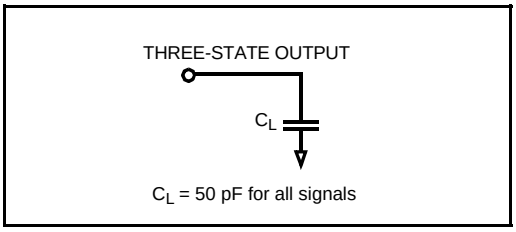


Figure 12. Test Load Circuit for Three-State Output Pins

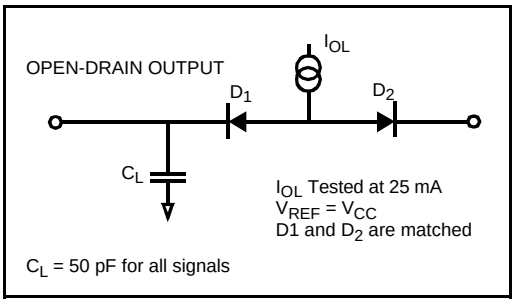


Figure 13. Test Load Circuit for Open-Drain Output Pins

2.6. Absolute Maximum Ratings

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

Operating Temperature (PGA)..... 0°C to +85°C Case
(PQFP) ..... 0°C to +100°C Case
Storage Temperature ..... –65°C to +150°C
Voltage on Any Pin..... –0.5V to V_{CC} +0.5V
Power Dissipation ..... 2.5W (25 MHz)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

2.7. DC Characteristics

PGA: 80960KB (16 MHz) T_{CASE} = 0°C to +85°C, V_{CC} = 5V ± 10%
80960KB (20 and 25 MHz) T_{CASE} = 0°C to +85°C, V_{CC} = 5V ± 5%
PQFP: 80960KB (16 MHz) T_{CASE} = 0°C to +100°C, V_{CC} = 5V ± 10%
80960KB (20 and 25 MHz) T_{CASE} = 0°C to +100°C, V_{CC} = 5V ± 5%

Table 6. DC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	–0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{CL}	CLK2 Input Low Voltage	–0.3	+0.8	V	
V_{CH}	CLK2 Input High Voltage	0.55 V_{CC}	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(1,2)
V_{OH}	Output High Voltage	2.4		V	(3,4)
I_{CC}	Power Supply Current: 16 MHz 20 MHz 25 MHz		 315 360 420	 mA mA mA	 (5) (5) (5)
I_{LI}	Input Leakage Current		±15	µA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±15	µA	$0.45 \le V_O \le V_{CC}$
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz (6)
C_O	Output Capacitance		12	pF	f_C = 1 MHz (6)
C_{CLK}	Clock Capacitance		10	pF	f_C = 1 MHz (6)

NOTES:
1. For three-state outputs, this parameter is measured at:
   Address/Data ..... 4.0 mA
   Controls ..... 5.0 mA
2. For open-drain outputs ..... 25 mA
3. This parameter is measured at:
   Address/Data ..... -1.0 mA
   Controls ..... -0.9 mA
   $\overline{ALE}$ ..... -5.0 mA
4. Not measured on open-drain outputs.
5. Measured at worst case frequency, V_{CC} and temperature, with device operating and outputs loaded to the test conditions in Figures 12 and 13. Figure 7, Figure 8 and Figure 9 indicate typical values.
6. Input, output and clock capacitance are not tested.

2.8. AC Specifications

This section describes the AC specifications for the 80960KB pins. All input and output timings are specified relative to the 1.5 V level of the rising edge of CLK2. For output timings the specifications refer to the time it takes the signal to reach 1.5 V.

For input timings the specifications refer to the time at which the signal reaches (for input setup) or leaves (for hold time) the TTL levels of LOW (0.8 V) or HIGH (2.0 V). All AC testing should be done with input voltages of 0.4 V and 2.4 V, except for the clock (CLK2), which should be tested with input voltages of 0.45 V and 0.55 V_{CC}.

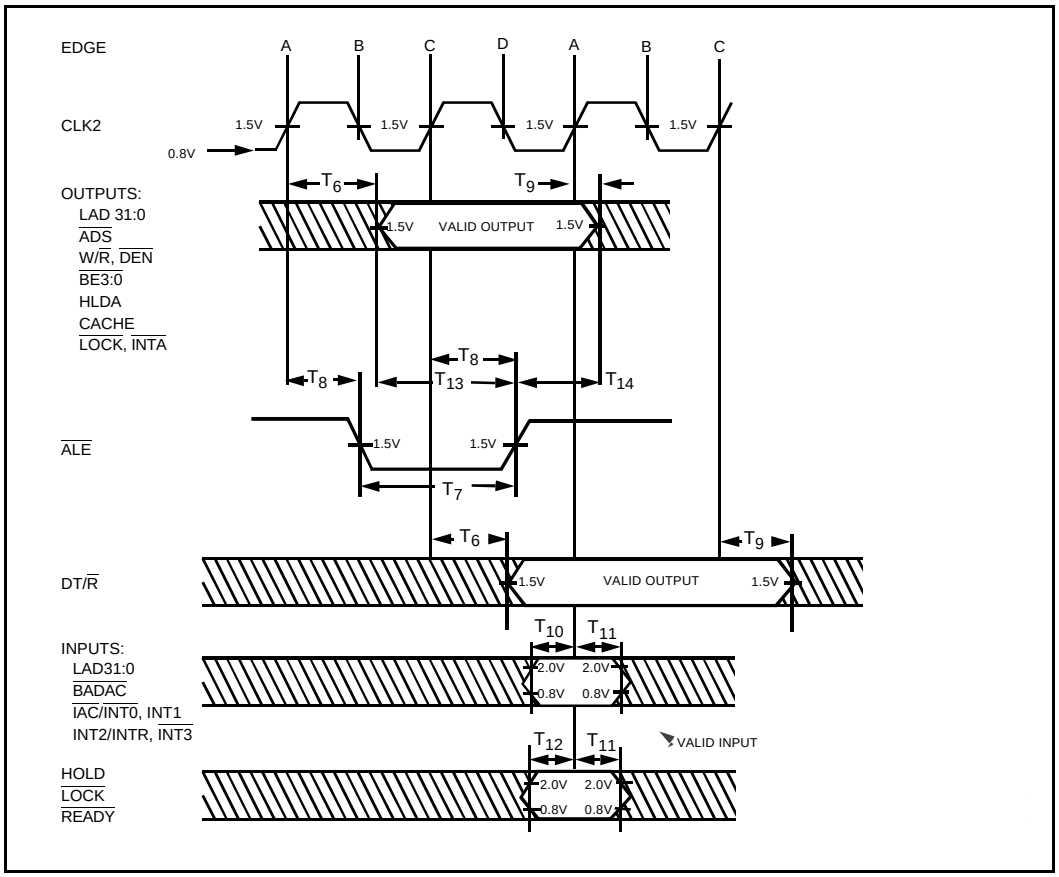


Figure 14. Drive Levels and Timing Relationships for 80960KB Signals

2.8.1. AC Specification Tables

Table 7. 80960KB AC Characteristics (16 MHz)

Symbol	Parameter	Min	Max	Units	Notes
Input Clock					
T_1	Processor Clock Period (CLK2)	31.25	125	ns	V_{IN} = 1.5V
T_2	Processor Clock Low Time (CLK2)	8		ns	V_{IL} = 10% Point = 1.2V
T_3	Processor Clock High Time (CLK2)	8		ns	V_{IH} = 90% Point = 0.1V + 0.5 V_{CC}
T_4	Processor Clock Fall Time (CLK2)		10	ns	V_{IN} = 90% Point to 10% Point (1)
T_5	Processor Clock Rise Time (CLK2)		10	ns	V_{IN} = 10% Point to 90% Point (1)
Synchronous Outputs					
T_6	Output Valid Delay	2	25	ns	
T_{6H}	HLDA Output Valid Delay	4	28	ns	
T_7	$\overline{ALE}$ Width	15		ns	
T_8	$\overline{ALE}$ Output Valid Delay	2	18	ns	
T_9	Output Float Delay	2	20	ns	(2)
T_{9H}	HLDA Output Float Delay	4	20	ns	(2)
Synchronous Inputs					
T_{10}	Input Setup 1	3		ns	(3)
T_{11}	Input Hold	5		ns	(3)
T_{11H}	HOLD Input Hold	4		ns	(3)
T_{12}	Input Setup 2	8		ns	(3)
T_{13}	Setup to $\overline{ALE}$ Inactive	10		ns	
T_{14}	Hold after $\overline{ALE}$ Inactive	8		ns	
T_{15}	Reset Hold	3		ns	(3)
T_{16}	Reset Setup	5		ns	(3)
T_{17}	Reset Width	1281		ns	41 CLK2 Periods Minimum

NOTES:

1. Clock rise and fall times are not tested.
2. A float condition occurs when the maximum output current becomes less than I_{LO}. Float delay is not tested; however, it should not be longer than the valid delay.
3. LAD31:0, $\overline{BADAC}$, HOLD, $\overline{LOCK}$ and $\overline{READY}$ are synchronous inputs. $\overline{IAC}/\overline{INT}_0$, INT_1, INT_2/INT_R and $\overline{INT}_3$ may be synchronous or asynchronous.

Table 8. 80960KB AC Characteristics (20 MHz)

Symbol	Parameter	Min	Max	Units	Notes
Input Clock					
T_1	Processor Clock Period (CLK2)	25	125	ns	V_{IN} = 1.5V
T_2	Processor Clock Low Time (CLK2)	6		ns	V_{IL} = 10% Point = 1.2V
T_3	Processor Clock High Time (CLK2)	6		ns	V_{IH} = 90% Point = 0.1V + 0.5 V_{CC}
T_4	Processor Clock Fall Time (CLK2)		10	ns	V_{IN} = 90% Point to 10% Point (1)
T_5	Processor Clock Rise Time (CLK2)		10	ns	V_{IN} = 10% Point to 90% Point (1)
Synchronous Outputs					
T_6	Output Valid Delay	2	20	ns	
T_{6H}	HLDA Output Valid Delay	4	23	ns	
T_7	$\overline{ALE}$ Width	12		ns	
T_8	$\overline{ALE}$ Output Valid Delay	2	18	ns	
T_9	Output Float Delay	2	20	ns	(2)
T_{9H}	HLDA Output Float Delay	4	20	ns	(2)
Synchronous Inputs					
T_{10}	Input Setup 1	3		ns	(3)
T_{11}	Input Hold	5		ns	(3)
T_{11H}	HOLD Input Hold	4		ns	(3)
T_{12}	Input Setup 2	7		ns	(3)
T_{13}	Setup to $\overline{ALE}$ Inactive	10		ns	
T_{14}	Hold after $\overline{ALE}$ Inactive	8		ns	
T_{15}	Reset Hold	3		ns	
T_{16}	Reset Setup	5		ns	
T_{17}	Reset Width	1025		ns	41 CLK2 Periods Minimum

NOTES:

1. Clock rise and fall times are not tested.
2. A float condition occurs when the maximum output current becomes less than I_{LO}. Float delay is not tested; however, it should not be longer than the valid delay.
3. LAD31:0, $\overline{BADAC}$, HOLD, $\overline{LOCK}$ and $\overline{READY}$ are synchronous inputs. $\overline{IAC}/\overline{INT}_0$, INT_1, INT_2/INT_R and $\overline{INT}_3$ may be synchronous or asynchronous.

Table 9. 80960KB AC Characteristics (25 MHz)

Symbol	Parameter	Min	Max	Units	Notes
Input Clock					
T_1	Processor Clock Period (CLK2)	20	125	ns	V_{IN} = 1.5V
T_2	Processor Clock Low Time (CLK2)	5		ns	V_{IL} = 10% Point = 1.2V
T_3	Processor Clock High Time (CLK2)	5		ns	V_{IH} = 90% Point = 0.1V + 0.5 V_{CC}
T_4	Processor Clock Fall Time (CLK2)		10	ns	V_{IN} = 90% Point to 10% Point (1)
T_5	Processor Clock Rise Time (CLK2)		10	ns	V_{IN} = 10% Point to 90% Point (1)
Synchronous Outputs					
T_6	Output Valid Delay	2	18	ns	
T_{6H}	HLDA Output Valid Delay	4	23	ns	
T_7	$\overline{ALE}$ Width	12		ns	
T_8	$\overline{ALE}$ Output Valid Delay	2	18	ns	
T_9	Output Float Delay	2	18	ns	(2)
T_{9H}	HLDA Output Float Delay	4	20	ns	(2)
Synchronous Inputs					
T_{10}	Input Setup 1	3		ns	(3)
T_{11}	Input Hold	5		ns	(3)
T_{11H}	HOLD Input Hold	4		ns	
T_{12}	Input Setup 2	7		ns	
T_{13}	Setup to $\overline{ALE}$ Inactive	8		ns	
T_{14}	Hold after $\overline{ALE}$ Inactive	8		ns	
T_{15}	Reset Hold	3		ns	
T_{16}	Reset Setup	5		ns	
T_{17}	Reset Width	820		ns	41 CLK2 Periods Minimum

NOTES:

1. Clock rise and fall times are not tested.
2. A float condition occurs when the maximum output current becomes less than I_{LO}. Float delay is not tested; however, it should not be longer than the valid delay.
3. LAD31:0, $\overline{BADAC}$, HOLD, $\overline{LOCK}$ and $\overline{READY}$ are synchronous inputs. $\overline{IAC}/\overline{INT}_0$, INT_1, INT_2/INT_R and $\overline{INT}_3$ may be synchronous or asynchronous.

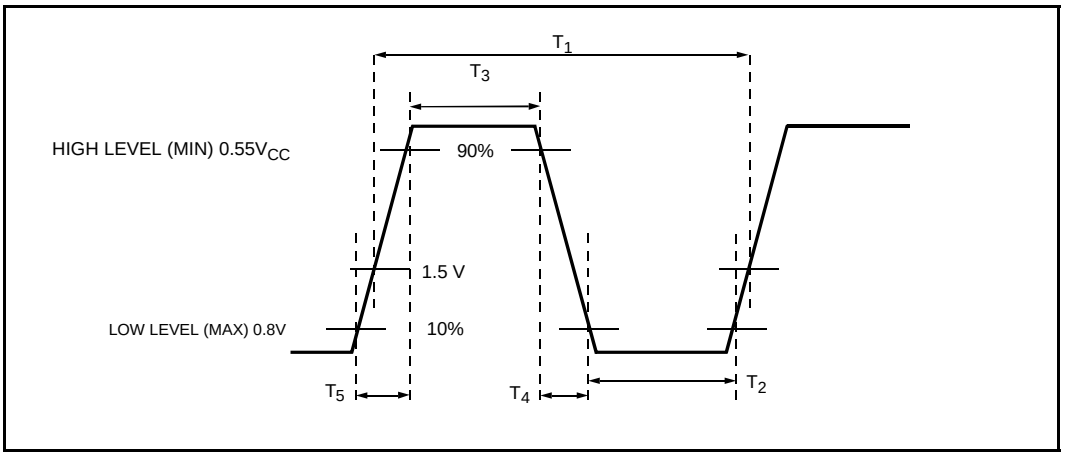


Figure 15. Processor Clock Pulse (CLK2)

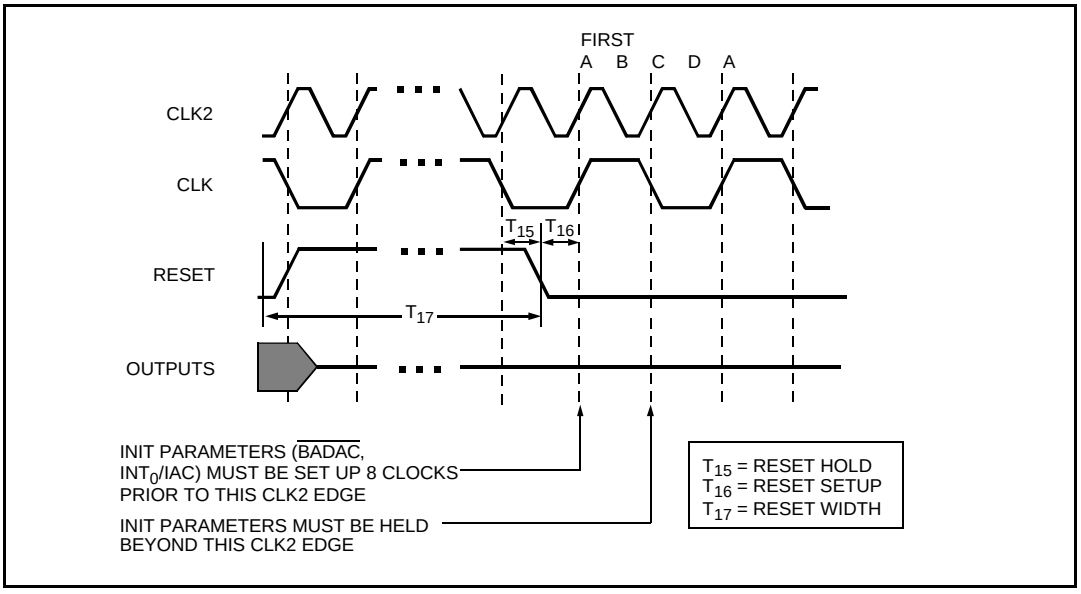


Figure 16. RESET Signal Timing

3.0 MECHANICAL DATA

3.1. Packaging

The 80960KB is available in two package types:

- 132-lead ceramic pin-grid array (PGA). Pins are arranged 0.100 inch (2.54 mm) center-to-center, in a 14 by 14 matrix, three rows around (see Figure 17).
- 132-lead plastic quad flat pack (PQFP). This package uses fine-pitch gull wing leads arranged in a single row along the package perimeter with 0.025 inch (0.64 mm) spacing (see Figure 20).

Dimensions for both package types are given in the Intel *Packaging* handbook (Order #240800).

3.1.1. Pin Assignment

The PGA and PQFP have different pin assignments. Figure 18 shows the view from the PGA bottom (pins facing up) and Figure 19 shows a view from the PGA top (pins facing down). Figure 20 shows the PQFP package; Figure 21 shows the PQFP pinout with signal names. Notice that the pins are numbered in order from 1 to 132 around the package perimeter. Table 10 and Table 11 list the function of each PGA pin; Table 12 and Table 13 list the function of each PQFP pin.

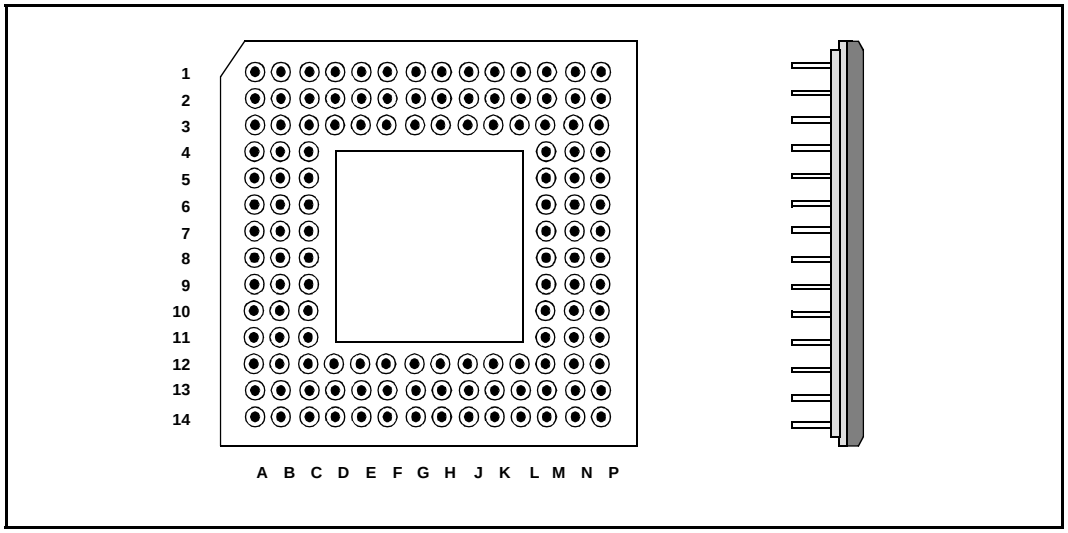


Figure 17. 132-Lead Pin-Grid Array (PGA) Package

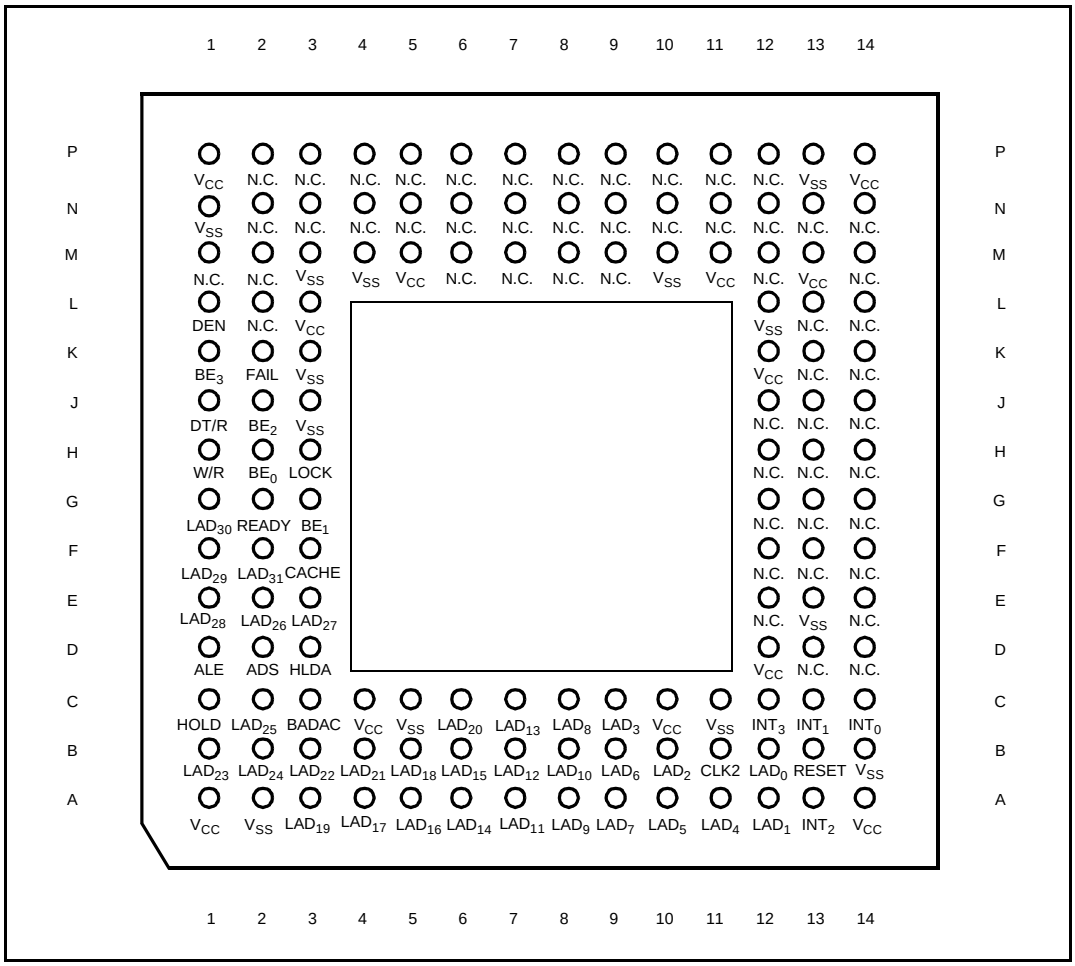


Figure 18. 80960KB PGA Pinout—View from Bottom (Pins Facing Up)

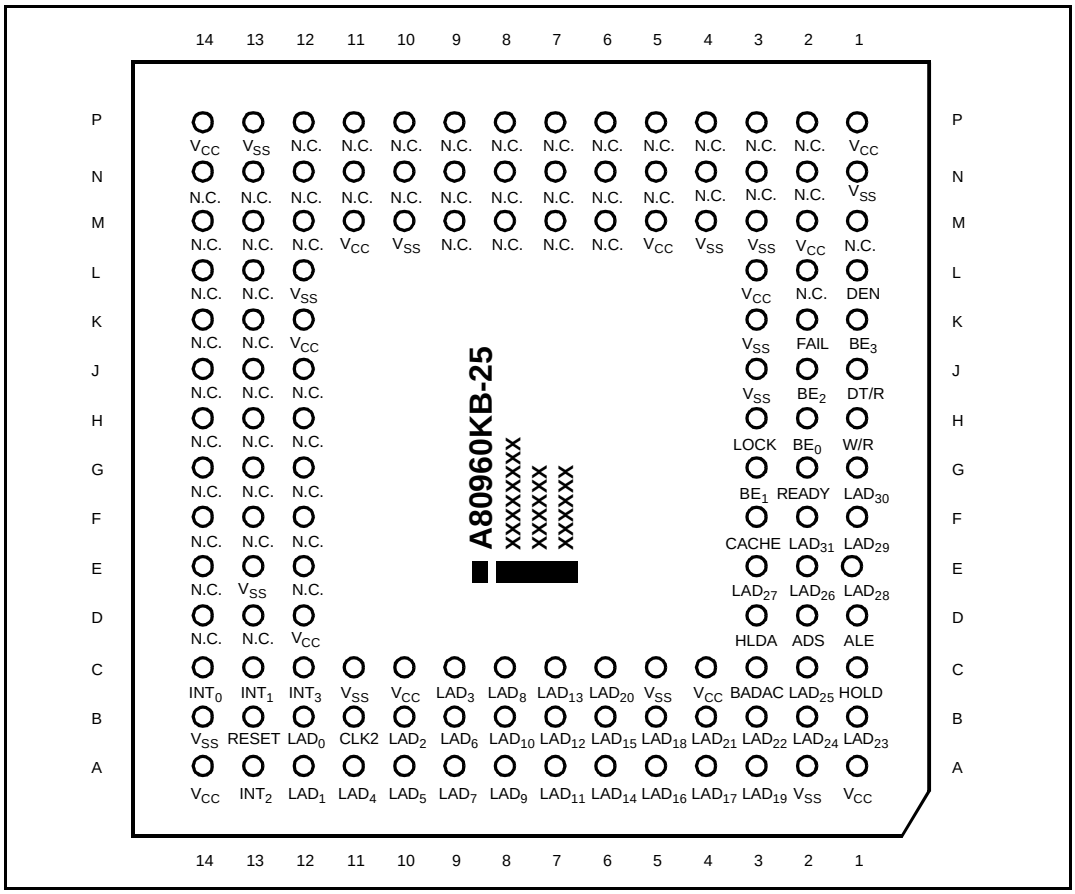


Figure 19. 80960KB PGA Pinout—View from Top (Pins Facing Down)

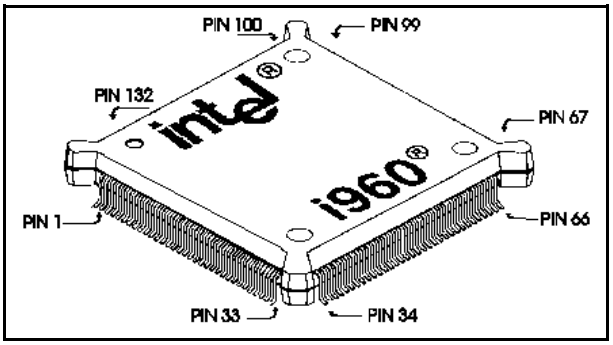


Figure 20. 80960KB 132-Lead Plastic Quad Flat-Pack (PQFP) Package

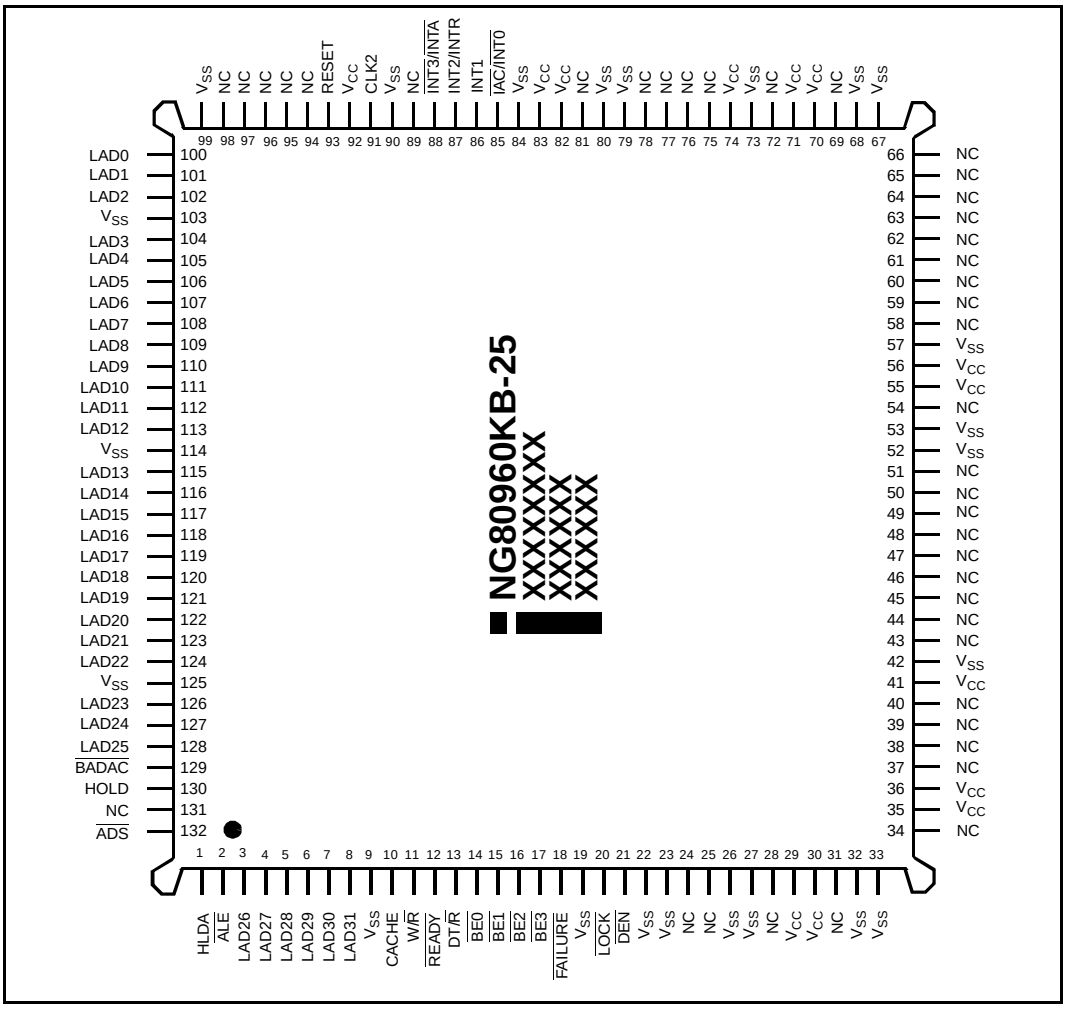


Figure 21. PQFP Pinout - View From Top

3.2. Pinout

Table 10. 80960KB PGA Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	V_{CC}	C6	LAD_{20}	H1	W/$\overline{R}$	M10	V_{SS}
A2	V_{SS}	C7	LAD_{13}	H2	$\overline{BE}_0$	M11	V_{CC}
A3	LAD_{19}	C8	LAD_8	H3	$\overline{LOCK}$	M12	N.C.
A4	LAD_{17}	C9	LAD_3	H12	N.C.	M13	N.C.
A5	LAD_{16}	C10	V_{CC}	H13	N.C.	M14	N.C.
A6	LAD_{14}	C11	V_{SS}	H14	N.C.	N1	V_{SS}
A7	LAD_{11}	C12	$\overline{INT}_3/\overline{INTA}$	J1	DT/$\overline{R}$	N2	N.C.
A8	LAD_9	C13	INT_1	J2	$\overline{BE}_2$	N3	N.C.
A9	LAD_7	C14	$\overline{IAC}/\overline{INT}_0$	J3	V_{SS}	N4	N.C.
A10	LAD_5	D1	$\overline{ALE}$	J12	N.C.	N5	N.C.
A11	LAD_4	D2	$\overline{ADS}$	J13	N.C.	N6	N.C.
A12	LAD_1	D3	HLDA	J14	N.C.	N7	N.C.
A13	INT_2/INTR	D12	V_{CC}	K1	$\overline{BE}_3$	N8	N.C.
A14	V_{CC}	D13	N.C.	K2	$\overline{FAILURE}$	N9	N.C.
B1	LAD_{23}	D14	N.C.	K3	V_{SS}	N10	N.C.
B2	LAD_{24}	E1	LAD_{28}	K12	V_{CC}	N11	N.C.
B3	LAD_{22}	E2	LAD_{26}	K13	N.C.	N12	N.C.
B4	LAD_{21}	E3	LAD_{27}	K14	N.C.	N13	N.C.
B5	LAD_{18}	E12	N.C.	L1	$\overline{DEN}$	N14	N.C.
B6	LAD_{15}	E13	V_{SS}	L2	N.C.	P1	V_{CC}
B7	LAD_{12}	E14	N.C.	L3	V_{CC}	P2	N.C.
B8	LAD_{10}	F1	LAD_{29}	L12	V_{SS}	P3	N.C.
B9	LAD_6	F2	LAD_{31}	L13	N.C.	P4	N.C.
B10	LAD_2	F3	CACHE	L14	N.C.	P5	N.C.
B11	CLK2	F12	N.C.	M1	N.C.	P6	N.C.
B12	LAD_0	F13	N.C.	M2	V_{CC}	P7	N.C.
B13	RESET	F14	N.C.	M3	V_{SS}	P8	N.C.
B14	V_{SS}	G1	LAD_{30}	M4	V_{SS}	P9	N.C.
C1	HOLD	G2	$\overline{READY}$	M5	V_{CC}	P10	N.C.
C2	LAD_{25}	G3	$\overline{BE}_1$	M6	N.C.	P11	N.C.
C3	$\overline{BADAC}$	G12	N.C.	M7	N.C.	P12	N.C.
C4	V_{CC}	G13	N.C.	M8	N.C.	P13	V_{SS}
C5	V_{SS}	G14	N.C.	M9	N.C.	P14	V_{CC}

NOTE: Do not connect any external logic to any pins marked N.C.

Table 11. 80960KB PGA Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
$\overline{ADS}$	D2	LAD_{15}	B6	N.C.	J14	N.C.	P9
$\overline{ALE}$	D1	LAD_{16}	A5	N.C.	K13	N.C.	P10
$\overline{BADAC}$	C3	LAD_{17}	A4	N.C.	K14	N.C.	P11
$\overline{BE}_0$	H2	LAD_{18}	B5	N.C.	L13	N.C.	P12
$\overline{BE}_1$	G3	LAD_{19}	A3	N.C.	L14	N.C.	L2
$\overline{BE}_2$	J2	LAD_{20}	C6	N.C.	M1	$\overline{READY}$	G2
$\overline{BE}_3$	K1	LAD_{21}	B4	N.C.	M6	RESET	B13
CACHE	F3	LAD_{22}	B3	N.C.	M7	V_{CC}	A1
CLK2	B11	LAD_{23}	B1	N.C.	M8	V_{CC}	A14
$\overline{DEN}$	L1	LAD_{24}	B2	N.C.	M9	V_{CC}	C4
DT/$\overline{R}$	J1	LAD_{25}	C2	N.C.	M12	V_{CC}	C10
$\overline{FAILURE}$	K2	LAD_{26}	E2	N.C.	M13	V_{CC}	D12
HLDA	D3	LAD_{27}	E3	N.C.	M14	V_{CC}	K12
HOLD	C1	LAD_{28}	E1	N.C.	N2	V_{CC}	L3
$\overline{IAC}/\overline{INT}_0$	C14	LAD_{29}	F1	N.C.	N3	V_{CC}	M2
INT_1	C13	LAD_{30}	G1	N.C.	N4	V_{CC}	M5
INT_2/INTR	A13	LAD_{31}	F2	N.C.	N5	V_{CC}	M11
$\overline{INT}_3/\overline{INTA}$	C12	$\overline{LOCK}$	H3	N.C.	N6	V_{CC}	P1
LAD_0	B12	N.C.	D13	N.C.	N7	V_{CC}	P14
LAD_1	A12	N.C.	D14	N.C.	N8	V_{SS}	A2
LAD_2	B10	N.C.	E12	N.C.	N9	V_{SS}	B14
LAD_3	C9	N.C.	E14	N.C.	N10	V_{SS}	C5
LAD_4	A11	N.C.	F12	N.C.	N11	V_{SS}	C11
LAD_5	A10	N.C.	F13	N.C.	N12	V_{SS}	E11
LAD_6	B9	N.C.	F14	N.C.	N13	V_{SS}	J3
LAD_7	A9	N.C.	G12	N.C.	N14	V_{SS}	K3
LAD_8	C8	N.C.	G13	N.C.	P2	V_{SS}	L12
LAD_9	A8	N.C.	G14	N.C.	P3	V_{SS}	M3
LAD_{10}	B8	N.C.	H12	N.C.	P4	V_{SS}	M4
LAD_{11}	A7	N.C.	H13	N.C.	P5	V_{SS}	M10
LAD_{12}	B7	N.C.	H14	N.C.	P6	V_{SS}	N1
LAD_{13}	C7	N.C.	J12	N.C.	P7	V_{SS}	P13
LAD_{14}	A6	N.C.	J13	N.C.	P8	W/$\overline{R}$	H1

NOTE: Do not connect any external logic to any pins marked N.C.

Table 12. 80960KB PQFP Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	HLDA	34	N.C.	67	V_{SS}	100	LAD_0
2	$\overline{ALE}$	35	V_{CC}	68	V_{SS}	101	LAD_1
3	LAD_{26}	36	V_{CC}	69	N.C.	102	LAD_2
4	LAD_{27}	37	N.C.	70	V_{CC}	103	V_{SS}
5	LAD_{28}	38	N.C.	71	V_{CC}	104	LAD_3
6	LAD_{29}	39	N.C.	72	N.C.	105	LAD_4
7	LAD_{30}	40	N.C.	73	V_{SS}	106	LAD_5
8	LAD_{31}	41	V_{CC}	74	V_{CC}	107	LAD_6
9	V_{SS}	42	V_{SS}	75	N.C.	108	LAD_7
10	CACHE	43	N.C.	76	N.C.	109	LAD_8
11	W/$\overline{R}$	44	N.C.	77	N.C.	110	LAD_9
12	$\overline{READY}$	45	N.C.	78	N.C.	111	LAD_{10}
13	DT/$\overline{R}$	46	N.C.	79	V_{SS}	112	LAD_{11}
14	$\overline{BE}_0$	47	N.C.	80	V_{SS}	113	LAD_{12}
15	$\overline{BE}_1$	48	N.C.	81	N.C.	114	V_{SS}
16	$\overline{BE}_2$	49	N.C.	82	V_{CC}	115	LAD_{13}
17	$\overline{BE}_3$	50	N.C.	83	V_{CC}	116	LAD_{14}
18	$\overline{FAILURE}$	51	N.C.	84	V_{SS}	117	LAD_{15}
19	V_{SS}	52	V_{SS}	85	$\overline{IAC}/\overline{INT}_0$	118	LAD_{16}
20	$\overline{LOCK}$	53	V_{SS}	86	INT_1	119	LAD_{17}
21	$\overline{DEN}$	54	N.C.	87	INT_2/INTR	120	LAD_{18}
22	V_{SS}	55	V_{CC}	88	$\overline{INT}_3/\overline{INTA}$	121	LAD_{19}
23	V_{SS}	56	V_{CC}	89	N.C.	122	LAD_{20}
24	N.C.	57	V_{SS}	90	V_{SS}	123	LAD_{21}
25	N.C.	58	N.C.	91	CLK2	124	LAD_{22}
26	V_{SS}	59	N.C.	92	V_{CC}	125	V_{SS}
27	V_{SS}	60	N.C.	93	RESET	126	LAD_{23}
28	N.C.	61	N.C.	94	N.C.	127	LAD_{24}
29	V_{CC}	62	N.C.	95	N.C.	128	LAD_{25}
30	V_{CC}	63	N.C.	96	N.C.	129	$\overline{BADAC}$
31	N.C.	64	N.C.	97	N.C.	130	HOLD
32	V_{SS}	65	N.C.	98	N.C.	131	N.C.
33	V_{SS}	66	N.C.	99	V_{SS}	132	$\overline{ADS}$

NOTE: Do not connect any external logic to any pins marked N.C.

Table 13. 80960KB PQFP Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
$\overline{ADS}$	132	LAD_{15}	117	N.C.	49	V_{CC}	41
$\overline{ALE}$	2	LAD_{16}	118	N.C.	50	V_{CC}	55
$\overline{BADAC}$	129	LAD_{17}	119	N.C.	51	V_{CC}	56
$\overline{BE}_0$	14	LAD_{18}	120	N.C.	54	V_{CC}	70
$\overline{BE}_1$	15	LAD_{19}	121	N.C.	58	V_{CC}	71
$\overline{BE}_2$	16	LAD_{20}	122	N.C.	59	V_{CC}	74
$\overline{BE}_3$	17	LAD_{21}	123	N.C.	60	V_{CC}	82
CACHE	10	LAD_{22}	124	N.C.	61	V_{CC}	83
CLK2	91	LAD_{23}	126	N.C.	62	V_{CC}	92
$\overline{DEN}$	21	LAD_{24}	127	N.C.	63	V_{SS}	9
DT/$\overline{R}$	13	LAD_{25}	128	N.C.	64	V_{SS}	19
$\overline{FAILURE}$	18	LAD_{26}	3	N.C.	65	V_{SS}	22
HLDA	1	LAD_{27}	4	N.C.	66	V_{SS}	23
HOLD	130	LAD_{28}	5	N.C.	69	V_{SS}	26
$\overline{IAC}/\overline{INT}_0$	85	LAD_{29}	6	N.C.	72	V_{SS}	27
INT_1	86	LAD_{30}	7	N.C.	75	V_{SS}	32
INT_2/INTR	87	LAD_{31}	8	N.C.	76	V_{SS}	33
$\overline{INT}_3/\overline{INTA}$	88	$\overline{LOCK}$	20	N.C.	77	V_{SS}	42
LAD_0	100	N.C.	24	N.C.	78	V_{SS}	52
LAD_1	101	N.C.	25	N.C.	81	V_{SS}	53
LAD_2	102	N.C.	28	N.C.	89	V_{SS}	57
LAD_3	104	N.C.	31	N.C.	94	V_{SS}	67
LAD_4	105	N.C.	34	N.C.	95	V_{SS}	68
LAD_5	106	N.C.	37	N.C.	96	V_{SS}	73
LAD_6	107	N.C.	38	N.C.	97	V_{SS}	79
LAD_7	108	N.C.	39	N.C.	98	V_{SS}	80
LAD_8	109	N.C.	40	N.C.	131	V_{SS}	84
LAD_9	110	N.C.	43	$\overline{READY}$	12	V_{SS}	90
LAD_{10}	111	N.C.	44	RESET	93	V_{SS}	99
LAD_{11}	112	N.C.	45	V_{CC}	29	V_{SS}	103
LAD_{12}	113	N.C.	46	V_{CC}	30	V_{SS}	114
LAD_{13}	115	N.C.	47	V_{CC}	35	V_{SS}	125
LAD_{14}	116	N.C.	48	V_{CC}	36	W/$\overline{R}$	11

NOTE: Do not connect any external logic to any pins marked N.C.

3.3. Package Thermal Specification

The 80960KB is specified for operation when case temperature is within the range 0°C to 85°C (PGA) or 0°C to 100°C (PQFP). Measure case temperature at the top center of the package. Ambient temperature can be calculated from:

$T_J = T_C + P*\theta_{jc}$

$T_A = T_J + P*\theta_{ja}$

$T_C = T_A + P*[\theta_{ja}–\theta_{jc}]$

Values for θ_{ja} and θ_{jc} for various airflows are given in Table 12 for the PGA package and in Table 12 for the PQFP package. The PGA's θ_{ja} can be reduced by adding a heatsink. For the PQFP, however, a heatsink is not generally used since the device is intended to be surface mounted.

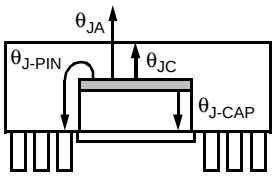
Maximum allowable ambient temperature (T_A) permitted without exceeding T_C is shown by the graphs in Figures 23, 24, 25 and 26. The curves assume the maximum permitted supply current (I_{CC}) at each speed, V_{CC} of +5.0 V and a T_{CASE} of +85°C (PGA) or +100°C (PQFP).

If the 80960KB is to be used in a harsh environment where the ambient temperature may exceed the limits for the normal commercial part, consider using an extended temperature device. These components are designated by the prefix "TA" and are available at 16, 20 and 25 MHz in the ceramic PGA package. Extended operating temperature range is –40° C to +125°C (case).

Figure 26 shows the maximum allowable ambient temperature for the 20 MHz extended temperature TA80960KB at various airflows. The curve assumes an I_{CC} of 420 mA, V_{CC} of 5.0 V and a T_{CASE} of +125°C.

Table 14. 80960KB PGA Package Thermal Characteristics

Thermal Resistance — °C/Watt							
Parameter	Airflow — ft./min (m/sec)						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ Junction-to-Case	2	2	2	2	2	2	2
θ Case-to-Ambient (No Heatsink)	19	18	17	15	12	10	9
θ Case-to-Ambient (Omnidirectional Heatsink)	16	15	14	12	9	7	6
θ Case-to-Ambient (Unidirectional Heatsink)	15	14	13	11	8	6	5



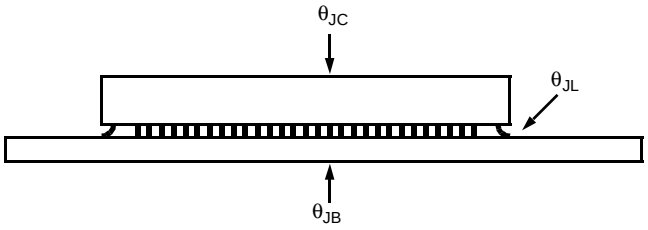
NOTES:

1. This table applies to 80960KB PGA plugged into socket or soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. $\theta_{J\text{-}CAP}$ = 4°C/W (approx.)
   $\theta_{J\text{-}PIN}$ = 4°C/W (inner pins) (approx.)
   $\theta_{J\text{-}PIN}$ = 8°C/W (outer pins) (approx.)

Table 15. 80960KB PQFP Package Thermal Characteristics

Thermal Resistance — °C/Watt							
Parameter	**Airflow — ft./min (m/sec)**						
	0 (0)	**50 (0.25)**	**100 (0.50)**	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**	**800 (4.06)**
θ Junction-to-Case	9	9	9	9	9	9	9
θ Case-to-Ambient (No Heatsink)	22	19	18	16	11	9	8

NOTES:
1. This table applies to 80960KB PQFP soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. θ_{JL} = 18°C/W (approx.)
   θ_{JB} = 18°C/W (approx.)



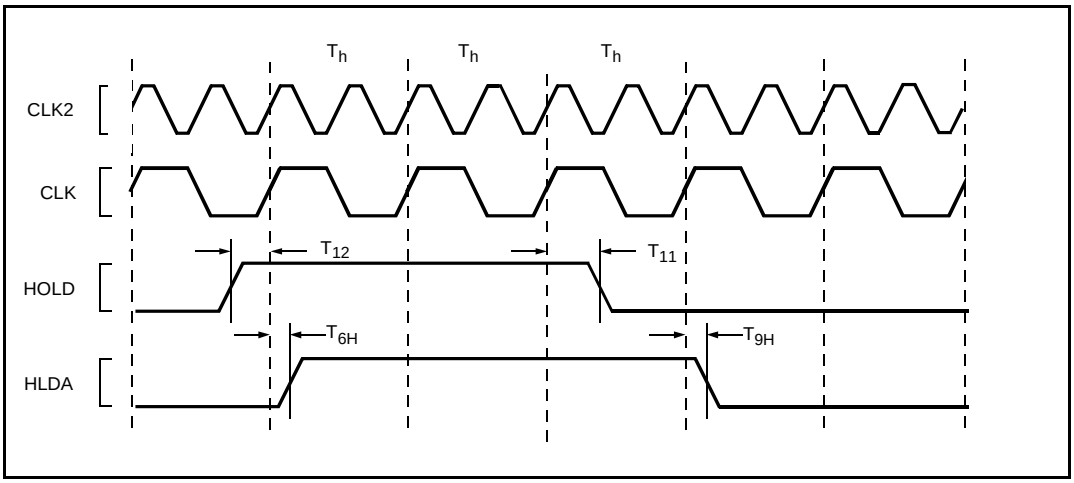


Figure 22. HOLD Timing

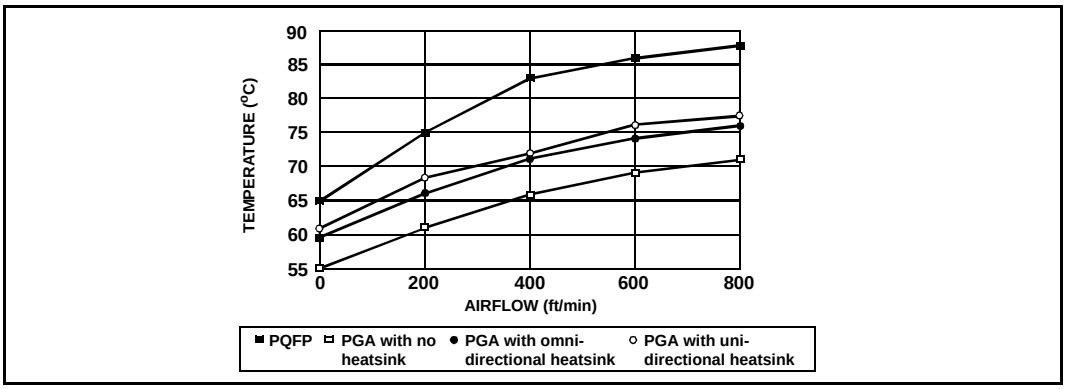


Figure 23. 16 MHz Maximum Allowable Ambient Temperature

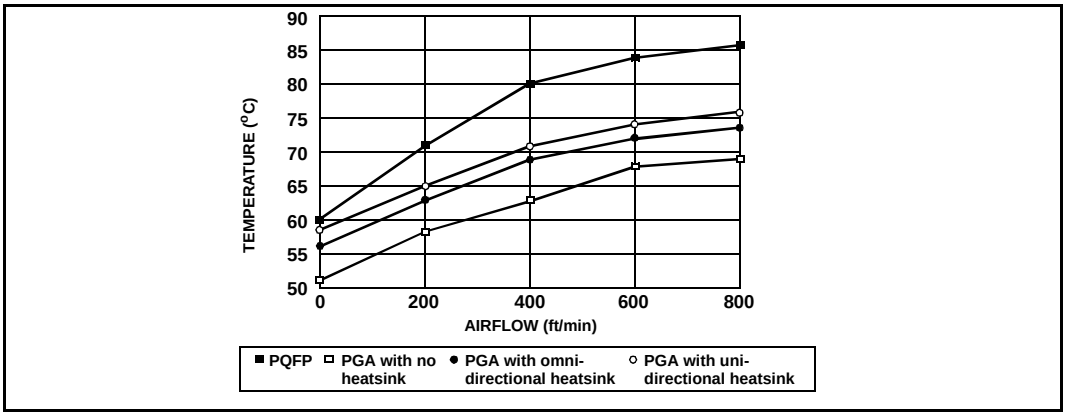


Figure 24. 20 MHz Maximum Allowable Ambient Temperature

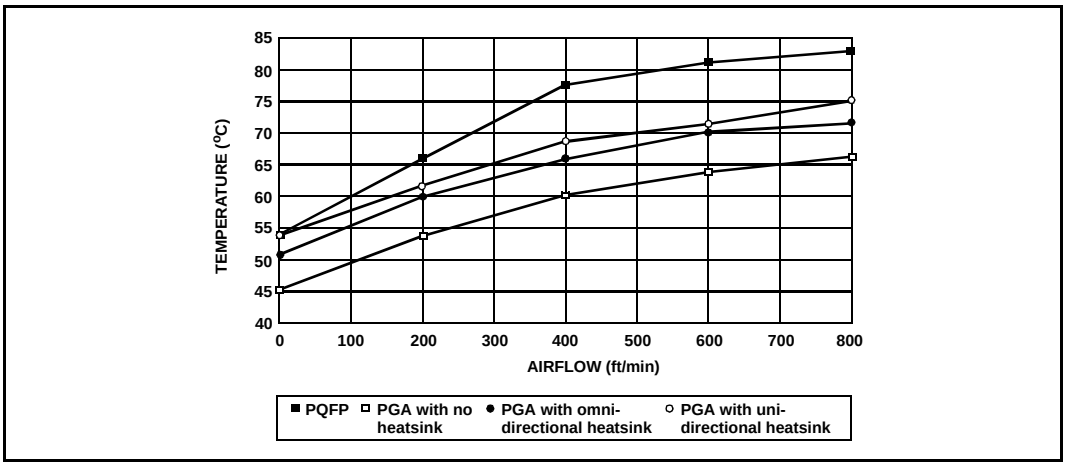


Figure 25. 25 MHz Maximum Allowable Ambient Temperature

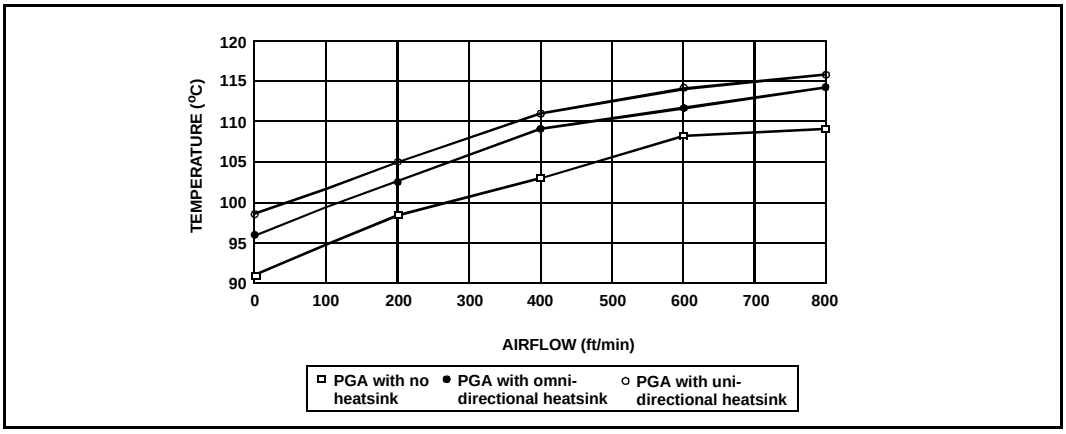


Figure 26. Maximum Allowable Ambient Temperature for the Extended Temperature TA-80960KB at 20 MHz in PGA Package

4.0 WAVEFORMS

Figures 27, 28, 29 and 30 show the waveforms for various transactions on the 80960KB's local bus.

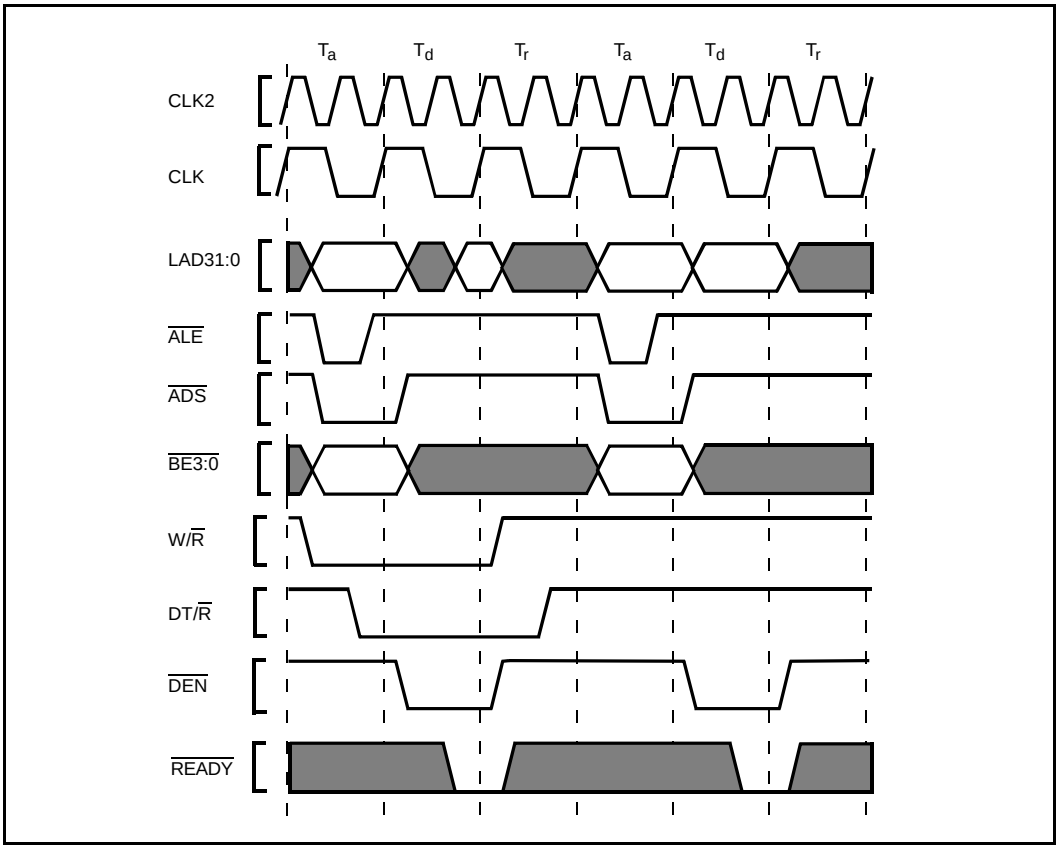


Figure 27. Non-Burst Read and Write Transactions Without Wait States

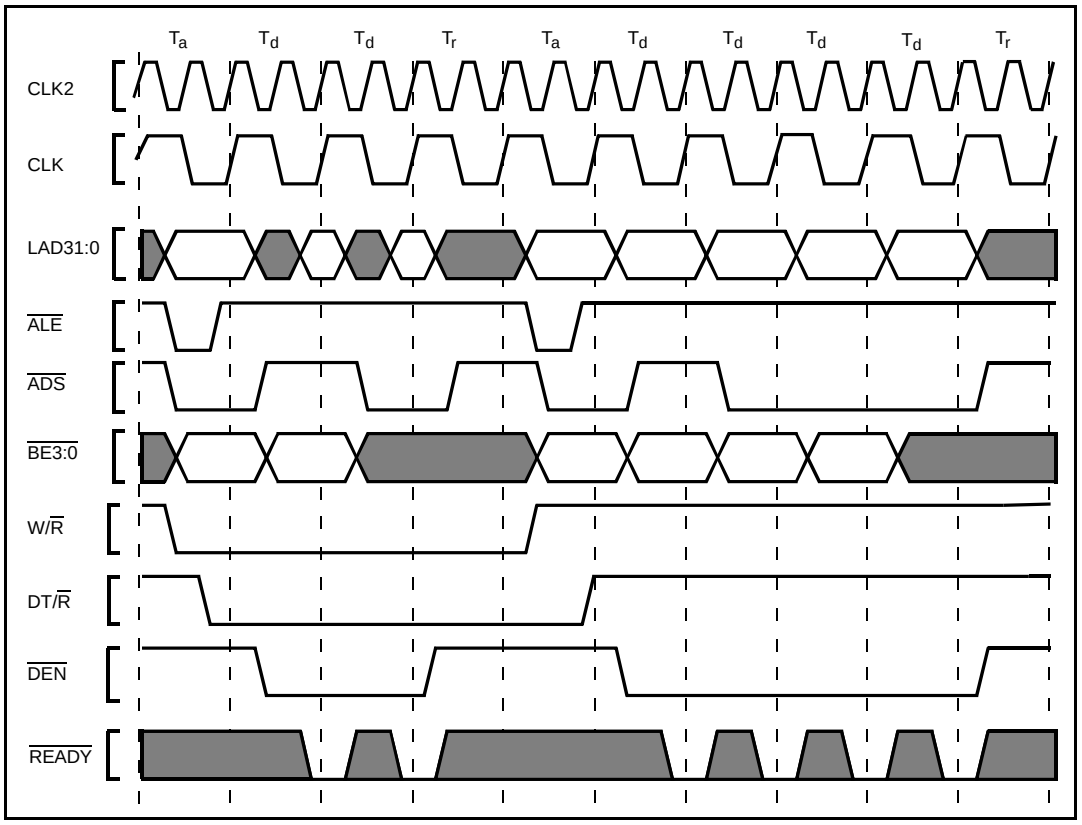


Figure 28. Burst Read and Write Transaction Without Wait States

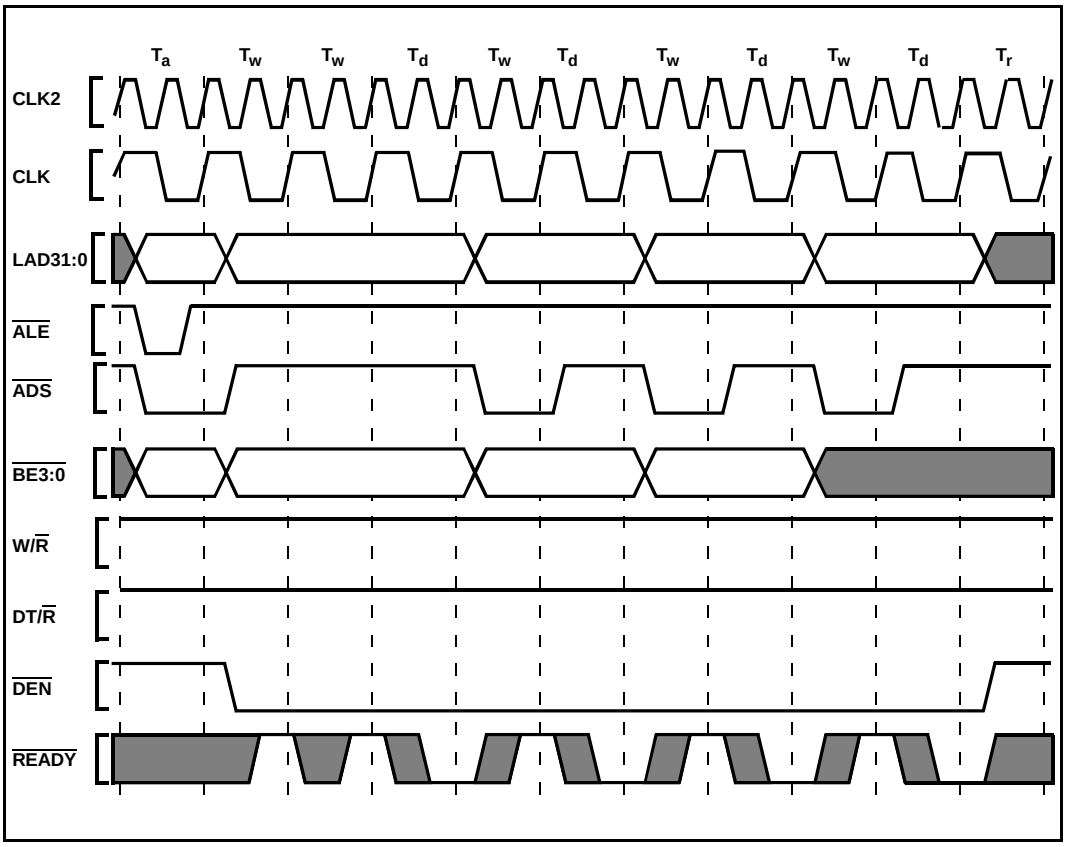


Figure 29. Burst Write Transaction with 2, 1, 1, 1 Wait States

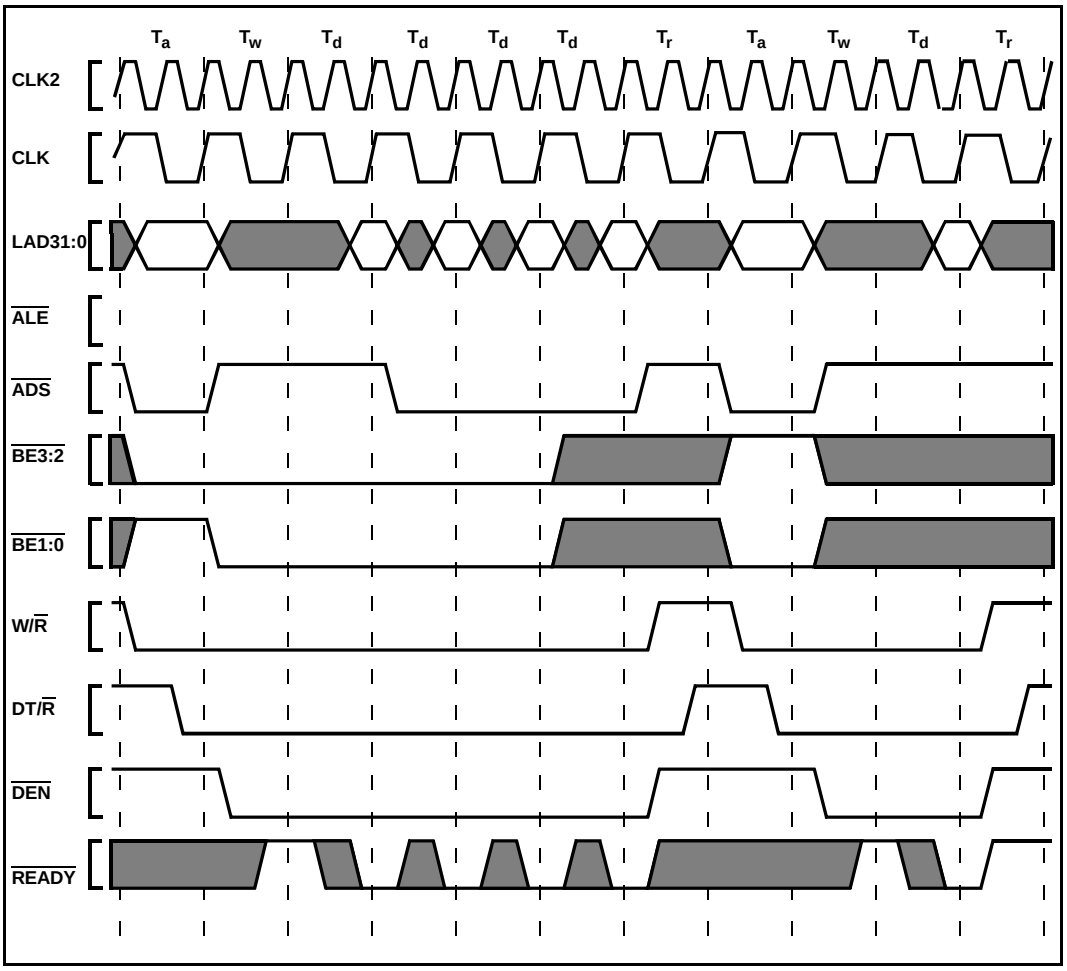
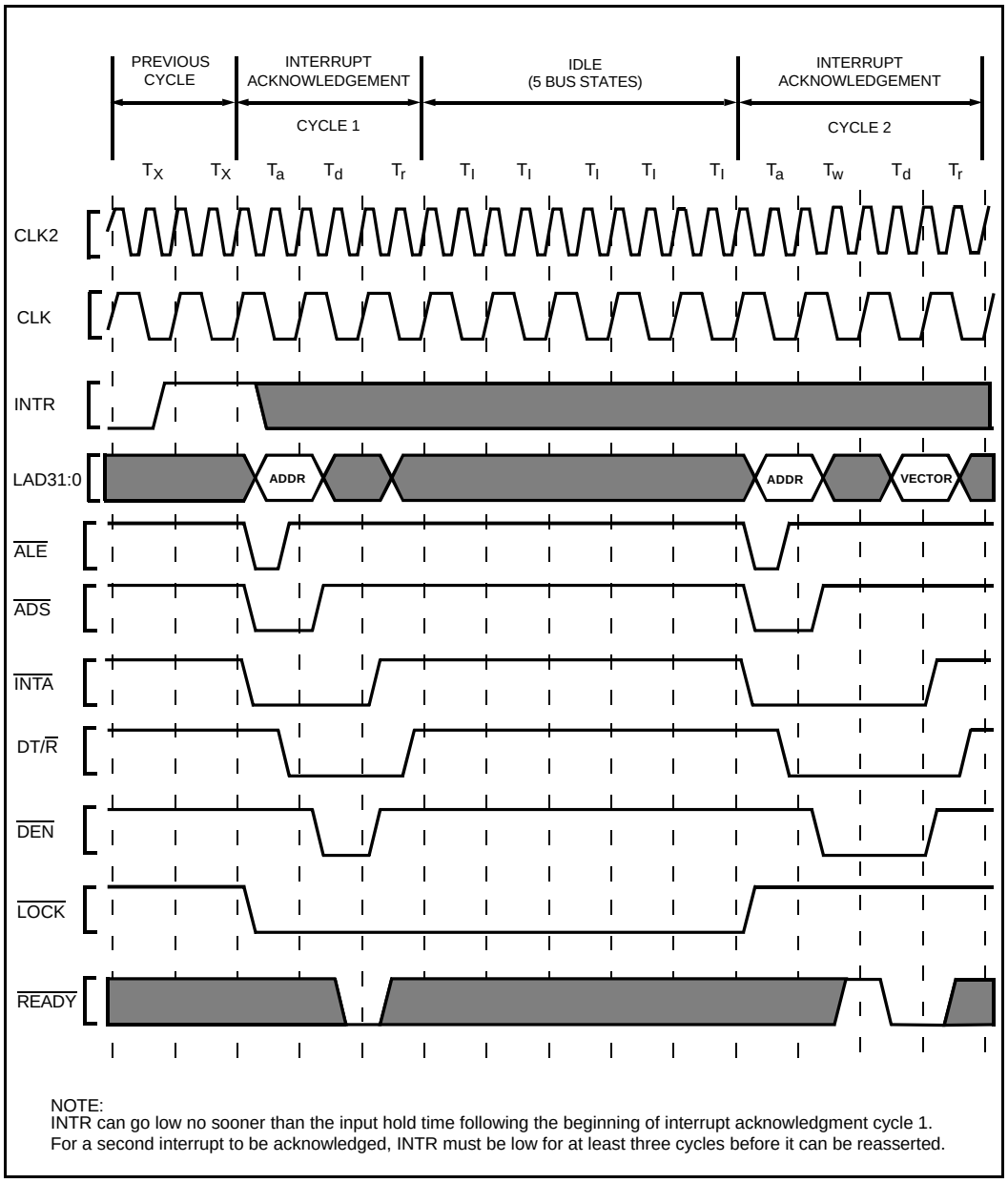


Figure 30. Accesses Generated by Quad Word Read Bus Request, Misaligned Two Bytes from Quad Word Boundary (1, 0, 0, 0 Wait States)



NOTE:
INTR can go low no sooner than the input hold time following the beginning of interrupt acknowledgment cycle 1. For a second interrupt to be acknowledged, INTR must be low for at least three cycles before it can be reasserted.

Figure 31. Interrupt Acknowledge Transaction

5.0 REVISION HISTORY

No revision history was maintained in earlier revisions of this data sheet. All errata that has been identified to date is incorporated into this revision. The sections significantly changed since the previous revision are:

Section	Last Rev.	Description
Table 4. 80960KB Pin Description: L-Bus Signals (pg. 8)	-005	$\overline{\text{LOCK}}$ pin description rewritten for clarity.
2.3. Connection Recommendations (pg. 11)	-005	Changed suggested open-drain termination networks to reflect more realistic operating conditions with reduction in DC power consumption.
Figure 9. Typical Current vs. Frequency (Hot Temp) (pg. 13)	-005	Added figure for typical power supply current at hot temperature to aid thermal analysis.
Figure 12. Test Load Circuit for Three-State Output Pins (pg. 14) Figure 13. Test Load Circuit for Open-Drain Output Pins (pg. 14)	-005	All outputs now specified with standard 50 pF test loads to agree with actual test methodology.
2.7. DC Characteristics (pg. 15)	-005	ICC max specification reduced: **WAS:** 375 mA, 420 mA, 480 mA **IS:** 315 mA, 360 mA, 420 mA **AT:** 16 MHz, 20 MHz, 25 MHz Figures 7, 8, 9, 23, 24, 25 and 26 have also been changed accordingly.
2.8. AC Specifications (pg. 16)	-005	25 MHz operation extended to product in PQFP package. T_8 min. improved at all frequencies from 0 ns to 2 ns and T_8 max. improved from 20 ns to 18 ns. T_{8H} max improvement: **WAS:** 31ns, 26ns, 24ns **IS:** 28ns, 23ns, 23ns **AT:** 16 MHz, 20 MHz, 25 MHz
Functional Waveforms	-005	Redrawn for clarity. CLK signal drawn with more likely phase relationship to CLK2. Open-drain output signals drawn to show correct inactive states.
Various	-005	Deleted all references to 10 MHz. Intel no longer offers a 10 MHz 80960KB device.