M87C51FB
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 16 KBYTES USER PROGRAMMABLE EPROM

Military

M87C51FB — 3.5 MHz to 12 MHz, V_{CC} = 5V ±20%
M87C51FB-16 — 3.5 MHz to 16 MHz, V_{CC} = 5V ±20%

- **High Performance CHMOS EPROM**
- **Three 16-Bit Timer/Counters**
- **Programmable Counter Array with:**
  - **— High Speed Output,**
  - **— Compare/Capture,**
  - **— Pulse Width Modulator,**
  - **— Watchdog Timer capabilities**
- **Up/Down Timer/Counter**
- **Three Level Program Lock System**
- **16K On-Chip EPROM**
- **256 Bytes of On-Chip Data RAM**
- **Improved Quick Pulse Programming Algorithm**
- **Boolean Processor**
- **ONCE (On-Circuit Emulation) Mode**
- **Available in 40-pin CERDIP and 44-pin Leadless Chip Carrier Packages**
- **Gullwing and J-lead Packages Also Available**
- **32 Programmable I/O Lines**
- **7 Interrupt Sources**
- **Programmable Serial Channel with:**
  - **— Framing Error Detection**
  - **— Automatic Address Recognition**
- **TTL and CMOS Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **MCS® 51 Microcontroller Fully Compatible Instruction Set**
- **Power Saving Idle and Power Down Modes**
- **Military Temperature Range: −55°C to +125°C (T_C)**

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 16 Kbytes of the program memory can reside in the on-chip EPROM. In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 256 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel M87C51FB is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. Being a member of the MCS 51 family of microcontrollers, the M87C51FB uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS 51 microcontroller family of products. The M87C51FB is an enhanced version of the M87C51. Its added features make it an even more powerful microcontroller for applications that require Pulse Width Modulation, High Speed I/O, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

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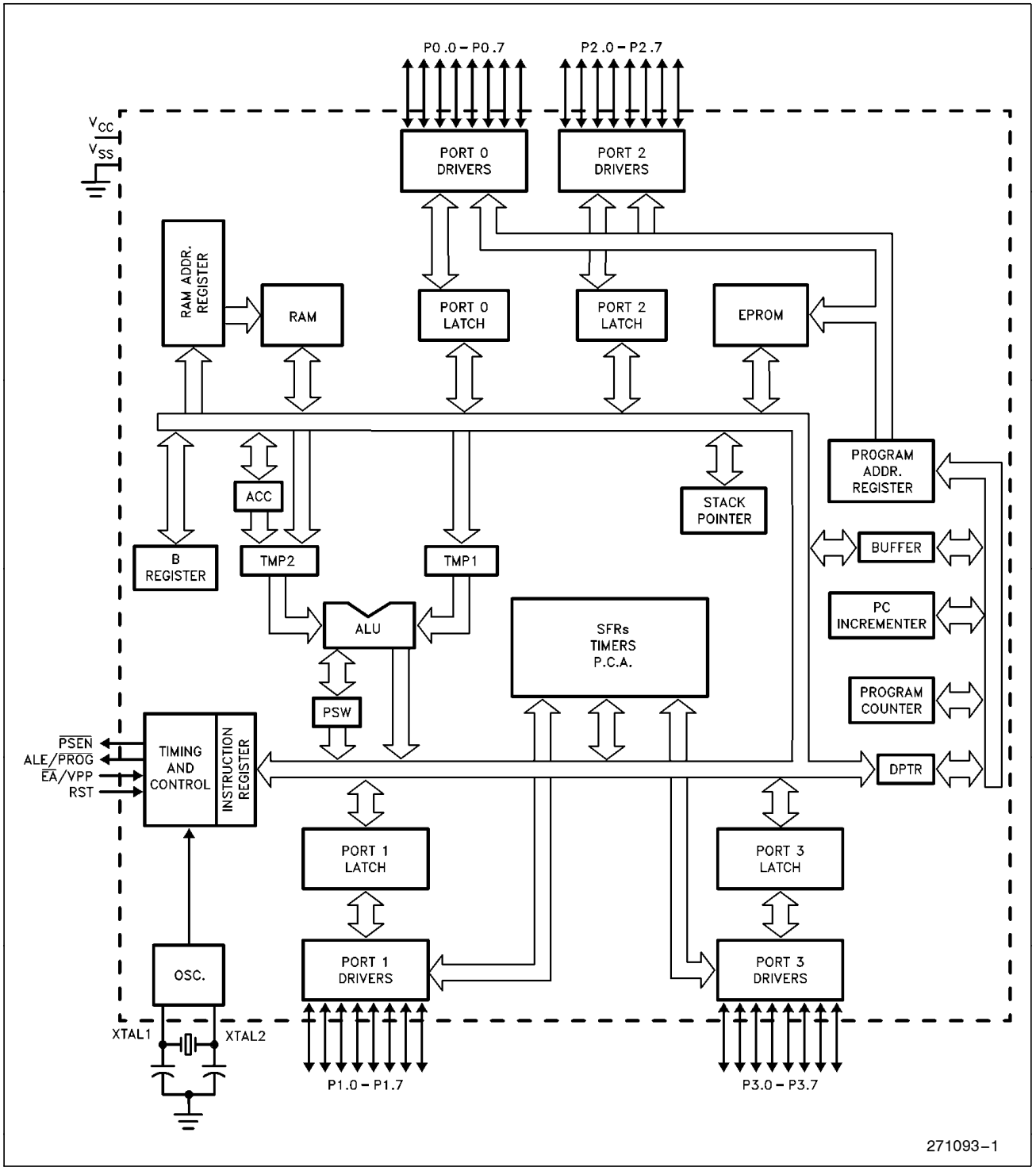


Figure 1. M87C51FB Block Diagram

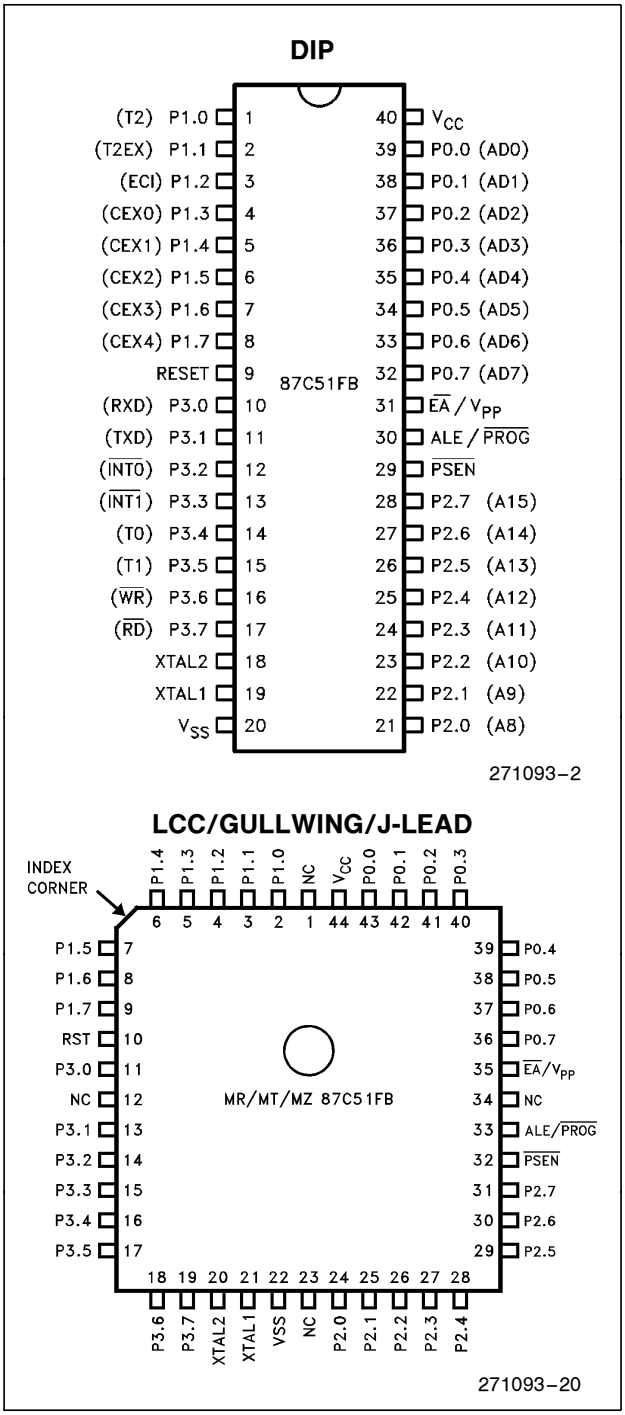


Figure 2. M87C51FB Pin Connections

PIN DESCRIPTIONS

V_{CC}: Supply voltage.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting1's, and can source and sink several LS TTL inputs.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullup resistors are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

In addition, Port 1 serves the functions of the following special features of the M87C51FB:

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2)
P1.1	T2EX (Timer/Counter 2 Capture/ Reload Trigger and Direction Control)
P1.2	ECI (External Count Input to the PCA)
P1.3	CEX0 (External I/O for Compare/ Capture Module 0)
P1.4	CEX1 (External I/O for Compare/ Capture Module 1)
P1.5	CEX2 (External I/O for Compare/ Capture Module 2)
P1.6	CEX3 (External I/O for Compare/ Capture Module 3)
P1.7	CEX4 (External I/O for Compare/ Capture Module 4)

Port 1 receives the low-order address bytes during EPROM programming and verifying.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Some Port 2 pins receive the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the M8051 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE: Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin (ALE/$\overline{PROG}$) is also the program pulse input during EPROM programming for the M87C51FB.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE/$\overline{PROG}$ pin, and the pin will be referred to as the ALE/$\overline{PROG}$ pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the M87C51FB is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to VSS in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFFH. Note, however, that if either of the Program Lock bits are programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the programming supply voltage (V_{PP}) during EPROM programming.

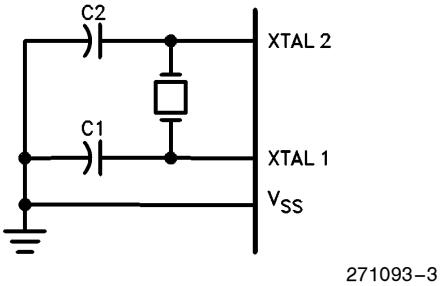
XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.



C1, C2 = 30 pF ±10 pF for Crystals
= 10 pF for Ceramic Resonators

Figure 3. Oscillator Connections

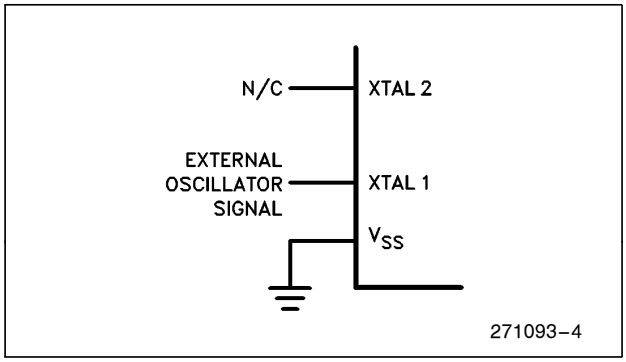


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs. The PCA timer/counter can optionally be left running or paused during Idle Mode.

POWER DOWN MODE

To save even more power, a Power Down Mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down Mode is terminated.

On the M87C51FB either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that puts the device into Power Down.

DESIGN CONSIDERATION

- Ambient light is known to affect the internal RAM contents during operation. If the M87C51FB application requires the part to be run under ambient lighting, an opaque label should be placed over the window to exclude light.
- When the Idle Mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

ONCE MODE

The ONCE (''On-Circuit Emulation'') Mode facilitates testing and debugging of systems using the M87C51FB without the M87C51FB having to be removed from the circuit. The ONCE Mode is invoked by:

1) Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2) Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the M87C51FB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to Application Note AP-255, ''Designing with the M80C51BH''.

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias
. . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on $\overline{EA}/V_{PP}$ Pin to V_{SS} . . . . . 0V to +13.0V
Voltage on Any Other Pin to V_{SS} . . −0.5V to +6.5V
Maximum I_{OL} Per I/O Pin . . . . . 15 mA
Power Dissipation 1.5W
(based on PACKAGE heat transfer limitations, not device power consumption)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions

Symbol	Description	Min	Max	Unit
T_C	Case Temperature (Instant On)	−55	+125	°C
V_{CC}	Digital Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency	3.5	16	MHz

DC CHARACTERISTICS: (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.2 V_{CC} − 0.1	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage(5) (Ports 1, 2, and 3)		0.3	V	I_{OL} = 100 μA (Note 1)
			0.45	V	I_{OL} = 1.6 mA (Note 1)
			1.0	V	I_{OL} = 3.5 mA (Notes 1, 4)
V_{OL1}	Output Low Voltage(5) (Port 0, ALE, $\overline{PSEN}$)		0.3	V	I_{OL} = 200 μA (Note 1)
			0.45	V	I_{OL} = 3.2 mA (Note 1)
			1.0	V	I_{OL} = 7.0 mA (Note 1, 4)
V_{OH}	Output High Voltage (Ports 1, 2, and 3)	V_{CC} − 0.3		V	I_{OH} = −10 μA
		V_{CC} − 0.7		V	I_{OH} = −30 μA
		V_{CC} − 1.5		V	I_{OH} = −60 μA

DC CHARACTERISTICS: (Over Specified Operating Conditions) (Continued)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	$V_{CC}-0.3$		V	$I_{OH} = -200\ \mu A$ (Note 2)
		$V_{CC}-0.7$		V	$I_{OH} = -3.2$ mA
		$V_{CC}-1.5$		V	$I_{OH} = -7.0$ mA (Note 4)
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)		−75	μA	$V_{IN} = 0.45V$
I_{LI}	Input leakage Current (Port 0)		±10	μA	$0.45V < V_{IN} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3)		−750	μA	$V_{IN} = 2V$
RRST	RST Pulldown Resistor	40	225	KΩ	
CIO	Pin Capacitance		10	pF	@1 MHz, 25°C
I_{CC}	Power Supply Current: Active Mode @ 16 MHz Idle Mode @ 16 MHz Power Down Mode @ 16 MHz		 45 15 130	 mA mA μA	(Note 3)

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pFs, the noise pulse on the ALE signal may exceed 0.8V. In these cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an Address Latch with a Schmitt Trigger Strobe input.
2. Capacitive loading on Ports 0 and 2 cause the V_{OH} on ALE and $\overline{PSEN}$ to drop below the V_{CC} − 0.3 specification when the address lines are stabilizing.
3. See Figures 5–8 for load circuits. Minimum V_{CC} for Power Down is 2V.
4. Care must be taken not to exceed the maximum allowable power dissipation.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port—
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

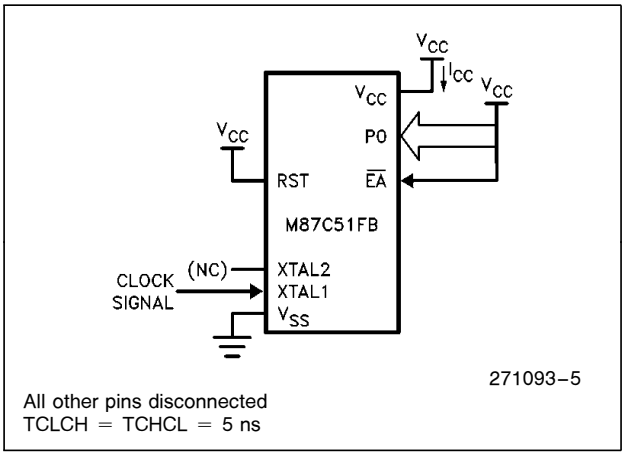


Figure 5. I_{CC} Load Circuit Active Mode

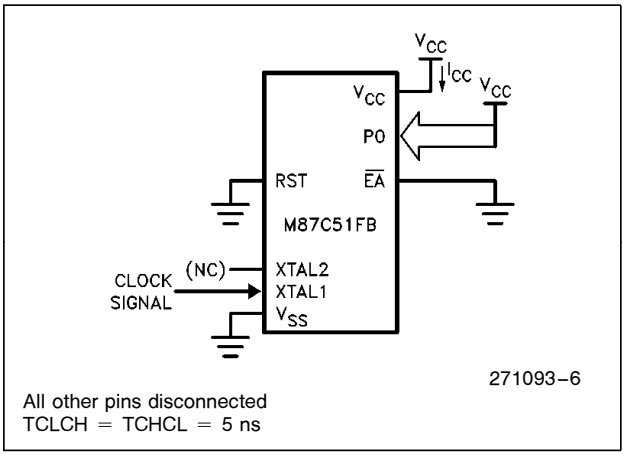


Figure 6. I_{CC} Load Circuit Idle Mode

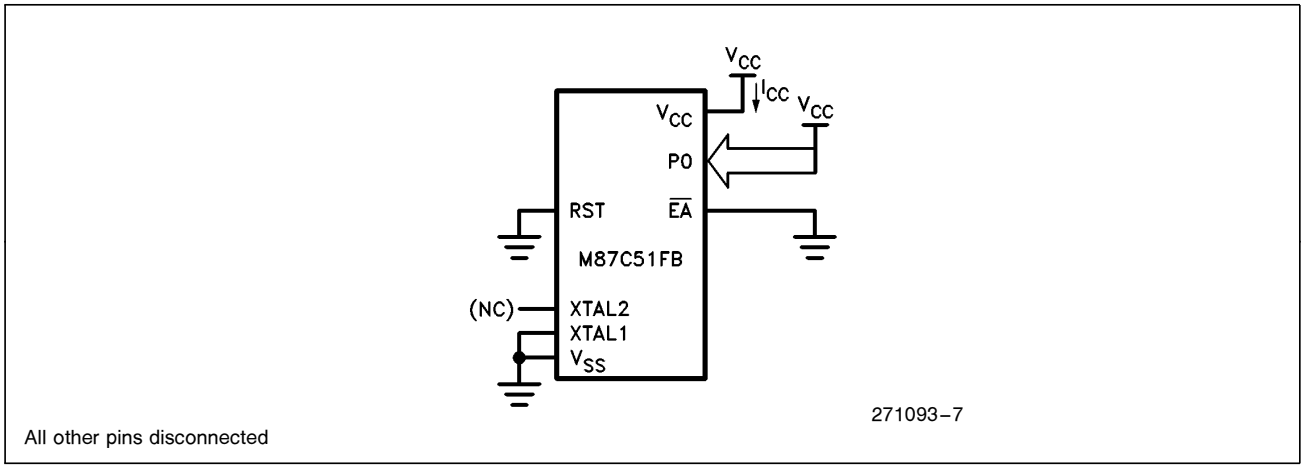


Figure 7. I_{CC} Load Circuit Power Down Mode. V_{CC} = 2.0V to 5.5V.

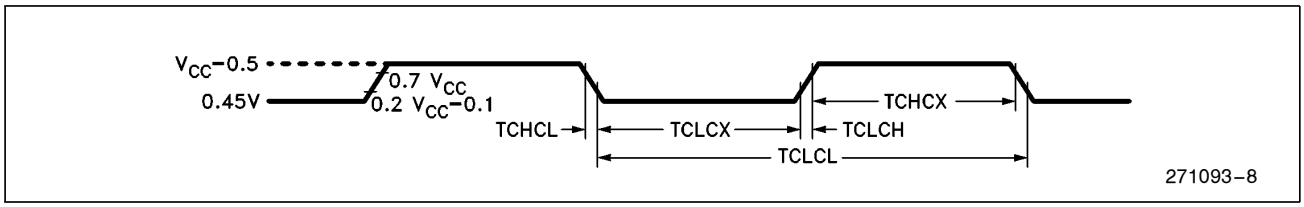


Figure 8. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
I: Instruction (program memory contents)
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: $\overline{\text{RD}}$ signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

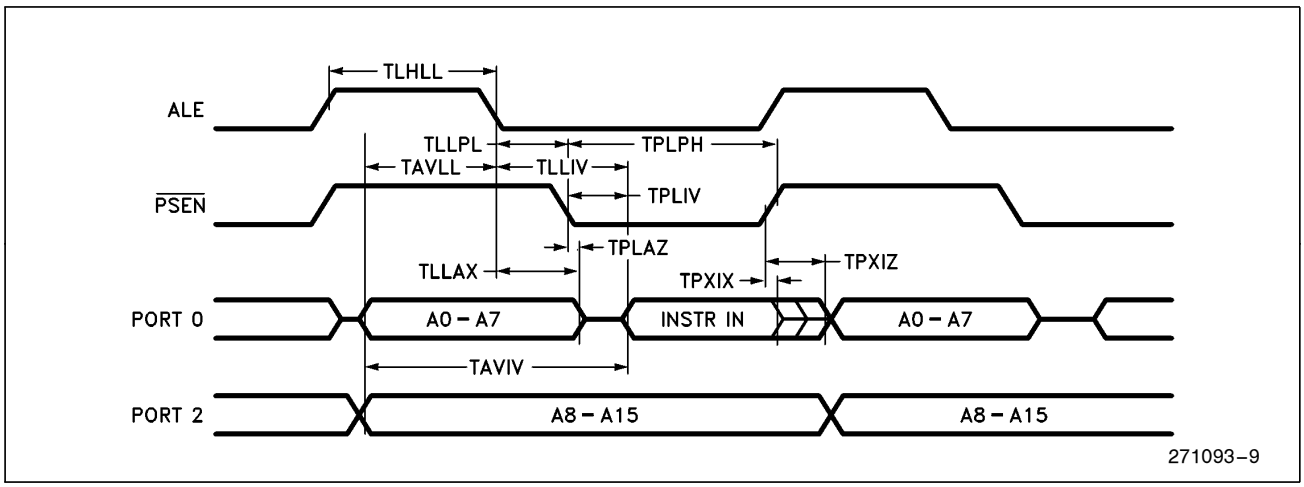
AC CHARACTERISTICS (Over Specified Operating Conditions)

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

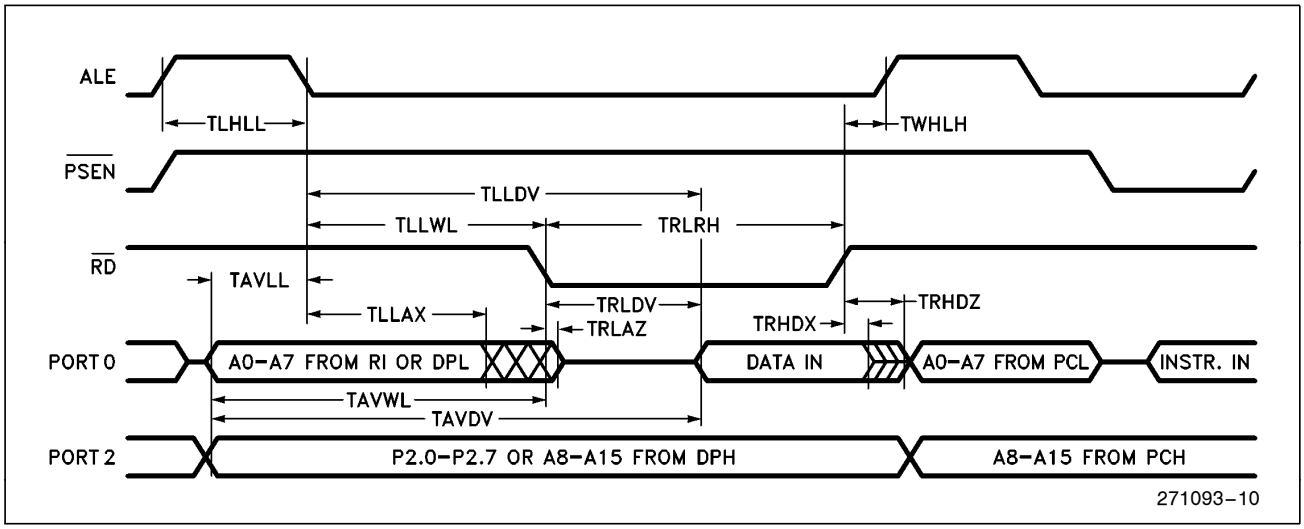
Symbol	Parameter	12 MHz Oscillator		16 MHz Oscillator		Variable Oscillator		Unit
		Min	Max	Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 87C51FB 87C51FB-16					 3.5 3.5	 12 16	MHz
TLHLL	ALE Pulse Width	127		85		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	43		23		TCLCL−40		ns
TLLAX	Address Hold After ALE Low	53		33		TCLCL−30		ns
TLLIV	ALE Low to Valid Instruction In		234		150		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	53		33		TCLCL−30		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		143		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		83		3TCLCL−105	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		59		38		TCLCL−25	ns
TAVIV	Address to Valid Instruction In		312		208		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		275		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		275		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		147.5		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		107		65		2TCLCL−60	ns
TLLDV	ALE Low to Valid Data In		517		350		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		398		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	138	238	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address Valid to $\overline{WR}$ Low	203		120		4TCLCL−130		ns
TQVWX	Data Valid before $\overline{WR}$	33		13		TCLCL−50		ns
TWHQX	Data Hold after $\overline{WR}$	33		13		TCLCL−50		ns
TQVWH	Data Valid to $\overline{WR}$ High	433		288		7TCLCL−150		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	23	103	TCLCL−40	TCLCL+40	ns

NOTE:
7. Case temperatures are ‘‘instant on’’.

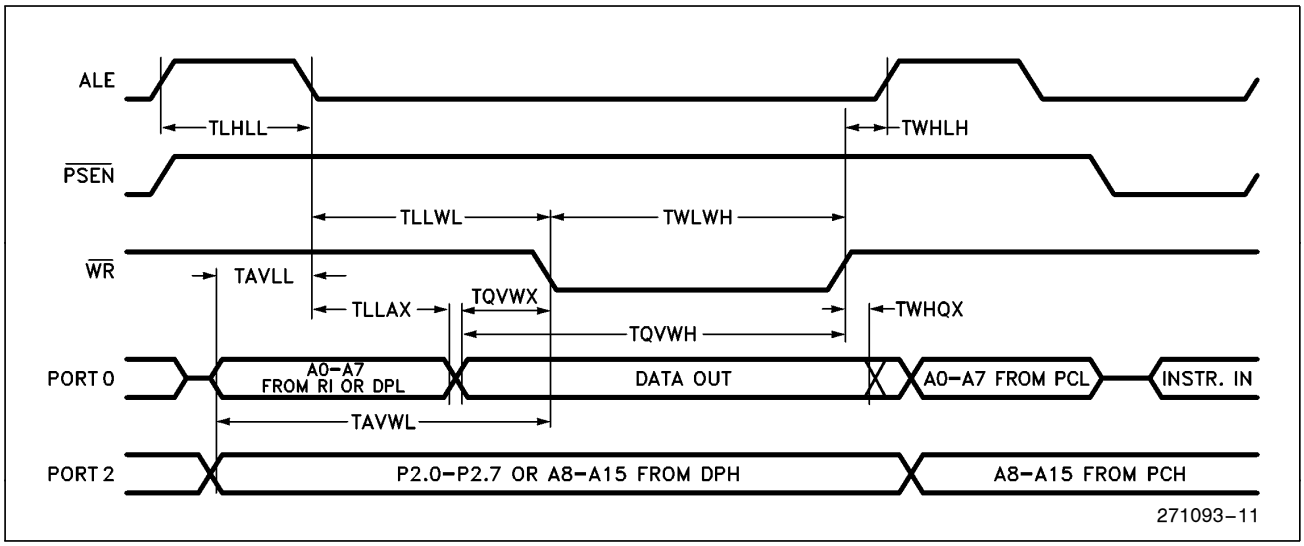
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

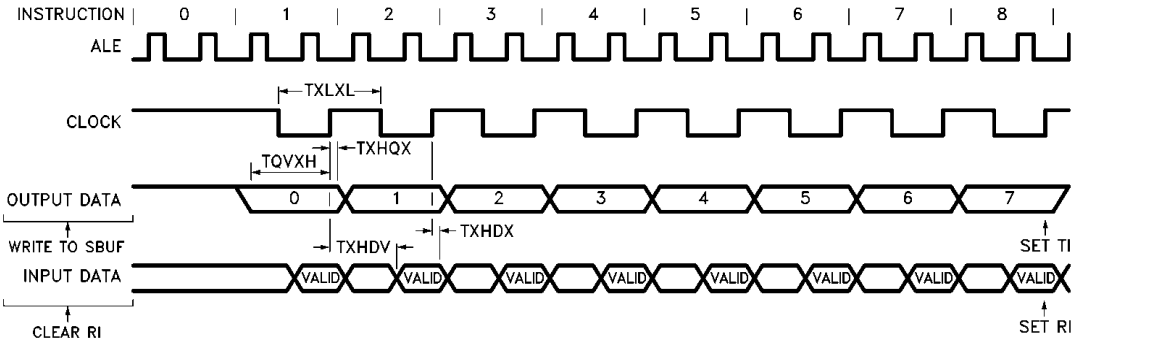


SERIAL PORT TIMING - SHIFT REGISTER MODE

Test Conditions: (Over Specified Operating Conditions)

Symbol	Parameter	12 MHz Oscillator		16 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1		0.75		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		492		10TCLCL − 133		ns
TXHQX	Output Data Hold after Clock Rising Edge	50		8		2TCLCL − 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		492		10TCLCL − 133	ns

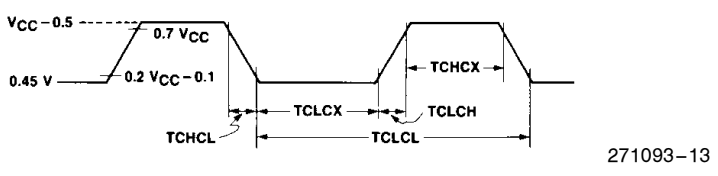
SHIFT REGISTER MODE TIMING WAVEFORMS



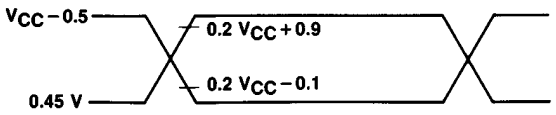
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 87C51FB 87C51FB-16	 3.5 3.5	 12 16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

EXTERNAL CLOCK DRIVE WAVEFORM



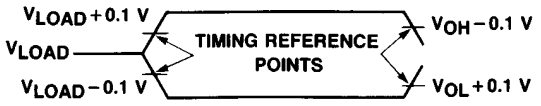
AC TESTING INPUT, OUTPUT WAVEFORMS



271093–14

AC Inputs during testing are driven at $V_{CC}-0.5V$ for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



271093–15

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

EPROM CHARACTERISTICS

Table 2 shows the logic levels for programming the Program Memory, the Encryption Table, and the Lock Bits and for reading the signature bytes.

Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	⊓	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0–3FH		H	L	⊓	12.75V	L	H	H	L	H
Program Lock Bits	Bit 1	H	L	⊓	12.75V	H	H	H	H	H
	Bit 2	H	L	⊓	12.75V	H	H	H	L	L
	Bit 3	H	L	⊓	12.75V	H	L	H	H	L
Read Signature Byte		H	L	H	H	L	L	L	L	L

NOTES:
"1" = Valid high for that pin
"0" = Valid low for that pin
"VPP" = +12.75V ±0.25V

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4–P3.5 respectively for A0–A15.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.3, P3.6, P3.7.

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$.

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:
Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.

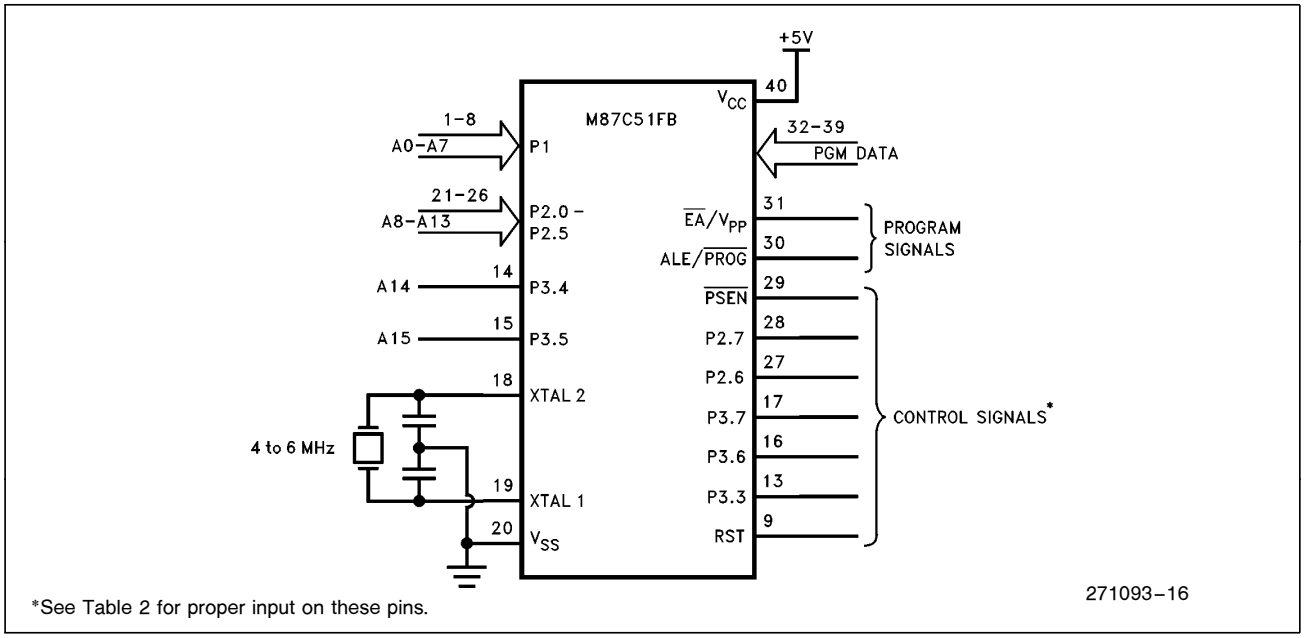


Figure 9. Programming the EPROM

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 9 and 10 for address, data, and control signals set up. To program the M87C51FB the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V $\pm$0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

PROGRAM VERIFY

Program verify may be done after each byte that is programmed, or after a block of bytes that is programmed. In either case a complete verify of the entire array that has been programmed will ensure a reliable programming of the M87C51FB.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled. Refer to the EPROM Program Lock section in this data sheet.

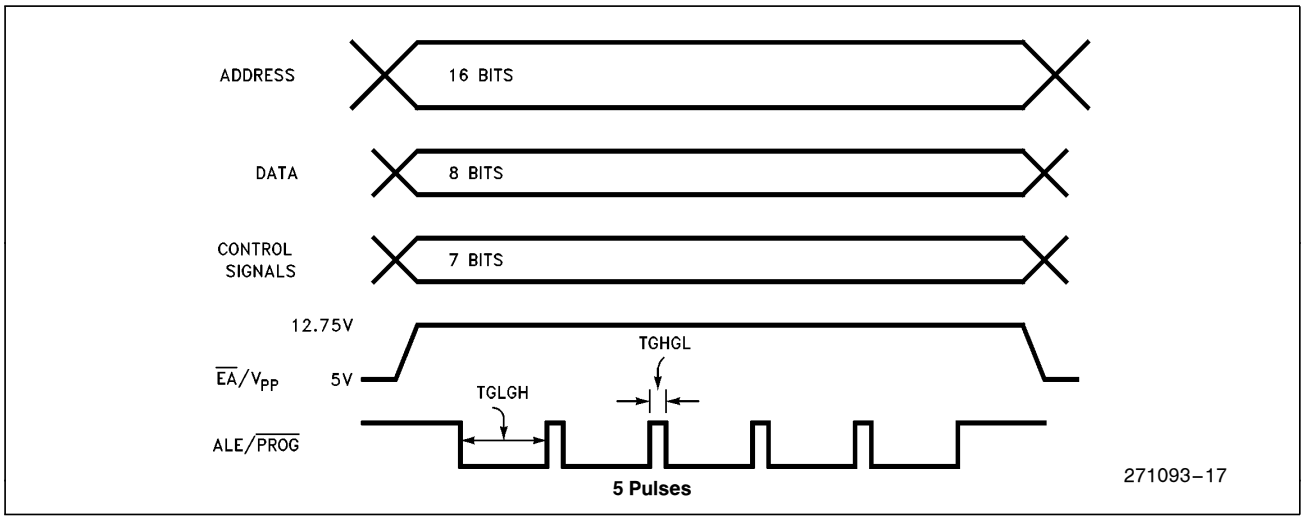


Figure 10. Programming Signal's Waveforms

EPROM Program Lock

The two-level Program Lock system consists of two Program Lock bits and a 32 byte Encryption Array which are used to protect the program memory against software piracy.

Encryption Array

Within the EPROM array are 32 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 5 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encrypted Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in it's original, unmodified form.

Program Lock Bits

Also included in the EPROM Program Lock scheme are two Program Lock Bits which are programmed as shown in Table 2.

Table 3 outlines the features of programming the Lock Bits.

Erasing the EPROM also erases the Encryption Array and the Program Lock Bits, returning the part to full functionality.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H and 60H. To read these bytes, follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location: 30H = 89H
31H = 58H
60H = FBH

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves all the EPROM Cells in a 1's state.

Table 3. Program Lock Bits and their Features

Program Lock Bits LB1	LB2	Logic Enabled
U	U	No Program Lock features enabled. (Code Verify will still be encrypted by the Encryption Array.)
P	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled.
P	P	Same as above, but Verify is also disabled
U	P	Reserved for Future Definition

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

(T_A = 21°C to 27°C; V_{CC} = 5V ± 0.25V; V_{SS} = 0V)

ADVANCED INFORMATION—CONTACT INTEL FOR DESIGN-IN INFORMATION

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		50	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 (ENABLE) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	ENABLE Low to Data Valid		48TCLCL	
TEHQZ	Data Float after ENABLE	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS