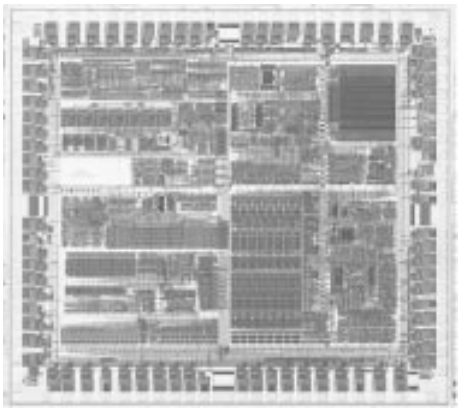
ADVANCE INFORMATION

M80C186XL20, 16, 12, 10
16-BIT HIGH-INTEGRATION EMBEDDED PROCESSOR

- **Low Power, Full Static Version of M80C186**
- **Operation Modes:**
  - **— Enhanced Mode**
    - **— DRAM Refresh Control Unit**
    - **— Power-Save Mode**
    - **— Direct Interface to 80C187**
  - **— Compatible Mode**
    - **— NMOS 80186 Pin-for-Pin Replacement for Non-Numerics Applications**
- **Integrated Feature Set**
  - **— Static, Modular CPU**
  - **— Clock Generator**
  - **— 2 Independent DMA Channels**
  - **— Programmable Interrupt Controller**
  - **— 3 Programmable 16-Bit Timers**
  - **— Dynamic RAM Refresh Control Unit**
  - **— Programmable Memory and Peripheral Chip Select Logic**
  - **— Programmable Wait State Generator**
  - **— Local Bus Controller**
  - **— Power-Save Mode**
  - **— System-Level Testing Support (High Impedance Test Mode)**
- **Completely Object Code Compatible with Existing 8086/8088 Software and Has 10 Additional Instructions over 8086/8088**
- **Speed Versions Available**
  - **— 20 MHz (M80C186XL20)**
  - **— 16 MHz (M80C186XL16)**
  - **— 12.5 MHz (M80C186XL12)**
  - **— 10 MHz (M80C186XL)**
- **Direct Addressing Capability to 1 MByte Memory and 64 Kbyte I/O**
- **Complete System Development Support**
  - **— All 8086 and 80C186 Software Development Tools Can Be Used for M80C186XL System Development**
    - **— ASM 86 Assembler, PL/M-86, Pascal-86, Fortran-86, iC-86 and System Utilities**
    - **— In-Circuit-Emulator (ICE™-186)**
- **Available in 68-Pin:**
  - **— Ceramic Pin Grid Array (PGA)**
- **Military Temperature Range:**
  - **— −55°C to +125°C (T_C)**

The Intel M80C186XL is a Modular Core re-implementation of the M80C186 microprocessor. It offers higher speed and lower power consumption than the standard M80C186 but maintains 100% clock-for-clock functional compatibility. Packaging and pinout are also identical.



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*Other brands and names are the property of their respective owners.

March 1995 Order Number: 271276-002

M80C186XL20, 16, 12, 10
16-BIT HIGH INTEGRATION EMBEDDED PROCESSOR

CONTENTS

PAGE

INTRODUCTION 10

M80C186XL BASE ARCHITECTURE 10

M80C186XL Clock Generator 10

Bus Interface Unit 11

M80C186XL PERIPHERAL ARCHITECTURE 11

Chip-Select/Ready Generation Logic 11

DMA Unit 12

Timer/Counter Unit 12

Interrupt Control Unit 12

Enhanced Mode Operation 12

Queue-Status Mode 12

DRAM Refresh Control Unit 13

Power-Save Control 13

Interface for 80C187 Math Coprocessor 13

ONCE Test Mode 13

ABSOLUTE MAXIMUM RATINGS 14

DC CHARACTERISTICS 14

CONTENTS

PAGE

AC CHARACTERISTICS 16

Major Cycle Timings (Read Cycle) 16

Major Cycle Timings (Write Cycle) 18

Major Cycle Timings (Interrupt Acknowledge Cycle) 20

Software Halt Cycle Timings 22

Clock Timings 23

Ready, Peripheral and Queue Status Timings 25

Reset and Hold/HLDA Timings 27

AC TIMING WAVEFORMS 33

EXPLANATION OF THE AC SYMBOLS 36

DERATING CURVES 37

M80C186XL EXECUTION TIMINGS 38

INSTRUCTION SET SUMMARY 39

FOOTNOTES 44

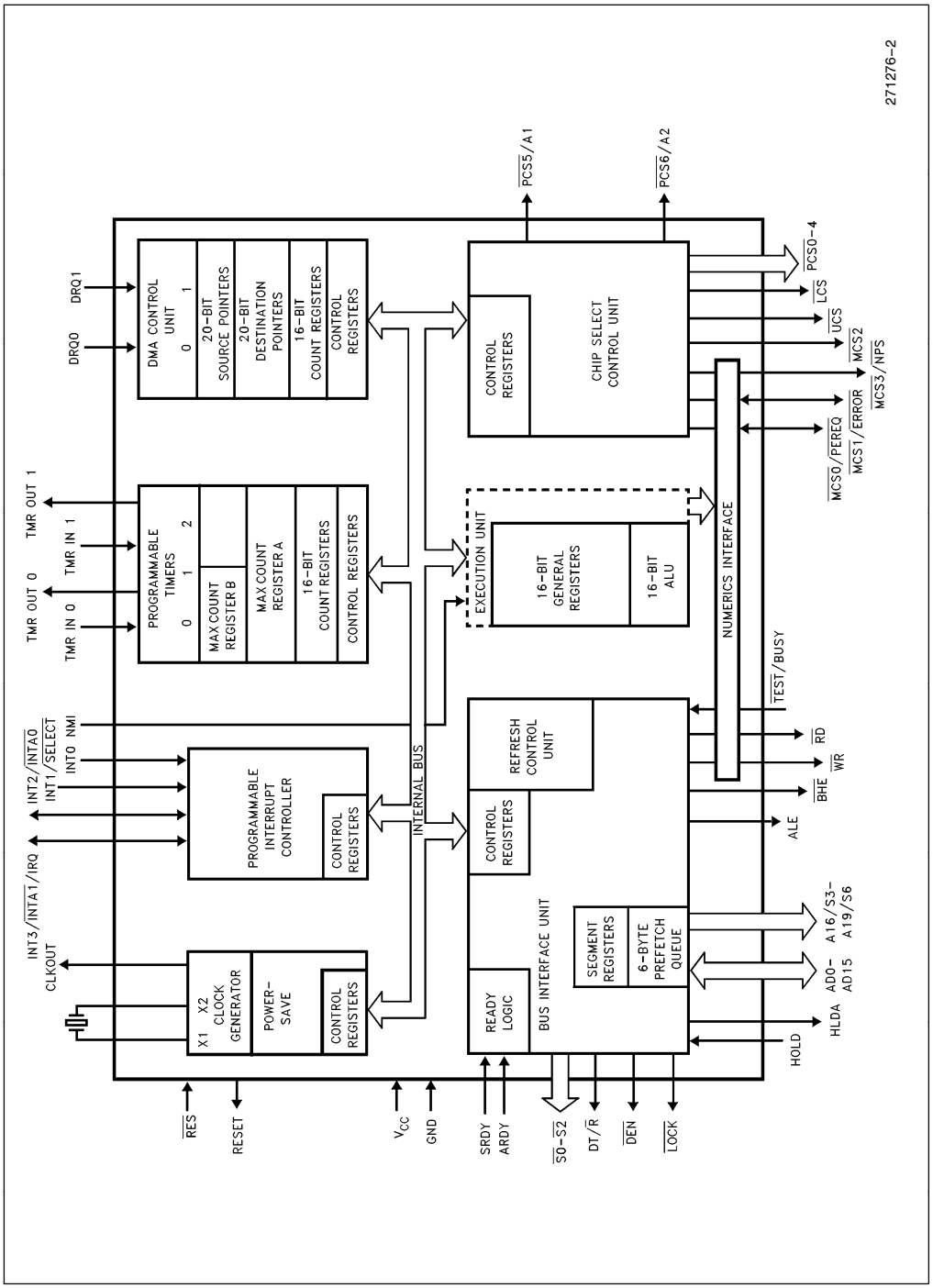
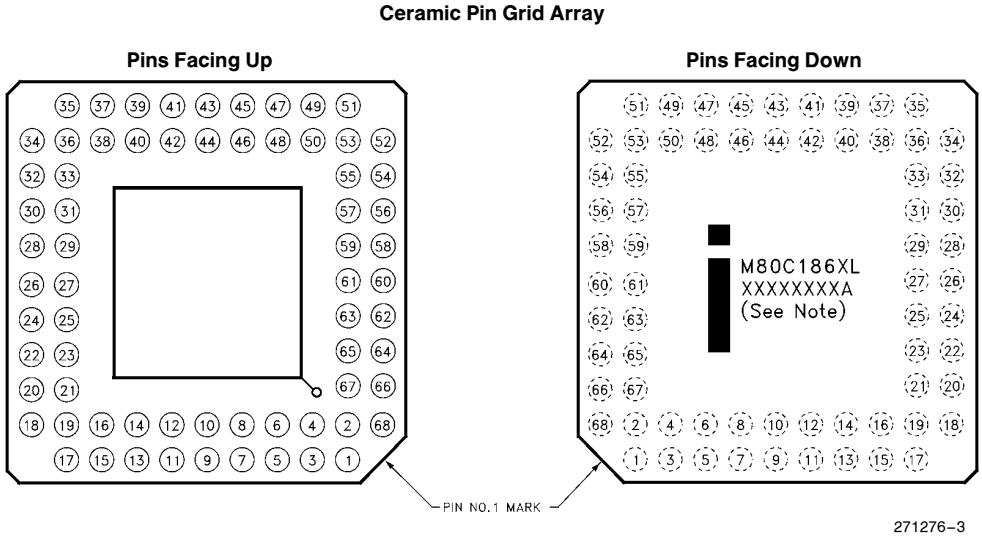


Figure 1. M80C186XL Block Diagram



NOTE:
XXXXXXXXA indicates the Intel FPO number.

Figure 2. M80C186XL Pinout Diagrams

Table 1. M80C186XL Pin Description

Symbol	PGA Pin No.	Type	Name and Function
V_{CC}	9 43	I I	System Power: +5 volt power supply.
V_{SS}	26 60	I I	System Ground.
RESET	57	O	RESET Output indicates that the M80C186XL CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal. Reset goes inactive 2 clockout periods after $\overline{RES}$ goes inactive. When tied to the $\overline{TEST}$/BUSY pin, RESET forces the M80C186XL into enhanced mode. RESET is not floated during bus hold.
X1 X2	59 58	I O	Crystal Inputs X1 and X2 provide external connections for a fundamental mode or third overtone parallel resonant crystal for the internal oscillator. X1 can connect to an external clock instead of a crystal. In this case, minimize the capacitance on X2. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT is active during reset and bus hold.
$\overline{RES}$	24	I	An active $\overline{RES}$ causes the M80C186XL to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the M80C186XL clock. The M80C186XL begins fetching instructions approximately 6½ clock cycles after $\overline{RES}$ is returned HIGH. For proper initialization, V_{CC} must be within specifications and the clock signal must be stable for more than 4 clocks with $\overline{RES}$ held LOW. $\overline{RES}$ is internally synchronized. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network.
$\overline{TEST}$/BUSY	47	I/O	The $\overline{TEST}$ pin is sampled during and after reset to determine whether the M80C186XL is to enter Compatible or Enhanced Mode. Enhanced Mode requires $\overline{TEST}$ to be HIGH on the rising edge of $\overline{RES}$ and LOW four CLKOUT cycles later. Any other combination will place the M80C186XL in Compatible Mode. During power-up, active $\overline{RES}$ is required to configure $\overline{TEST}$/BUSY as an input. A weak internal pullup ensures a HIGH state when the input is not externally driven. $\overline{TEST}$—In Compatible Mode this pin is configured to operate as $\overline{TEST}$. This pin is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when WAIT execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled every five clocks until it goes LOW, at which time execution will resume. If interrupts are enabled while the M80C186XL is waiting for $\overline{TEST}$, interrupts will be serviced. BUSY—In Enhanced Mode, this pin is configured to operate as BUSY. The BUSY input is used to notify the M80C186XL of Math Coprocessor activity. Floating point instructions executing in the M80C186XL sample the BUSY pin to determine when the Math Coprocessor is ready to accept a new command. BUSY is active HIGH.

Table 1. M80C186XL Pin Description (Continued)

Symbol	PGA Pin No.	Type	Name and Function
TMR IN 0 TMR IN 1	20 21	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized. Timer Inputs must be tied HIGH when not being used as clock or retrigger inputs.
TMR OUT 0 TMR OUT 1	22 23	O O	Timer outputs are used to provide single pulse or continous waveform generation, depending upon the timer mode selected. These outputs are not floated during a bus hold.
DRQ0 DRQ1	18 19	I I	DMA Request is asserted HIGH by an external device when it is ready for DMA Channel 0 or 1 to perform a transfer. These signals are level-triggered and internally synchronized.
NMI	46	I	The Non-Maskable Interrupt input causes a Type 2 interrupt. An NMI transition from LOW to HIGH is latched and synchronized internally, and initiates the interrupt at the next instruction boundary. NMI must be asserted for at least one CLKOUT period. The Non-Maskable Interrupt cannot be avoided by programming.
INT0 INT1/$\overline{\text{SELECT}}$ INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$/IRQ	45 44 42 41	I I I/O I/O	Maskable Interrupt Requests can be requested by activating one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When Slave Mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
A19/S6 A18/S5 A17/S4 A16/S3	65 66 67 68	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) indicate the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W and T_4, the S6 pin is LOW to indicate a CPU-initiated bus cycle or HIGH to indicate a DMA-initiated or refresh bus cycle. During the same T-states, S3, S4 and S5 are always LOW. These outputs are floated during bus hold or reset.
AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	1 3 5 7 10 12 14 16 2 4 6 8 11 13 15 17	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Address/Data Bus (0–15) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W and T_4) bus. The bus is active HIGH. A_0 is analogous to $\overline{\text{BHE}}$ for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations. These pins are floated during a bus hold or reset.

Table 1. M80C186XL Pin Description (Continued)

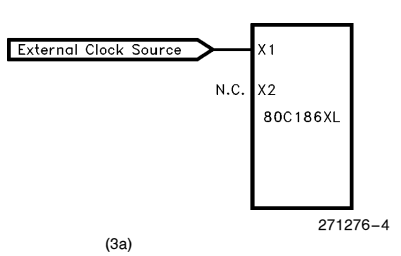
Symbol	PGA Pin No.	Type	Name and Function
$\overline{BHE}$	64	O	The $\overline{BHE}$ (Bus High Enable) signal is analogous to A0 in that it is used to enable data on to the most significant half of the data bus, pins D15–D8. $\overline{BHE}$ will be LOW during T_1 when the upper byte is transferred and will remain LOW through T_3 AND T_W. $\overline{BHE}$ does not need to be latched. $\overline{BHE}$ will float during HOLD or RESET. In Enhanced Mode, $\overline{BHE}$ will also be used to signify DRAM refresh cycles. A refresh cycle is indicated by both $\overline{BHE}$ and A0 being HIGH.
			$\overline{BHE}$ and A0 Encodings
			$\overline{BHE}$ Value / **A0 Value** / **Function** 0 / 0 / Word Transfer 0 / 1 / Byte Transfer on upper half of data bus (D15–D8) 1 / 0 / Byte Transfer on lower half of data bus (D_7–D_0) 1 / 1 / Refresh
ALE/QS0	61	O	Address Latch Enable/Queue Status 0 is provided by the M80C186XL to latch the address. ALE is active HIGH, with addresses guaranteed valid on the trailing edge.
$\overline{WR}$/QS1	63	O	Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. It is active LOW, and floats during bus hold or reset. When the M80C186XL is in Queue Status Mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.
			QS1 / **QS0** / **Queue Operation** 0 / 0 / No queue operation 0 / 1 / First opcode byte fetched from the queue 1 / 1 / Subsequent byte fetched from the queue 1 / 0 / Empty the queue
$\overline{RD}$/$\overline{QSMD}$	62	O/I	Read Strobe is an active LOW signal which indicates that the M80C186XL is performing a memory or I/O read cycle. It is guaranteed not to go LOW before the A/D bus is floated. An internal pull-up ensures that $\overline{RD}$/$\overline{QSMD}$ is HIGH during RESET. Following RESET the pin is sampled to determine whether the M80C186XL is to provide ALE, $\overline{RD}$, and $\overline{WR}$, or queue status information. To enable Queue Status Mode, $\overline{RD}$ must be connected to GND. $\overline{RD}$ will float during bus HOLD.
ARDY	55	I	Asynchronous Ready informs the M80C186XL that the addressed memory space or I/O device will complete a data transfer. The ARDY pin accepts a rising edge that is asynchronous to CLKOUT and is active HIGH. The falling edge of ARDY must be synchronized to the M80C186XL clock. Connecting ARDY HIGH will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the SRDY pin.
SRDY	49	I	Synchronous Ready informs the M80C186XL that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active-HIGH input synchronized to CLKOUT. The use of SRDY allows a relaxed system timing over ARDY. This is accomplished by elimination of the one-half clock cycle required to internally synchonize the ARDY input signal. Connecting SRDY high will always assert the ready condition to the CPU. If this line is unused, it should be tied LOW to yield control to the ARDY pin.

Table 1. M80C186XL Pin Description (Continued)

Symbol	PGA Pin No.	Type	Name and Function
$\overline{LOCK}$	48	O	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus. $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction immediately following the LOCK prefix. It remains active until the completion of that instruction. No instruction prefetching will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ floats during bus hold or reset.
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$	52 53 54	O O O	Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information: **M80C186XL Bus Cycle Status Information** $\overline{S2}$ $\overline{S1}$ $\overline{S0}$ — Bus Cycle Initiated 0 0 0 — Interrupt Acknowledge 0 0 1 — Read I/O 0 1 0 — Write I/O 0 1 1 — Halt 1 0 0 — Instruction Fetch 1 0 1 — Read Data from Memory 1 1 0 — Write Data to Memory 1 1 1 — Passive (no bus cycle) The status pins float during HOLD. $\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.
HOLD HLDA	50 51	I O	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. The M80C186XL generates HLDA (HIGH) in response to a HOLD request. Simultaneous with the issuance of HLDA, the M80C186XL will float the local bus and control lines. After HOLD is detected as being LOW, the M80C186XL will lower HLDA. When the M80C186XL needs to run another bus cycle, it will again drive the local bus and control lines. In Enhanced Mode, HLDA will go low when a DRAM refresh cycle is pending in the M80C186XL and an external bus master has control of the bus. It will be up to the external master to relinquish the bus by lowering HOLD so that the M80C186XL may execute the refresh cycle.
$\overline{UCS}$	34	O/I	Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. $\overline{UCS}$ does not float during bus hold. The address range activating $\overline{UCS}$ is software programmable. $\overline{UCS}$ and $\overline{LCS}$ are sampled upon the rising edge of $\overline{RES}$. If both pins are held low, the M80C186XL will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. $\overline{UCS}$ has a weak internal pullup that is active during RESET to ensure that the M80C186XL does not enter ONCE Mode inadvertently.
$\overline{LCS}$	33	O/I	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. $\overline{LCS}$ does not float during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.

Table 1. M80C186XL Pin Description (Continued)

Symbol	PGA Pin No.	Type	Name and Function
LCS (Continued)			UCS and LCS are sampled upon the rising edge of RES. If both pins are held low, the M80C186XL will enter ONCE Mode. In ONCE Mode all pins assume a high impedance state and remain so until a subsequent RESET. LCS has a weak internal pullup that is active only during RESET to ensure that the M80C186XL does not enter ONCE mode inadvertently.
MCS0/PEREQ MCS1/ERROR MCS2 MCS3/NPS	38 37 36 35	O/I O/I O O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines do not float during bus HOLD. The address ranges activating MCS0–3 are software programmable. In Enhanced Mode, MCS0 becomes a PEREQ input (Processor Extension Request). When connected to the Math Coprocessor, this input is used to signal the M80C186XL when to make numeric data transfers to and from the coprocessor. MCS3 becomes NPS (Numeric Processor Select) which may only be activated by communication to the 80C187. MCS1 becomes ERROR in Enhanced Mode and is used to signal numerics coprocessor errors. MCS0/PEREQ and MCS1/ERROR have weak internal pullups which are active during reset.
PCS0 PCS1 PCS2 PCS3 PCS4	25 27 28 29 30	O O O O O	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O or 1 MByte memory space). These lines do not float during bus HOLD. The address ranges activating PCS0–4 are software programmable.
PCS5/A1	31	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating PCS5 is software-programmable. PCS5/A1 does not float during bus HOLD. When programmed to provide latched A1, this pin will retain the previously latched value during HOLD.
PCS6/A2	32	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating PCS6 is software-programmable. PCS6/A2 does not float during bus HOLD. When programmed to provide latched A2, this pin will retain the previously latched value during HOLD.
DT/R	40	O	Data Transmit/Receive controls the direction of data flow through an external data bus transceiver. When LOW, data is transferred to the M80C186XL. When HIGH the M80C186XL places write data on the data bus. DT/R floats during a bus hold or reset.
DEN	39	O	Data Enable is provided as a data bus transceiver output enable. DEN is active LOW during each memory and I/O access (including 80C187 access). DEN is HIGH whenever DT/R changes state. During RESET, DEN is driven HIGH for one clock, then floated. DEN also floats during HOLD.
N.C.	—	—	Not connected. To maintain compatibility with future products, do not connect to these pins.



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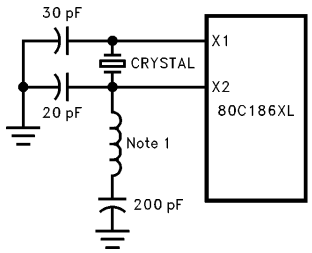


(3b)

Note 1:

XTAL Frequency	L1 Value
20 MHz	12.0 μH ±20%
25 MHz	8.2 μH ±20%
32 MHz	4.7 μH ±20%
40 MHz	3.0 μH ±20%

LC network is only required when using a third overtone crystal.

Figure 3. M80C186XL Oscillator Configurations (see text)

INTRODUCTION

The following Functional Description describes the base architecture of the M80C186XL. The M80C186XL is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip. The M80C186XL is object code compatible with the 8086/8088 microprocessors and adds 10 new instruction types to the 8086/8088 instruction set.

The M80C186XL has two major modes of operation, Compatible and Enhanced. In Compatible Mode the M80C186XL is completely compatible with NMOS 80186, with the exception of 8087 support. The Enhanced mode adds three new features to the system design. These are Power-Save control, Dynamic RAM refresh, and an asynchronous Numerics Coprocessor interface.

M80C186XL BASE ARCHITECTURE

M80C186XL Clock Generator

The M80C186XL provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

The M80C186XL oscillator circuit is designed to be used either with a parallel resonant fundamental or third-overtone mode crystal, depending upon the frequency range of the application. This is used as the time base for the M80C186XL.

The output of the oscillator is not directly available outside the M80C186XL. The recommended crystal configuration is shown in Figure 3b. When used in third-overtone mode, the tank circuit is recommended for stable operation. Alternately, the oscillator may be driven from an external source as shown in Figure 3a.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide by two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All AC Timings are referenced to CLKOUT.

Intel recommends the following values for crystal selection parameters.

Temperature Range:	Application Specific
ESR (Equivalent Series Resistance):	60Ω max
C_0 (Shunt Capacitance of Crystal):	7.0 pF max
C_1 (Load Capacitance):	20 pF ±5 pF
Drive Level:	2 mW max

Bus Interface Unit

The M80C186XL provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data from the local bus during a read operation. Synchronous and asynchronous ready input pins are provided to extend a bus cycle beyond the minimum four states (clocks).

The M80C186XL bus controller also generates two control signals ($\overline{DEN}$ and DT/$\overline{R}$) when interfacing to external transceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

During RESET the local bus controller will perform the following action:

- Drive $\overline{DEN}$, $\overline{RD}$ and $\overline{WR}$ HIGH for one clock cycle, then float them.
- Drive $\overline{S0}$–$\overline{S2}$ to the inactive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Float AD0–15, A16–19, $\overline{BHE}$, DT/$\overline{R}$.
- Drive ALE LOW
- Drive HLDA LOW.

$\overline{RD}$/$\overline{QSMD}$, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$ and $\overline{TEST}$/BUSY pins have internal pullup devices which are active while $\overline{RES}$ is applied. Excessive loading or grounding certain of these pins causes the M80C186XL to enter an alternative mode of operation:

- $\overline{RD}$/$\overline{QSMD}$ low results in Queue Status Mode.
- $\overline{UCS}$ and $\overline{LCS}$ low results in ONCE Mode.
- $\overline{TEST}$/BUSY low (and high later) results in Enhanced Mode.

M80C186XL PERIPHERAL ARCHITECTURE

All the M80C186XL integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The control block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles. An offset map of the 256-byte control register block is shown in Figure 4.

Chip-Select/Ready Generation Logic

The M80C186XL contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

The M80C186XL provides 6 memory chip select outputs for 3 address areas; upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

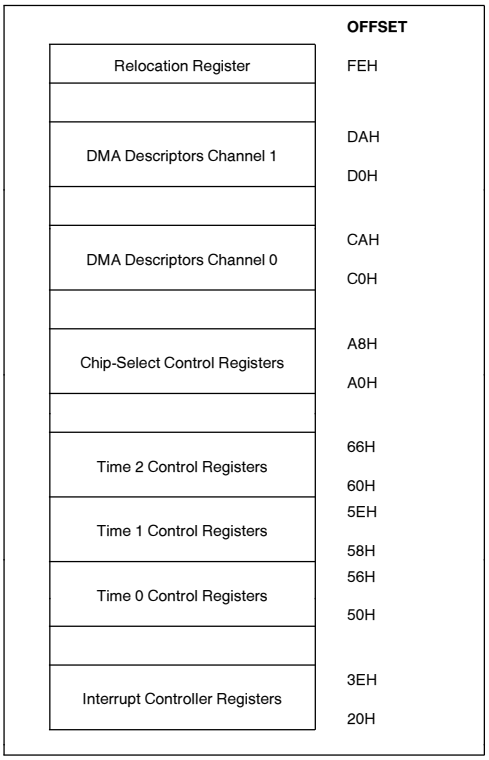


Figure 4. Internal Register Map

The M80C186XL provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the M80C186XL begins executing at memory location FFFF0H.

The M80C186XL provides a chip select for low memory called LCS. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The M80C186XL provides four MCS lines which are active within a user-locatable memory block. This block can be located within the M80C186XL 1 Mbyte memory address space exclusive of the areas defined by UCS and LCS. Both the base address and size of this memory block are programmable.

The M80C186XL can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. The base address may be located in either memory or I/O space.

The M80C186XL can generate a READY signal internally for each of the memory or peripheral CS lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the M80C186XL may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

Upon RESET, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the UCS line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to insert 3 wait states in conjunction with external READY (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers.

DMA Unit

The M80C186XL DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data.

Timer/Counter Unit

The M80C186XL provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

Interrupt Control Unit

The M80C186XL can receive interrupts from a number of sources, both internal and external. The M80C186XL has 5 external and 2 internal interrupt sources (Timer/Couners and DMA). The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU.

Enhanced Mode Operation

In Compatible Mode the M80C186XL operates with all the features of the NMOS 80186, with the exception of 8087 support (i.e. no math coprocessing is possible in Compatible Mode). Queue-Status information is still available for design purposes other than 8087 support.

All the Enhanced Mode features are completely masked when in Compatible Mode. A write to any of the Enhanced Mode registers will have no effect, while a read will not return any valid data.

In Enhanced Mode, the M80C186XL will operate with Power-Save, DRAM refresh, and numerics coprocessor support in addition to all the Compatible Mode features.

If connected to a math coprocessor, this mode will be invoked automatically. Without an NPX, this mode can be entered by tying the RESET output signal from the M80C186XL to the TEST/BUSY input.

Queue-Status Mode

The queue-status mode is entered by strapping the RD pin low. RD is sampled at RESET and if LOW, the M80C186XL will reconfigure the ALE and WR pins to be QS0 and QS1 respectively. This mode is available on the M80C186XL in both Compatible and Enhanced Modes.

DRAM Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates DRAM refresh bus cycles. The RCU operates only in Enhanced Mode. After a programmable period of time, the RCU generates a memory read request to the BIU. If the address generated during a refresh bus cycle is within the range of a properly programmed chip select, that chip select will be activated when the BIU executes the refresh bus cycle.

Power-Save Control

The M80C186XL, when in Enhanced Mode, can enter a power saving state by internally dividing the processor clock frequency by a programmable factor. This divided frequency is also available at the CLKOUT pin.

All internal logic, including the Refresh Control Unit and the timers, have their clocks slowed down by the division factor. To maintain a real time count or a fixed DRAM refresh rate, these peripherals must be re-programmed when entering and leaving the power-save mode.

Interface for 80C187 Math Coprocessor

In Enhanced Mode, three of the mid-range memory chip selects are redefined according to Table 2 for use with the 80C187. The fourth chip select, $\overline{MCS2}$ functions as in compatible mode, and may be programmed for activity with ready logic and wait states accordingly. As in Compatible Mode, $\overline{MCS2}$ will function for one-fourth a programmed block size.

Table 2. $\overline{MCS}$ Assignments

Compatible Mode	Enhanced Mode	
$\overline{MCS0}$	PEREQ	Processor Extension Request
$\overline{MCS1}$	$\overline{ERROR}$	NPX Error
$\overline{MCS2}$	$\overline{MCS2}$	Mid-Range Chip Select
$\overline{MCS3}$	$\overline{NPS}$	Numeric Processor Select

ONCE Test Mode

To facilitate testing and inspection of devices when fixed into a target system, the M80C186XL has a test mode available which allows all pins to be placed in a high-impedance state. ONCE stands for ''ON Circuit Emulation''. When placed in this mode, the M80C186XL will put all pins in the high-impedance state until RESET.

The ONCE mode is selected by tying the $\overline{UCS}$ and the $\overline{LCS}$ LOW during RESET. These pins are sampled on the low-to-high transition of the $\overline{RES}$ pin. The $\overline{UCS}$ and the $\overline{LCS}$ pins have weak internal pull-up resistors similar to the $\overline{RD}$ and $\overline{TEST}$/BUSY pins to guarantee ONCE Mode is not entered inadvertently during normal operation. $\overline{LCS}$ and $\overline{UCS}$ must be held low at least one clock after $\overline{RES}$ goes high to guarantee entrance into ONCE Mode.

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias . . . −55°C to +125°C

Storage Temperature . . . . . −65°C to +150°C

Voltage on Any Pin with
Respect to Ground . . . . . −1.0V to +7.0V

/Package Power Dissipation 1W
Not to exceed the maximum allowable die temperature based on thermal resistance of the package.

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTICE: The specifications are subject to change without notice.

DC CHARACTERISTICS $T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (Except X1)	−0.5	0.2 V_{CC} − 0.3	V	
V_{IL1}	Clock Input Low Voltage (X1)	−0.5	0.6	V	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	V	
V_{IH2}	Clock Input High Voltage (X1)	3.9	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.5 mA (S0, 1, 2) I_{OL} = 2.0 mA (others)
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −2.4 mA @ 2.4V (4)
		V_{CC} − 0.5	V_{CC}	V	I_{OH} = −200 μA @ V_{CC} −0.5(4)
I_{CC}	Power Supply Current		100	mA	@ 20 MHz, −55°C V_{CC} = 5.5V(3)
			90	mA	@16 MHz, −55°C V_{CC} = 5.5V(3)
			80	mA	@ 12.5 MHz, −55°C V_{CC} = 5.5V (3)
			70	mA	@ 10 MHz, −55°C V_{CC} = 5.5V (3)
I_{LI}	Input Leakage Current		±10	μA	@ 0.5 MHz, 0.45V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current		±10	μA	@ 0.5 MHz, 0.45V ≤ V_{OUT} ≤ V_{CC}(1)
V_{CLO}	Clock Output Low		0.45	V	I_{CLO} = 4.0 mA

DC CHARACTERISTICS (Continued) $T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{CHO}	Clock Output High	$V_{CC} - 0.5$		V	$I_{CHO} = -500\ \mu A$
C_{IN}	Input Capacitance		10	pF	@ 1 MHz(2)
C_{IO}	Output or I/O Capacitance		20	pF	@ 1 MHz(2)

NOTES:
1. Pins being floated during HOLD or by invoking the ONCE Mode.
2. Characterization conditions are a) Frequency = 1 MHz; b) Unmeasured pins at GND; c) V_{IN} at + 5.0V or 0.45V. This parameter is not tested.
3. Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open.
4. $\overline{RD}$/QSMD, $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS0}$/PEREQ, $\overline{MCS1}$/$\overline{ERROR}$ and $\overline{TEST}$/BUSY pins have internal pullup devices. Loading some of these pins above $I_{OH} = -200\ \mu A$ can cause the M80C186XL to go into alternative modes of operation. See the section on Local Bus Controller and Reset for details.

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (READ CYCLE)

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL		M80C186XL12			
		Min	Max	Min	Max		
M80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 18$		$T_{CLCH} - 15$		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	$T_{CHCL} - 15$		$T_{CHCL} - 15$		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	$T_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	35	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay	3	44	3	37	ns	
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	
M80C186XL TIMING RESPONSES (Read Cycle)							
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	3	44	3	37	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL} - 30$		$2T_{CLCL} - 25$		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	3	44	3	37	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	$T_{CLCH} - 14$		$T_{CLCH} - 14$		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	Equal Loading

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (READ CYCLE)

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL16		M80C186XL20			
		Min	Max	Min	Max		
M80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		10		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	1	31	1	25	ns	
T_{CLSH}	Status Inactive Delay	1	30	1	25	ns	
T_{CLAV}	Address Valid Delay	1	33	1	27	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	1	33	1	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 15$		$T_{CLCH} - 10$		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	$T_{CHCL} - 15$		$T_{CHCL} - 10$		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CLCSV}	Chip-Select Active Delay	1	30	1	25	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	$t_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	1	25	1	20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	1	31	1	22	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay	1	31	1	22	ns	
T_{CHCTV}	Control Active Delay 2	1	31	1	22	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	1	35	1	22	ns	
M80C186XL TIMING RESPONSES (Read Cycle)							
T_{AZRL}	Address Float to $\overline{RD}$ Active	0		0		ns	
T_{CLRL}	$\overline{RD}$ Active Delay	1	31	1	27	ns	
T_{RLRH}	$\overline{RD}$ Pulse Width	$2T_{CLCL} - 25$		$2T_{CLCL} - 20$		ns	
T_{CLRH}	$\overline{RD}$ Inactive Delay	1	31	1	27	ns	
T_{RHLH}	$\overline{RD}$ Inactive to ALE High	$T_{CLCH} - 14$		$T_{CLCH} - 14$		ns	Equal Loading
T_{RHAV}	$\overline{RD}$ Inactive to Address Active	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	Equal Loading

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (WRITE CYCLE)

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL		M80C186XL12			
		Min	Max	Min	Max		
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 18$		$T_{CLCH} - 15$		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	$T_{CHCL} - 15$		$T_{CHCL} - 15$		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLDOX}	Data Hold Time	3		3		ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	ns	
T_{CLCSV}	Chip-Select Active Delay	3	42	3	33	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	$T_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	35	3	30	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	
M80C186XL TIMING RESPONSES (Write Cycle)							
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL} - 30$		$2T_{CLCL} - 25$		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	$T_{CLCH} - 14$		$T_{CLCH} - 14$		ns	Equal Loading
T_{WHDX}	Data Hold after $\overline{WR}$	$T_{CLCL} - 34$		$T_{CLCL} - 20$		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	$T_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (WRITE CYCLE)

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL16		M80C186XL20			
		Min	Max	Min	Max		
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	1	31	1	25	ns	
T_{CLSH}	Status Inactive Delay	1	30	1	25	ns	
T_{CLAV}	Address Valid Delay	1	33	1	27	ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	1	33	1	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 15$		$T_{CLCH} - 10$		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	$T_{CHCL} - 15$		$T_{CHCL} - 10$		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLDOX}	Data Hold Time	1		1		ns	
T_{CVCTV}	Control Active Delay 1	1	31	1	25	ns	
T_{CVCTX}	Control Inactive Delay	1	31	1	25	ns	
T_{CLCSV}	Chip-Select Active Delay	1	30	1	25	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	$T_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	1	25	1	20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	1	35	1	22	ns	
M80C186XL TIMING RESPONSES (Write Cycle)							
T_{WLWH}	$\overline{WR}$ Pulse Width	$2T_{CLCL} - 25$		$2T_{CLCL} - 20$		ns	
T_{WHLH}	$\overline{WR}$ Inactive to ALE High	$T_{CLCH} - 14$		$T_{CLCH} - 14$		ns	Equal Loading
T_{WHDX}	Data Hold after $\overline{WR}$	$T_{CLCL} - 20$		$T_{CLCL} - 15$		ns	Equal Loading
T_{WHDEX}	$\overline{WR}$ Inactive to $\overline{DEN}$ Inactive	$T_{CLCH} - 10$		$T_{CLCH} - 10$		ns	Equal Loading

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL		M80C186XL12			
		Min	Max	Min	Max		
M80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		15		ns	
T_{CLDX}	Data in Hold (A/D)	3		3		ns	
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	3	40	3	36	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 18$		$T_{CLCH} - 15$		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	$T_{CHCL} - 15$		$T_{CHCL} - 15$		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CVCTV}	Control Active Delay 1	3	44	3	37	ns	
T_{CVCTX}	Control Inactive Delay	3	44	3	37	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	3	44	3	37	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	3	40	3	37	ns	

AC CHARACTERISTICS

MAJOR CYCLE TIMINGS (INTERRUPT ACKNOWLEDGE CYCLE)

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL16		M80C186XL20			
		Min	Max	Min	Max		
M80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{DVCL}	Data in Setup (A/D)	15		10		ns	
T_{CLDX}	Data in Hold (A/D)	1		1		ns	
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	1	31	1	25	ns	
T_{CLSH}	Status Inactive Delay	1	30	1	25	ns	
T_{CLAV}	Address Valid Delay	1	33	1	27	ns	
T_{AVCH}	Address Valid to Clock High	0		0		ns	
T_{CLAX}	Address Hold	0		0		ns	
T_{CLDV}	Data Valid Delay	1	33	1	27	ns	
T_{CHDX}	Status Hold Time	10		10		ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{AVLL}	Address Valid to ALE Low	$T_{CLCH} - 15$		$T_{CLCH} - 10$		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	$T_{CHCL} - 15$		$T_{CHCL} - 10$		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CVCTV}	Control Active Delay 1	1	31	1	25	ns	
T_{CVCTX}	Control Inactive Delay	1	31	1	25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low	0		0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	1	31	1	22	ns	
T_{CVDEX}	$\overline{DEN}$ Inactive Delay (Non-Write Cycles)	1	31	1	22	ns	
T_{CLLV}	$\overline{LOCK}$ Valid/Invalid Delay	1	35	1	22	ns	

AC CHARACTERISTICS

SOFTWARE HALT CYCLE TIMINGS

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL		M80C186XL12			
		Min	Max	Min	Max		
M80C186XL GENERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	45	3	35	ns	
T_{CLSH}	Status Inactive Delay	3	46	3	35	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
T_{CHLH}	ALE Active Delay		30		25	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		30		25	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	44	3	37	ns	

Symbol	ParameterTarget	Values				Unit	Test Conditions
		M80C186XL16		M80C186XL20			
		Min	Max	Min	Max		
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CHSV}	Status Active Delay	3	31	3	25	ns	
T_{CLSH}	Status Inactive Delay	3	30	3	25	ns	
T_{CLAV}	Address Valid Delay	3	33	3	27	ns	
T_{CHLH}	ALE Active Delay		20		20	ns	
T_{LHLL}	ALE Width	$T_{CLCL} - 15$		$T_{CLCL} - 15$		ns	
T_{CHLL}	ALE Inactive Delay		20		20	ns	
T_{DXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low		0		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	31	3	22	ns	

AC CHARACTERISTICS

CLOCK TIMINGS

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL		M80C186XL12			
		Min	Max	Min	Max		
M80C186XL CLKIN REQUIREMENTS(1)							
T_{CKIN}	CLKIN Period	50	∞	40	∞	ns	
T_{CLCK}	CLKIN Low Time	20	∞	16	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	20	∞	16	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5	ns	1.0 to 3.5V
M80C186XL CLKOUT TIMING							
T_{CICO}	CLKIN to CLKOUT Skew		25		21	ns	
T_{CLCL}	CLKOUT Period	100	∞	80	∞	ns	
T_{CLCH}	CLKOUT Low Time	$0.5\ T_{CLCL} - 6$		$0.5\ T_{CLCL} - 5$		ns	$C_L = 100$ pF(3)
T_{CHCL}	CLKOUT High Time	$0.5\ T_{CLCL} - 6$		$0.5\ T_{CLCL} - 5$		ns	$C_L = 100$ pF(4)
T_{CH1CH2}	CLKOUT Rise Time		10		10	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		10		10	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: $V_{CC} = 5.5V$ $T_C = +125°C$.
4. Tested under worst case conditions: $V_{CC} = 4.5V$ $T_C = -55°C$.

AC CHARACTERISTICS

CLOCK TIMINGS

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL16		M80C186XL20			
		Min	Max	Min	Max		
M80C186XL CLKIN REQUIREMENTS(1)							
T_{CKIN}	CLKIN Period	31.25	∞	25	∞	ns	
T_{CLCK}	CLKIN Low Time	13	∞	10	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	13	∞	10	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5		5	ns	1.0 to 3.5V
M80C186XL CLKOUT TIMING							
T_{CICO}	CLKIN to CLKOUT Skew		17		17	ns	
T_{CLCL}	CLKOUT Period	62.5		50		ns	
T_{CLCH}	CLKOUT Low Time	$0.5\ T_{CLCL} - 5$		$0.5\ T_{CLCL} - 5$		ns	$C_L = 100$ pF(3)
T_{CHCL}	CLKOUT High Time	$0.5\ T_{CLCL} - 5$		$0.5\ T_{CLCL} - 5$		ns	$C_L = 100$ pF(4)
T_{CH1CH2}	CLKOUT Rise Time		10		8	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		10		8	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: $V_{CC} = 5.5V$. $T_C = +125°C$.
4. Tested under worst case conditions: $V_{CC} = 4.5V$. $T_C = -55°C$.

AC CHARACTERISTICS

READY, PERIPHERAL AND QUEUE STATUS TIMINGS

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL		M80C186XL12			
		Min	Max	Min	Max		
M80C186XL READY AND PERIPHERAL TIMING REQUIREMENTS (Listed More Than Once)							
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		15		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	15		15		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		15		ns	
T_{CLARX}	ARDY Active Hold Time(1)	15		15		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	15		15		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		25		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	15		15		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	15		15		ns	
M80C186XL PERIPHERAL AND QUEUE STATUS TIMING RESPONSES							
T_{CLTMV}	Timer Output Delay		40		33	ns	
T_{CHQSV}	Queue Status Delay		37		32	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

AC CHARACTERISTICS

READY, PERIPHERAL, AND QUEUE STATUS TIMINGS

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL16		M80C186XL20			
		Min	Max	Min	Max		
M80C186XL READY AND PERIPHERAL TIMING REQUIREMENTS							
T_{SRYCL}	Synchronous Ready (SRDY) Transition Setup Time(1)	15		10		ns	
T_{CLSRY}	SRDY Transition Hold Time(1)	15		10		ns	
T_{ARYCH}	ARDY Resolution Transition Setup Time(2)	15		10		ns	
T_{CLARX}	ARDY Active Hold Time(1)	15		10		ns	
T_{ARYCHL}	ARDY Inactive Holding Time	15		10		ns	
T_{ARYLCL}	Asynchronous Ready (ARDY) Setup Time(1)	25		15		ns	
T_{INVCH}	INTx, NMI, $\overline{TEST}$/BUSY, TMR IN Setup Time(2)	15		10		ns	
T_{INVCL}	DRQ0, DRQ1 Setup Time(2)	15		10		ns	
M80C186XL PERIPHERAL AND QUEUE STATUS TIMING RESPONSES							
T_{CLTMV}	Timer Output Delay		27		22	ns	
T_{CHQSV}	Queue Status Delay		30		27	ns	

NOTES:
1. To guarantee proper operation.
2. To guarantee recognition at clock edge.

AC CHARACTERISTICS

RESET AND HOLD/HLDA TIMINGS

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL		M80C186XL12			
		Min	Max	Min	Max		
M80C186XL RESET AND HOLD/HLDA TIMING REQUIREMENTS							
T_{RESIN}	$\overline{RES}$ Setup	15		15		ns	
T_{HVCL}	HOLD Setup(1)	15		15		ns	
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CLAZ}	Address Float Delay	T_{CLAX}	30	T_{CLAX}	25	ns	
T_{CLAV}	Address Valid Delay	3	44	3	36	ns	
M80C186XL RESET AND HOLD/HLDA TIMING RESPONSES							
T_{CLRO}	Reset Delay		40		33	ns	
T_{CLHAV}	HLDA Valid Delay	3	40	3	33	ns	
T_{CHCZ}	Command Lines Float Delay		40		33	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		44		36	ns	

NOTE:
1. To guarantee recognition at next clock.

AC CHARACTERISTICS

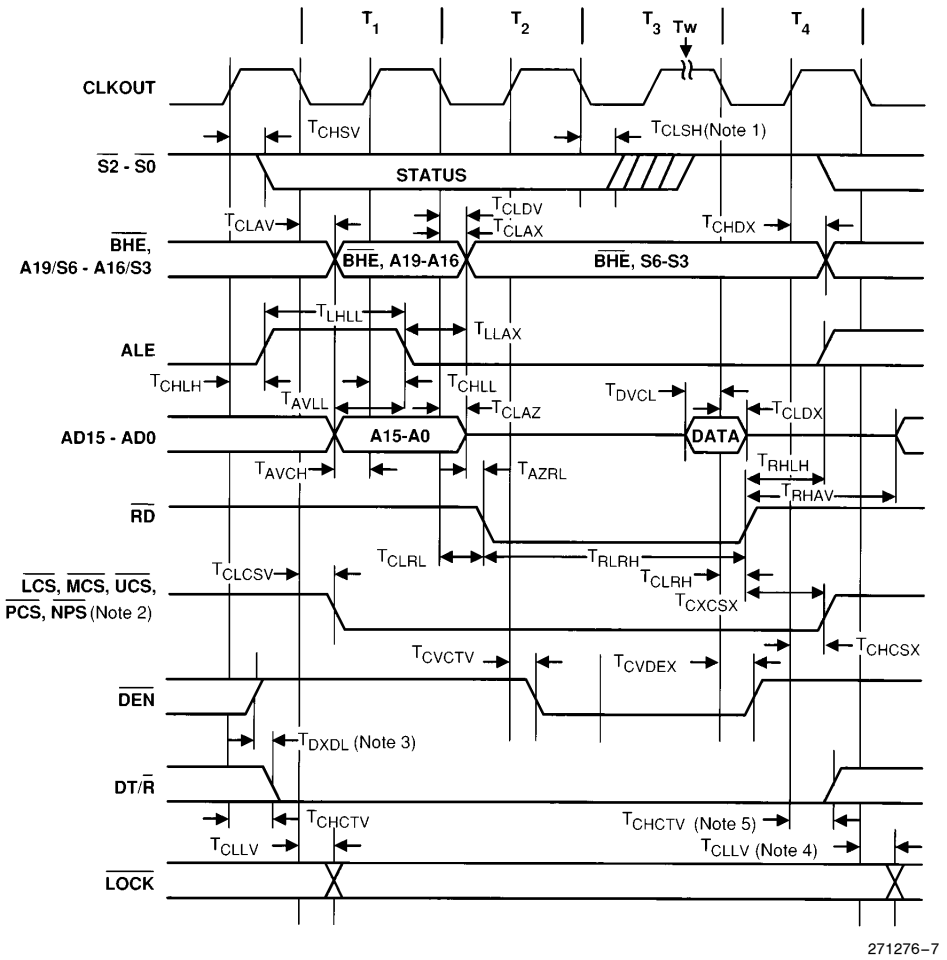
RESET AND HOLD/HLDA TIMINGS

$T_C = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$
All timings are measured at 1.5V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with $C_L = 50$ pF.
For AC tests, input $V_{IL} = 0.45V$ and $V_{IH} = 2.4V$ except at X1 where $V_{IH} = V_{CC} - 0.5V$.

Symbol	Parameter	Values				Unit	Test Conditions
		M80C186XL16		M80C186XL20			
		Min	Max	Min	Max		
M80C186XL RESET AND HOLD/HLDA TIMING REQUIREMENTS							
T_{RESIN}	$\overline{RES}$ Setup	15		15		ns	
T_{HVCL}	HOLD Setup(1)	15		10		ns	
M80C186XL GENERAL TIMING RESPONSES (Listed More Than Once)							
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	T_{CLAX}	20	ns	
T_{CLAV}	Address Valid Delay	1	33	1	22	ns	
M80C186XL RESET AND HOLD/HLDA TIMING RESPONSES							
T_{CLRO}	Reset Delay		27		22	ns	
T_{CLHAV}	HLDA Valid Delay	1	25	1	22	ns	
T_{CHCZ}	Command Lines Float Delay		28		25	ns	
T_{CHCV}	Command Lines Valid Delay (after Float)		32		26	ns	

NOTE:
1. To guarantee recognition at next clock.

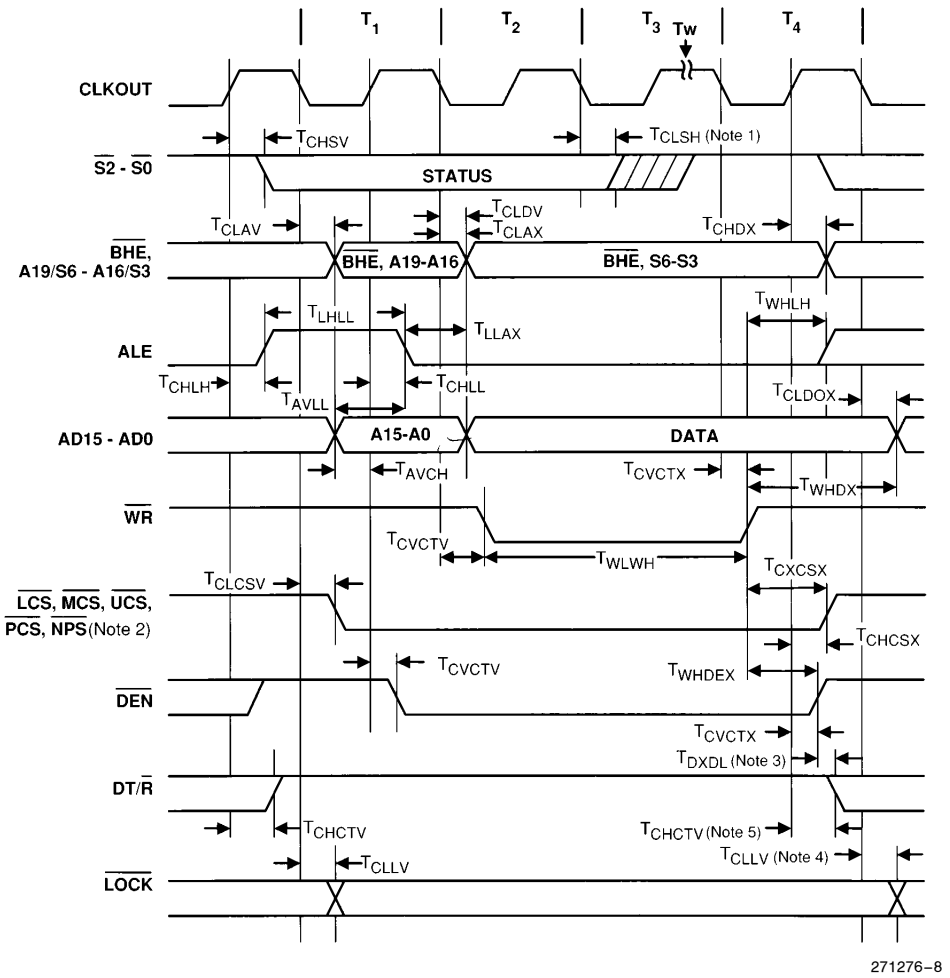
AC CHARACTERISTICS



NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by write.

Figure 5. Read Cycle Waveforms

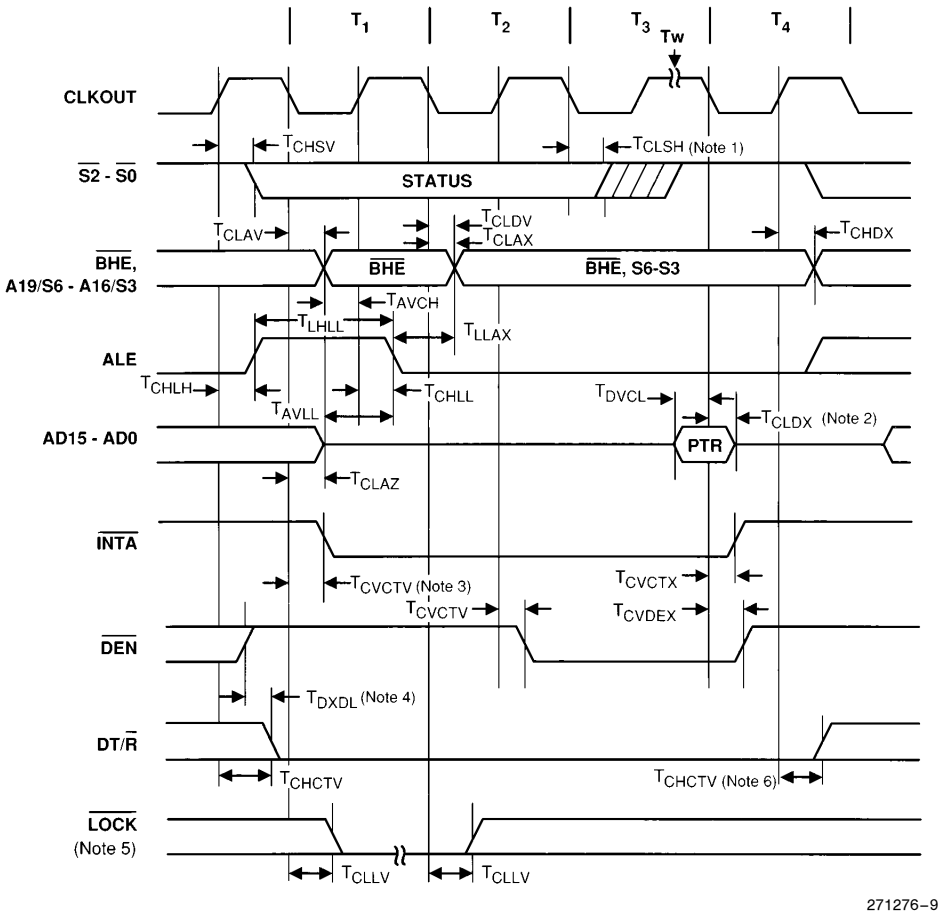
AC CHARACTERISTICS



NOTES:
1. Status inactive in state preceding T_4.
2. If latched A_1 and A_2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only T_{CLCSV} is applicable.
3. For write cycle followed by read cycle.
4. T_1 of next bus cycle.
5. Changes in T-state preceding next bus cycle if followed by read, INTA, or halt.

Figure 6. Write Cycle Waveforms

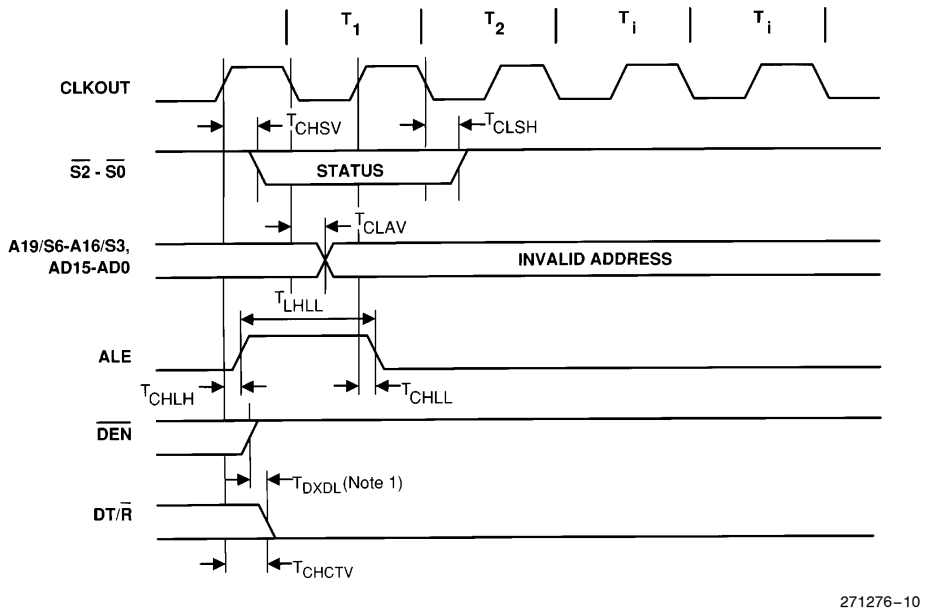
AC CHARACTERISTICS



NOTES:
1. Status inactive in state preceding T_4.
2. The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to T_{CLDX} (min).
3. $\overline{INTA}$ occurs one clock later in Slave Mode.
4. For write cycle followed by interrupt acknowledge cycle.
5. $\overline{LOCK}$ is active upon T_1 of the first interrupt acknowledge cycle and inactive upon T_2 of the second interrupt acknowledge cycle.
6. Changes in T-state preceding next bus cycle if followed by write.

Figure 7. Interrupt Acknowledge Cycle Waveforms

AC CHARACTERISTICS



NOTE:
1. For write cycle followed by halt cycle.

Figure 8. Software Halt Cycle Waveforms

WAVEFORMS

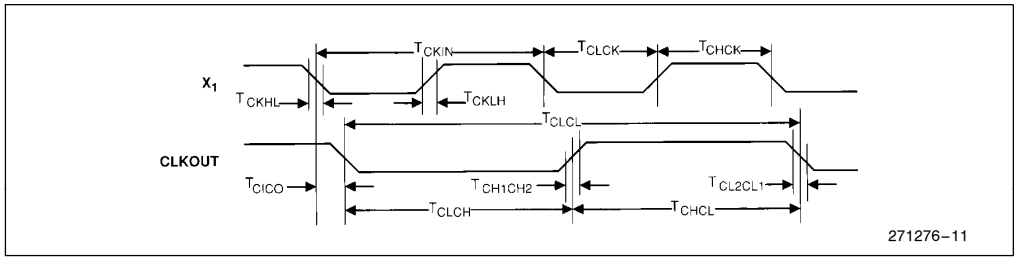


Figure 9. Clock Waveforms

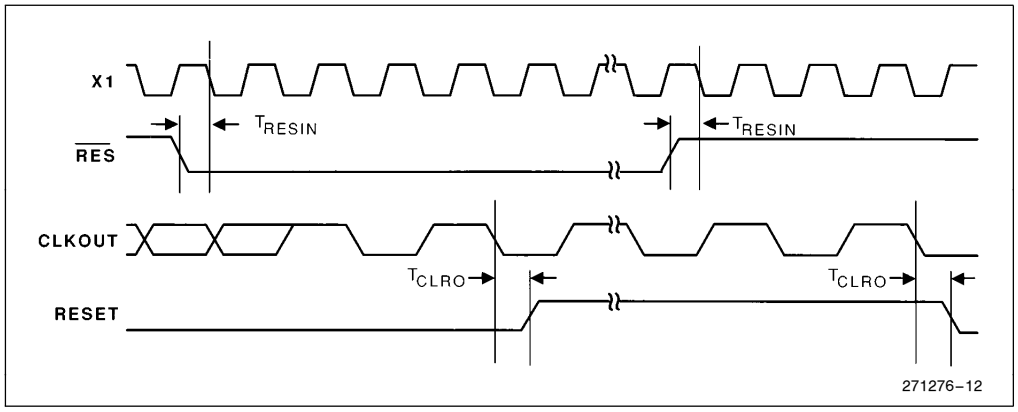


Figure 10. Reset Waveforms

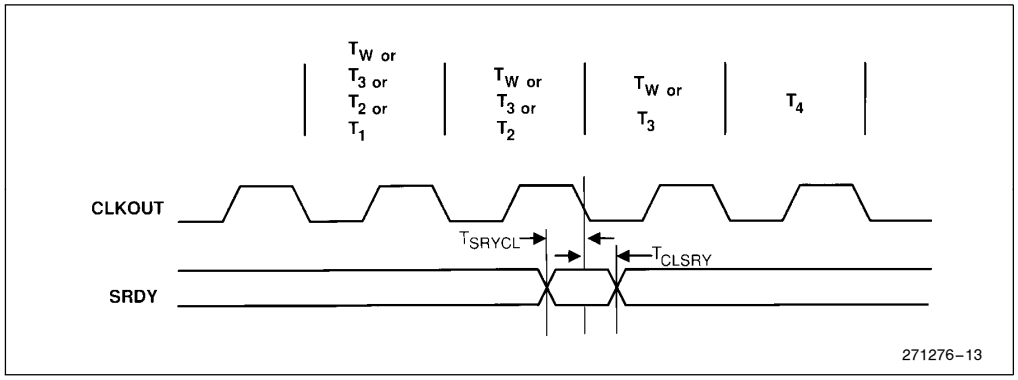


Figure 11. Synchronous Ready (SRDY) Waveforms

AC CHARACTERISTICS

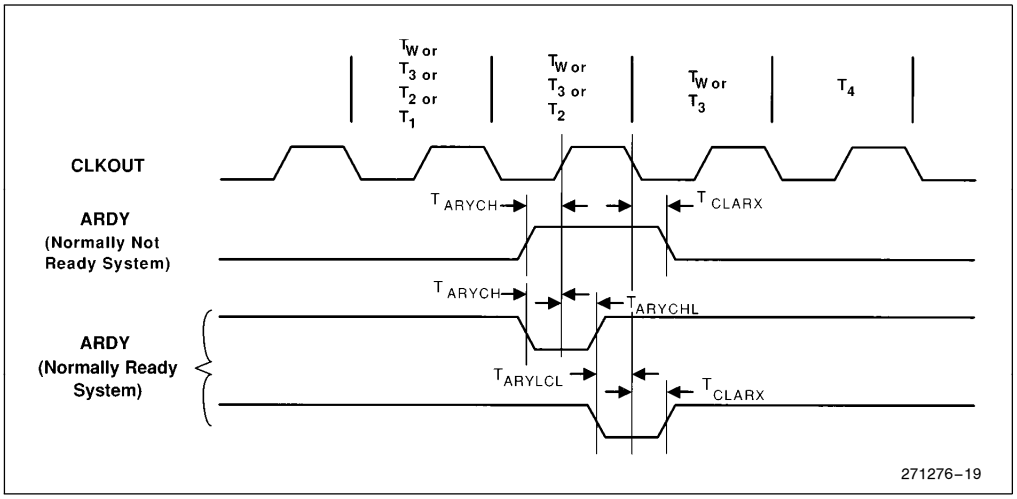


Figure 12. Asynchronous Ready (ARDY) Waveforms

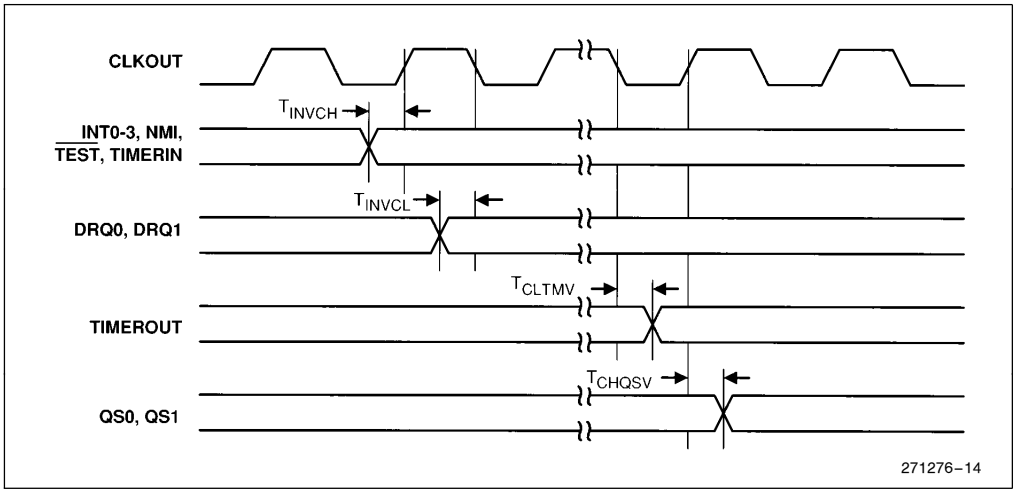


Figure 13. Peripheral and Queue Status Waveforms

AC CHARACTERISTICS

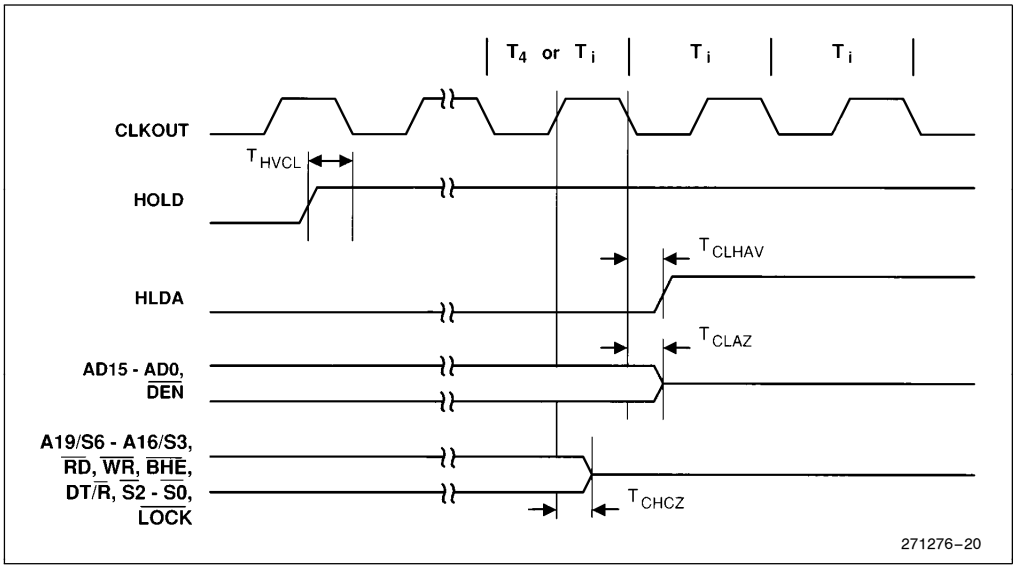


Figure 14. HOLD/HLDA Waveforms (Entering Hold)

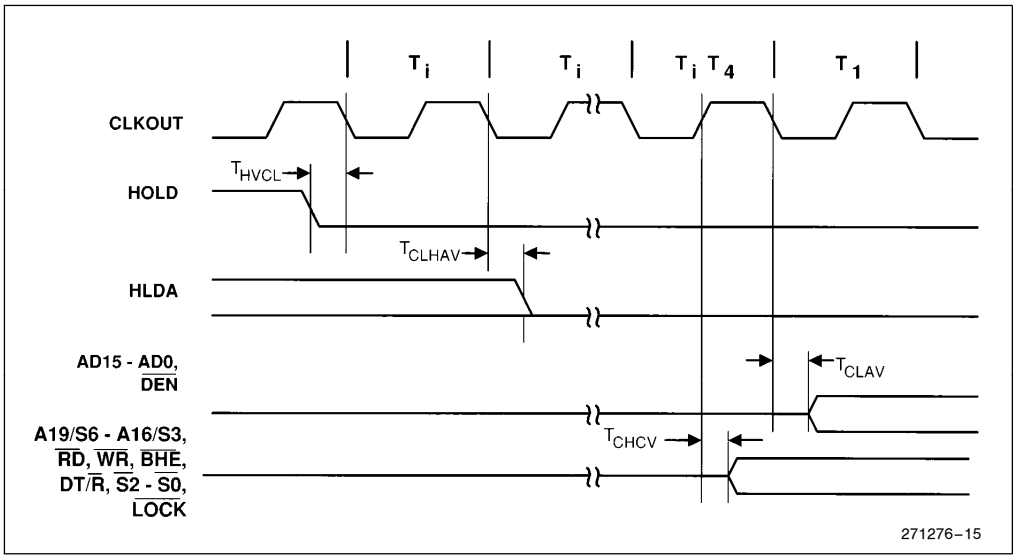


Figure 15. HOLD/HLDA Waveforms (Leaving Hold)

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has from 5 to 7 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
ARY: Asynchronous Ready Input
C: Clock Output
CK: Clock Input
CS: Chip Select
CT: Control (DT/$\overline{R}$, $\overline{DEN}$, . . .)
D: Data Input
DE: $\overline{DEN}$
H: Logic Level High
OUT: Input (DRQ0, TIM0, . . .)
L: Logic Level Low or ALE
O: Output
QS: Queue Status (QS1, QS2)
R: $\overline{RD}$ Signal, RESET Signal
S: Status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$)
SRY: Synchronous Ready Input
V: Valid
W: WR Signal
X: No Longer a Valid Logic Level
Z: Float

Examples:

T_{CLAV} — Time from Clock low to Address valid
T_{CHLH} — Time from Clock high to ALE high
T_{CLCSV} — Time from Clock low to Chip Select valid

DERATING CURVES

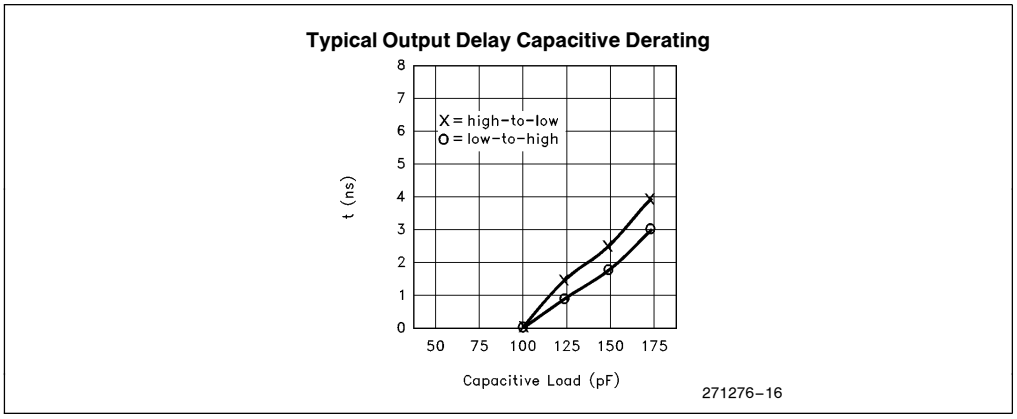


Figure 16. Capacitive Derating Curve

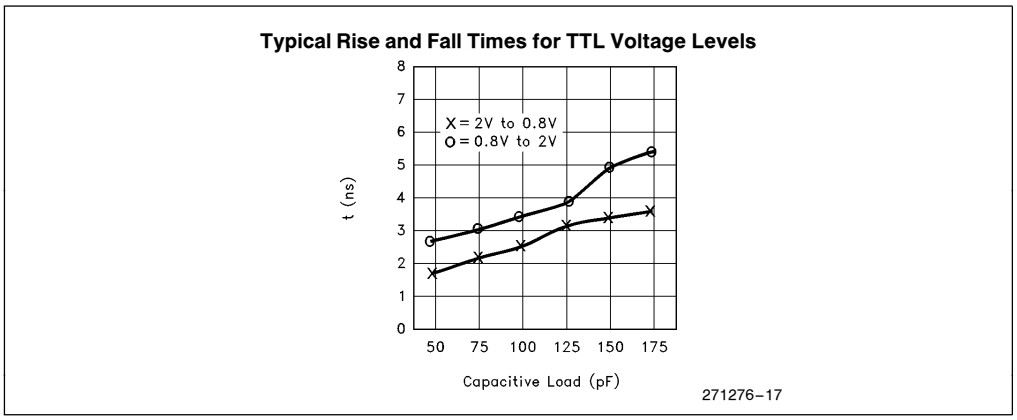


Figure 17. TTL Level Rise and Fall Times for Output Buffers

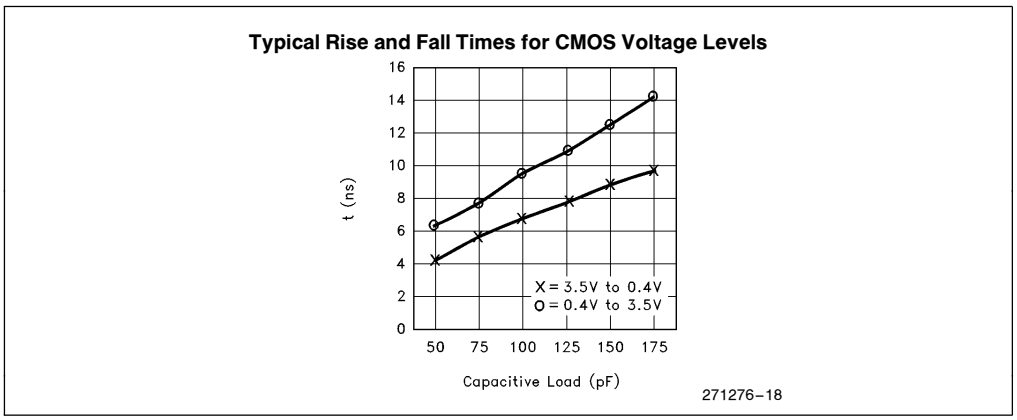


Figure 18. CMOS Level Rise and Fall Times for Output Buffers

M80C186XL EXECUTION TIMINGS

A determination of M80C186XL program execution timing must consider the bus cycles necessary to prefetch instructions as well as the number of execution unit cycles necessary to execute instructions. The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory accesses can require one or two additional clocks above the minimum timings shown due to the asynchronous handshake between the bus interface unit (BIU) and execution unit.

With a 16-bit BIU, the M80C186XL has sufficient bus performance to ensure that an adequate number of prefetched bytes will reside in the queue most of the time. Therefore, actual program execution time will not be substantially greater than that derived from adding the instruction timings shown.

INSTRUCTION SET SUMMARY

Function	Format				Clock Cycles	Comments
DATA TRANSFER						
MOV = Move:						
Register to Register/Memory	1 0 0 0 1 0 0 w	mod reg r/m			2/12	
Register/memory to register	1 0 0 0 1 0 1 w	mod reg r/m			2/9	
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 000 r/m	data	data if w = 1	12–13	8/16-bit
Immediate to register	1 0 1 1 w reg	data	data if w = 1		3–4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high		8	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high		9	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m			2/9	
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m			2/11	
PUSH = Push:						
Memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m			16	
Register	0 1 0 1 0 reg				10	
Segment register	0 0 0 reg 1 1 0				9	
Immediate	0 1 1 0 1 0 s 0	data	data if s = 0		10	
PUSHA = Push All	0 1 1 0 0 0 0 0				36	
POP = Pop:						
Memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m			20	
Register	0 1 0 1 1 reg				10	
Segment register	0 0 0 reg 1 1 1	(reg≠01)			8	
POPA = Pop All	0 1 1 0 0 0 0 1				51	
XCHG = Exchange:						
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m			4/17	
Register with accumulator	1 0 0 1 0 reg				3	
IN = Input from:						
Fixed port	1 1 1 0 0 1 0 w	port			10	
Variable port	1 1 1 0 1 1 0 w				8	
OUT = Output to:						
Fixed port	1 1 1 0 0 1 1 w	port			9	
Variable port	1 1 1 0 1 1 1 w				7	
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1				11	
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m			6	
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m	(mod≠11)		18	
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m	(mod≠11)		18	
LAHF = Load AH with flags	1 0 0 1 1 1 1 1				2	
SAHF = Store AH into flags	1 0 0 1 1 1 1 0				3	
PUSHF = Push flags	1 0 0 1 1 1 0 0				9	
POPF = Pop flags	1 0 0 1 1 1 0 1				8	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
DATA TRANSFER (Continued)						
SEGMENT = Segment Override:						
CS	00101110				2	
SS	00110110				2	
DS	00111110				2	
ES	00100110				2	
ARITHMETIC						
ADD = Add:						
Reg/memory with register to either	000000dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0000010w	data	data if w=1		3/4	8/16-bit
ADC = Add with carry:						
Reg/memory with register to either	000100dw	mod reg r/m			3/10	
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w=01	4/16	
Immediate to accumulator	0001010w	data	data if w=1		3/4	8/16-bit
INC = Increment:						
Register/memory	1111111w	mod 000 r/m			3/15	
Register	01000 reg				3	
SUB = Subtract:						
Reg/memory and register to either	001010dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0010110w	data	data if w=1		3/4	8/16-bit
SBB = Subtract with borrow:						
Reg/memory and register to either	000110dw	mod reg r/m			3/10	
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w=01	4/16	
Immediate from accumulator	0001110w	data	data if w=1		3/4	8/16-bit
DEC = Decrement						
Register/memory	1111111w	mod 001 r/m			3/15	
Register	01001 reg				3	
CMP = Compare:						
Register/memory with register	0011101w	mod reg r/m			3/10	
Register with register/memory	0011100w	mod reg r/m			3/10	
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w=01	3/10	
Immediate with accumulator	0011110w	data	data if w=1		3/4	8/16-bit
NEG = Change sign register/memory	1111011w	mod 011 r/m			3/10	
AAA = ASCII adjust for add	00110111				8	
DAA = Decimal adjust for add	00100111				4	
AAS = ASCII adjust for subtract	00111111				7	
DAS = Decimal adjust for subtract	00101111				4	
MUL = Multiply (unsigned):	1111011w	mod 100 r/m				
Register-Byte					26–28	
Register-Word					35–37	
Memory-Byte					32–34	
Memory-Word					41–43	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
ARITHMETIC (Continued)						
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w	mod 1 0 1 r/m				
Register-Byte					25–28	
Register-Word					34–37	
Memory-Byte					31–34	
Memory-Word					40–43	
IMUL = Integer Immediate multiply (signed)	0 1 1 0 1 0 s 1	mod reg r/m	data	data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w	mod 1 1 0 r/m				
Register-Byte					29	
Register-Word					38	
Memory-Byte					35	
Memory-Word					44	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w	mod 1 1 1 r/m				
Register-Byte					44–52	
Register-Word					53–61	
Memory-Byte					50–58	
Memory-Word					59–67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0			19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0			15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0				2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1				4	
LOGIC **Shift/Rotate Instructions:**						
Register/Memory by 1	1 1 0 1 0 0 0 w	mod TTT r/m			2/15	
Register/Memory by CL	1 1 0 1 0 0 1 w	mod TTT r/m			5+n/17+n	
Register/Memory by Count	1 1 0 0 0 0 0 w	mod TTT r/m	count		5+n/17+n	
	TTT Instruction 0 0 0 ROL 0 0 1 ROR 0 1 0 RCL 0 1 1 RCR 1 0 0 SHL/SAL 1 0 1 SHR 1 1 1 SAR					
AND = **And:**						
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1		3/4	8/16-bit
TEST = **And function to flags, no result:**						
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1		3/4	8/16-bit
OR = **Or:**						
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1		3/4	8/16-bit

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
LOGIC (Continued)						
XOR = **Exclusive or:**						
Reg/memory and register to either	0 0 1 1 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1	4/16	
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1		3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w	mod 0 1 0 r/m			3/10	
STRING MANIPULATION						
MOVS = Move byte/word	1 0 1 0 0 1 0 w				14	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w				22	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w				15	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w				12	
STOS = Store byte/wd from AL/AX	1 0 1 0 1 0 1 w				10	
INS = Input byte/wd from DX port	0 1 1 0 1 1 0 w				14	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w				14	
Repeated by count in CX (REP/REPE/REPZ/REPNE/REPNZ)						
MOVS = Move string	1 1 1 1 0 0 1 0	1 0 1 0 0 1 0 w			8 + 8n	
CMPS = Compare string	1 1 1 1 0 0 1 z	1 0 1 0 0 1 1 w			5 + 22n	
SCAS = Scan string	1 1 1 1 0 0 1 z	1 0 1 0 1 1 1 w			5 + 15n	
LODS = Load string	1 1 1 1 0 0 1 0	1 0 1 0 1 1 0 w			6 + 11n	
STOS = Store string	1 1 1 1 0 0 1 0	1 0 1 0 1 0 1 w			6 + 9n	
INS = Input string	1 1 1 1 0 0 1 0	0 1 1 0 1 1 0 w			8 + 8n	
OUTS = Output string	1 1 1 1 0 0 1 0	0 1 1 0 1 1 1 w			8 + 8n	
CONTROL TRANSFER						
CALL = **Call:**						
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high		15	
Register/memory indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m			13/19	
Direct intersegment	1 0 0 1 1 0 1 0	segment offset			23	
		segment selector				
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	(mod ≠ 11)		38	
JMP = **Unconditional jump:**						
Short/long	1 1 1 0 1 0 1 1	disp-low			14	
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high		14	
Register/memory indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m			11/17	
Direct intersegment	1 1 1 0 1 0 1 0	segment offset			14	
		segment selector				
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	(mod ≠ 11)		26	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format				Clock Cycles	Comments
CONTROL TRANSFER (Continued)						
RET = **Return from CALL:**						
Within segment	11000011				16	
Within seg adding immed to SP	11000010	data-low	data-high		18	
Intersegment	11001011				22	
Intersegment adding immediate to SP	11001010	data-low	data-high		25	
JE/JZ = Jump on equal/zero	01110100	disp			4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp			4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp			4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp			4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp			4/13	
JP/JPE = Jump on parity/parity even	01111010	disp			4/13	
JO = Jump on overflow	01110 000	disp			4/13	
JS = Jump on sign	01111000	disp			4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp			4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp			4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp			4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp			4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp			4/13	
JNP/JPO = Jump on not par/par odd	01111011	disp			4/13	
JNO = Jump on not overflow	01110001	disp			4/13	
JNS = Jump on not sign	01111001	disp			4/13	
JCXZ = Jump on CX zero	11100011	disp			5/15	
LOOP = Loop CX times	11100010	disp			6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp			6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp			6/16	
ENTER = Enter Procedure	11001000	data-low	data-high	L		
L = 0					15	
L = 1					25	
L > 1					22+16(n−1)	
LEAVE = Leave Procedure	11001001				8	
INT = **Interrupt:**						
Type specified	11001101	type			47	
Type 3	11001100				45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	11001110				48/4	
IRET = Interrupt return	11001111				28	
BOUND = Detect value out of range	01100010	mod reg r/m			33–35	

Shaded areas indicate instructions not available in 8086/8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
NOP = No Operation	10010000	3	
	(TTT LLL are opcode to processor extension)		

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FOOTNOTES

The Effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment Override Prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

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