



## 8XC196KD/8XC196KD20 COMMERCIAL CHMOS MICROCONTROLLER

87C196KD—32 Kbytes of On-Chip OTPROM

83C196KD—32 Kbytes of ROM

- 16 MHz and 20 MHz Available
- 1000 Byte Register RAM
- Register-to-Register Architecture
- 28 Interrupt Sources/16 Vectors
- Peripheral Transaction Server
- 1.4  $\mu$ s 16 x 16 Multiply (20 MHz)
- 2.4  $\mu$ s 32/16 Divide (20 MHz)
- Powerdown and Idle Modes
- Five 8-Bit I/O Ports
- 16-Bit Watchdog Timer
- Dynamically Configurable 8-Bit or 16-Bit Buswidth
- Full Duplex Serial Port
- High Speed I/O Subsystem
- 16-Bit Timer
- 16-Bit Up/Down Counter with Capture
- 3 Pulse-Width-Modulated Outputs
- Four 16-Bit Software Timers
- 8- or 10-Bit A/D Converter with Sample/Hold
- $\overline{\text{HOLD}}/\overline{\text{HLDA}}$  Bus Protocol
- OTP One-Time Programmable Version

The 8XC196KD 16-bit microcontroller is a high performance member of the MCS<sup>®</sup> 96 microcontroller family. The 8XC196KD is an enhanced 80C196KC device with 1000 bytes RAM, 16 MHz operation and an optional 32 Kbytes of ROM/EPROM. Intel's CHMOS III process provides a high performance processor along with low power consumption.

The 8XC196KD has a maximum guaranteed frequency of 16 MHz. The 8XC196KD20 has a maximum guaranteed frequency of 20 MHz. Unless otherwise noted, all references to the 8XC196KD also refer to the 8XC196KD20.

Four high-speed capture inputs are provided to record times when events occur. Six high-speed outputs are available for pulse or waveform generation. The high-speed output can also generate four software timers or start an A/D conversion. Events can be based on the timer or up/down counter.

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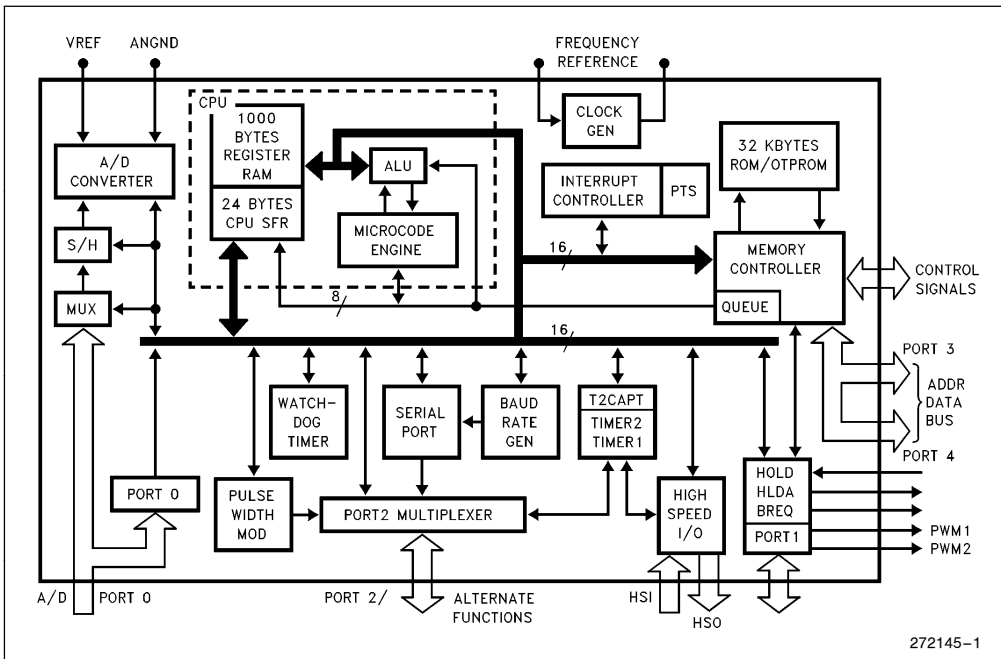


Figure 1. 8XC196KD Block Diagram

**87C196KD ENHANCED FEATURE SET OVER THE 87C196KC**

1. The 87C196KD has twice the RAM and twice the OTPROM space of the 87C196KC.
2. The vertical windowing scheme has been extended to allow all 1000 bytes of register RAM to be windowed into the lower bytes register file.

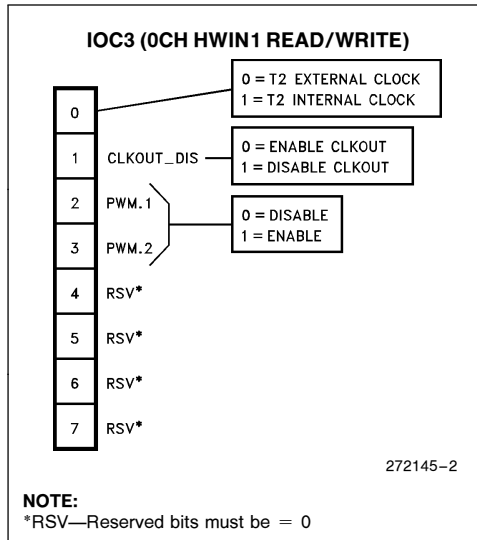


Figure 2. 87C196KD New SFR Bit (CLKOUT Disable)



**8XC196KD VERTICAL WINDOWING MAP**

**Table 1. 128-Byte Windows**

Address to Remap	Device Series	WSR Contents
0380H	KD	X001 0111B = 17H
0300H	KD	X001 0110B = 16H
0280H	KD	X001 0101B = 15H
0200H	KD	X001 0100B = 14H
0180H	KC, KD	X001 0011B = 13H
0100H	KC, KD	X001 0010B = 12H
0080H	KC, KD	X001 0001B = 11H
0000H	KC, KD	X001 0000B = 10H

Window in Lower Register File: 80H–FFH

**Table 2. 64-Byte Windows**

Address to Remap	Device Series	WSR Contents
03C0H	KD	X010 1111B = 2FH
0380H	KD	X010 1110B = 2EH
0340H	KD	X010 1101B = 2DH
0300H	KD	X010 1100B = 2CH
02C0H	KD	X010 1011B = 2BH
0280H	KD	X010 1010B = 2AH
0240H	KD	X010 1001B = 29H
0200H	KD	X010 1000B = 28H
01C0H	KC, KD	X010 0111B = 27H
0180H	KC, KD	X010 0110B = 26H
0140H	KC, KD	X010 0101B = 25H
0100H	KC, KD	X010 0100B = 24H
00C0H	KC, KD	X010 0011B = 23H
0080H	KC, KD	X010 0010B = 22H
0040H	KC, KD	X010 0001B = 21H
0000H	KC, KD	X010 0000B = 20H

Window in Lower Register File: C0H–FFH

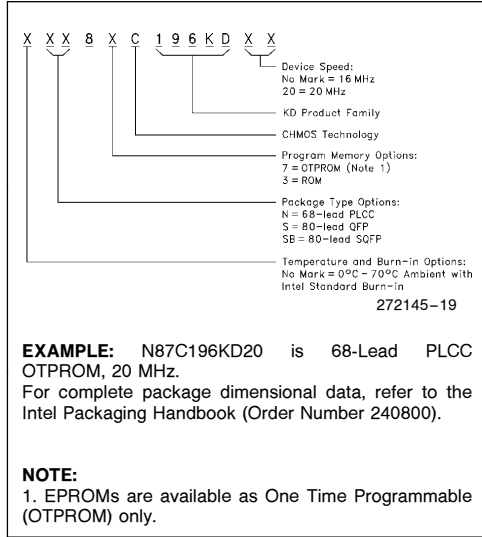
**Table 3. 32-Byte Windows**

Address to Remap	Device Series	WSR Contents
03E0H	KD	X101 1111B = 5FH
03C0H	KD	X101 1110B = 5EH
03A0H	KD	X101 1101B = 5DH
0380H	KD	X101 1100B = 5CH
0360H	KD	X101 1011B = 5BH
0340H	KD	X101 1010B = 5AH
0320H	KD	X101 1001B = 59H
0300H	KD	X101 1000B = 58H
02E0H	KD	X101 0111B = 57H
02C0H	KD	X101 0110B = 56H
02A0H	KD	X101 0101B = 55H
0280H	KD	X101 0100B = 54H
0260H	KD	X101 0011B = 53H
0240H	KD	X101 0010B = 52H
0220H	KD	X101 0001B = 51H
0200H	KD	X101 0000B = 50H
01E0H	KC, KD	X100 1111B = 4FH
01C0H	KC, KD	X100 1110B = 4EH
01A0H	KC, KD	X100 1101B = 4DH
0180H	KC, KD	X100 1100B = 4CH
0160H	KC, KD	X100 1011B = 4BH
0140H	KC, KD	X100 1010B = 4AH
0120H	KC, KD	X100 1001B = 49H
0100H	KC, KD	X100 1000B = 48H
00E0H	KC, KD	X100 0111B = 47H
00C0H	KC, KD	X100 0110B = 46H
00A0H	KC, KD	X100 0101B = 45H
0080H	KC, KD	X100 0100B = 44H
0060H	KC, KD	X100 0011B = 43H
0040H	KC, KD	X100 0010B = 42H
0020H	KC, KD	X100 0001B = 41H
0000H	KC, KD	X100 0000B = 40H

Window in Lower Register File: E0H–FFH

**PROCESS INFORMATION**

This device is manufactured on PX29.5 or PX29.9, a CHMOS III process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook*, Order Number 210997.



**Figure 3. The 8XC196KD Family Nomenclature**

**Table 4. Thermal Characteristics**

Package Type	$\theta_{ja}$	$\theta_{jc}$
PLCC	35°C/W	13°C/W
QFP	56°C/W	12°C/W
SQFP	68°C/W	15.5°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operation conditions and application. See the Intel *Packaging Handbook* (order number 240800) for a description of Intel's thermal impedance test methodology.

**Table 5. 8XC196KD Memory Map**

Description	Address
External Memory or I/O	0FFFFH 0A000H
Internal ROM/OTPROM or External Memory (Determined by EA)	9FFFH 2080H
Reserved. Must contain FFH. (Note 5)	207FH 205EH
PTS Vectors	205DH 2040H
Upper Interrupt Vectors	203FH 2030H
ROM/OTPROM Security Key	202FH 2020H
Reserved. Must contain FFH. (Note 5)	201FH 201AH
Reserved. Must Contain 20H (Note 5)	2019H
CCB	2018H
Reserved. Must contain FFH. (Note 5)	2017H 2014H
Lower Interrupt Vectors	2013H 2000H
Port 3 and Port 4	1FFFH 1FFEh
External Memory	1FFDH 0400H
1000 Bytes Register RAM (Note 1)	03FFH 0018H
CPU SFR's (Notes 1, 3)	0017H 0000H

**NOTES:**

- Code executed in locations 0000H to 03FFH will be forced external.
- Reserved memory locations must contain 0FFH unless noted.
- Reserved SFR bit locations must contain 0.
- Refer to 8XC196KC for SFR descriptions.
- WARNING:** Reserved memory locations must not be written or read. The contents and/or function of these locations may change with future revisions of the device. Therefore, a program that relies on one or more of these locations may not function properly.

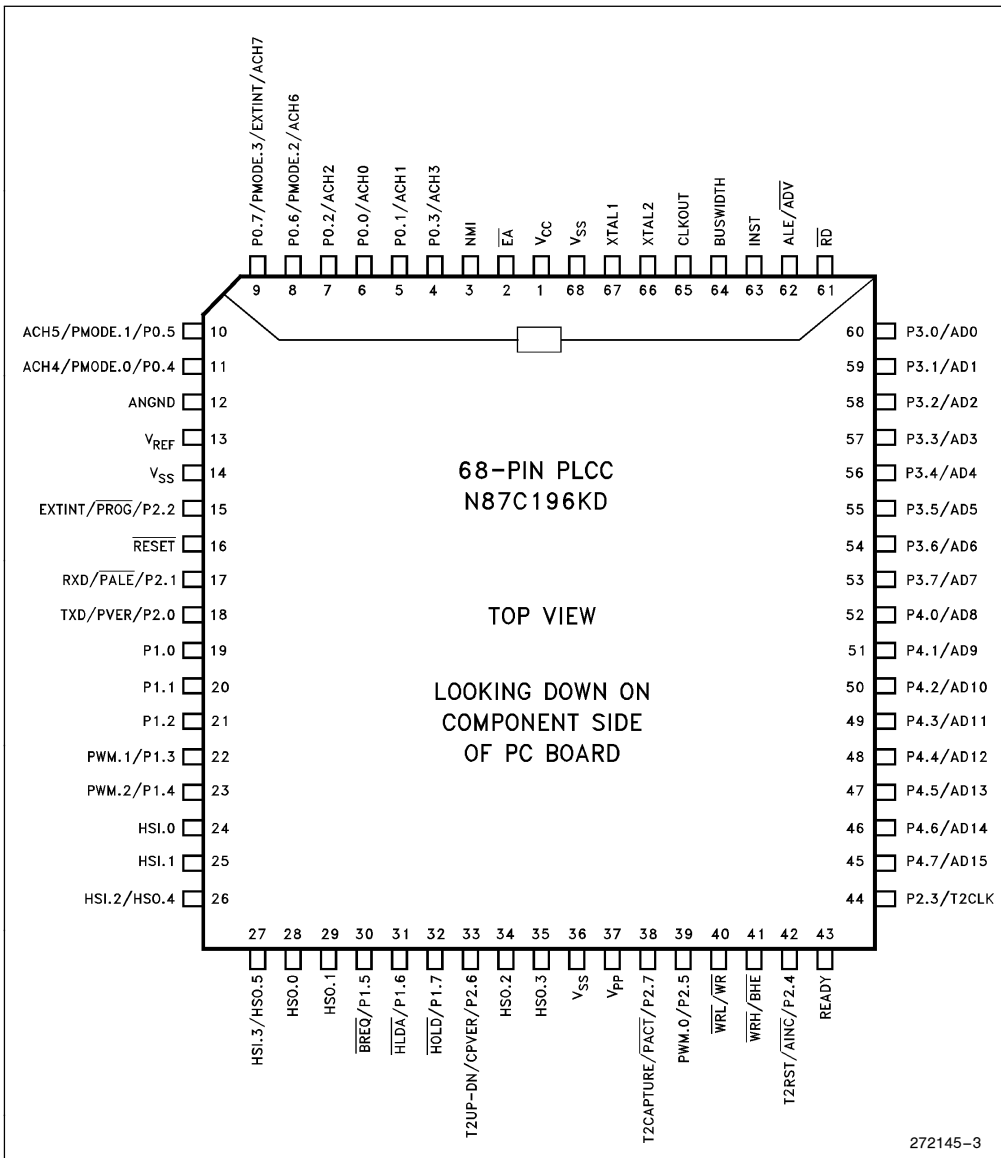


Figure 4. 68-Pin PLCC Package

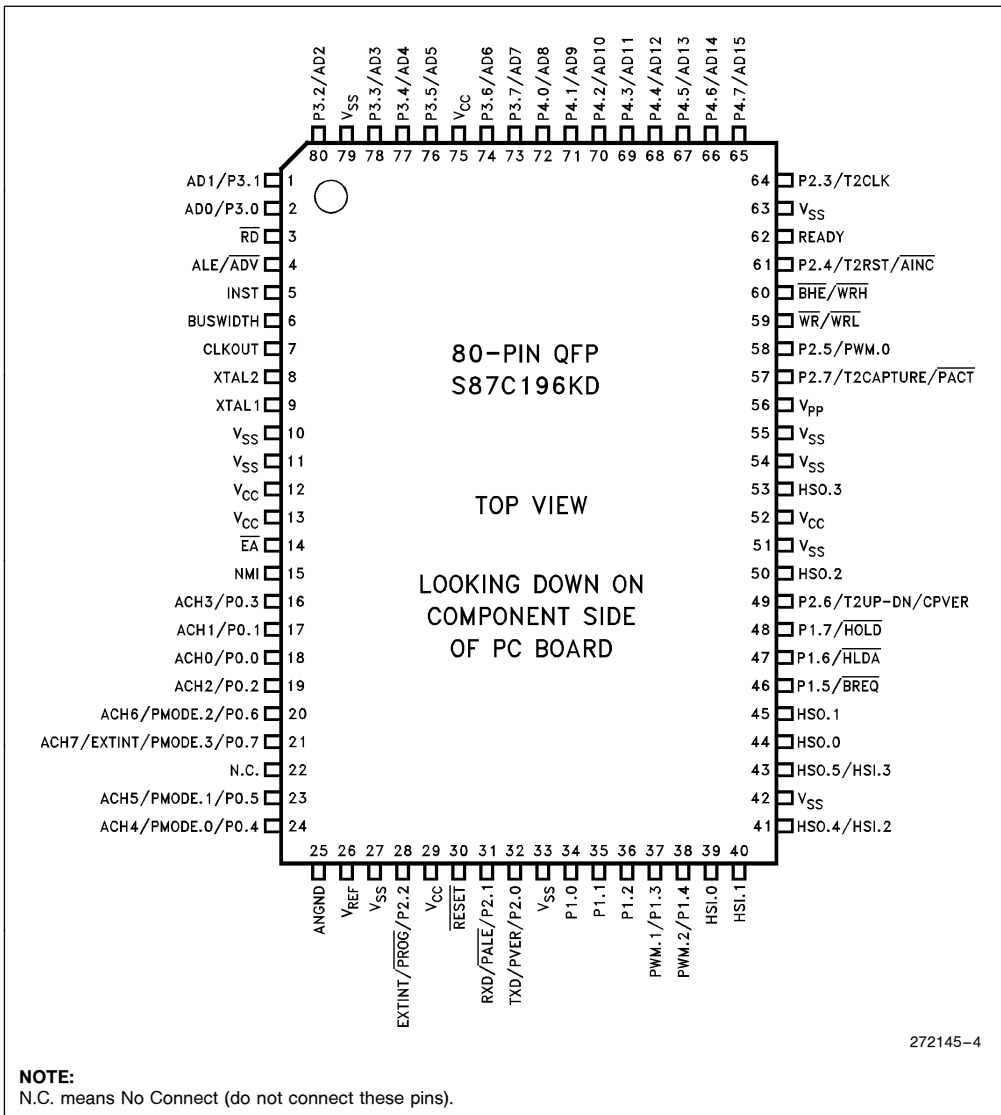


Figure 5. 80-Pin QFP Package

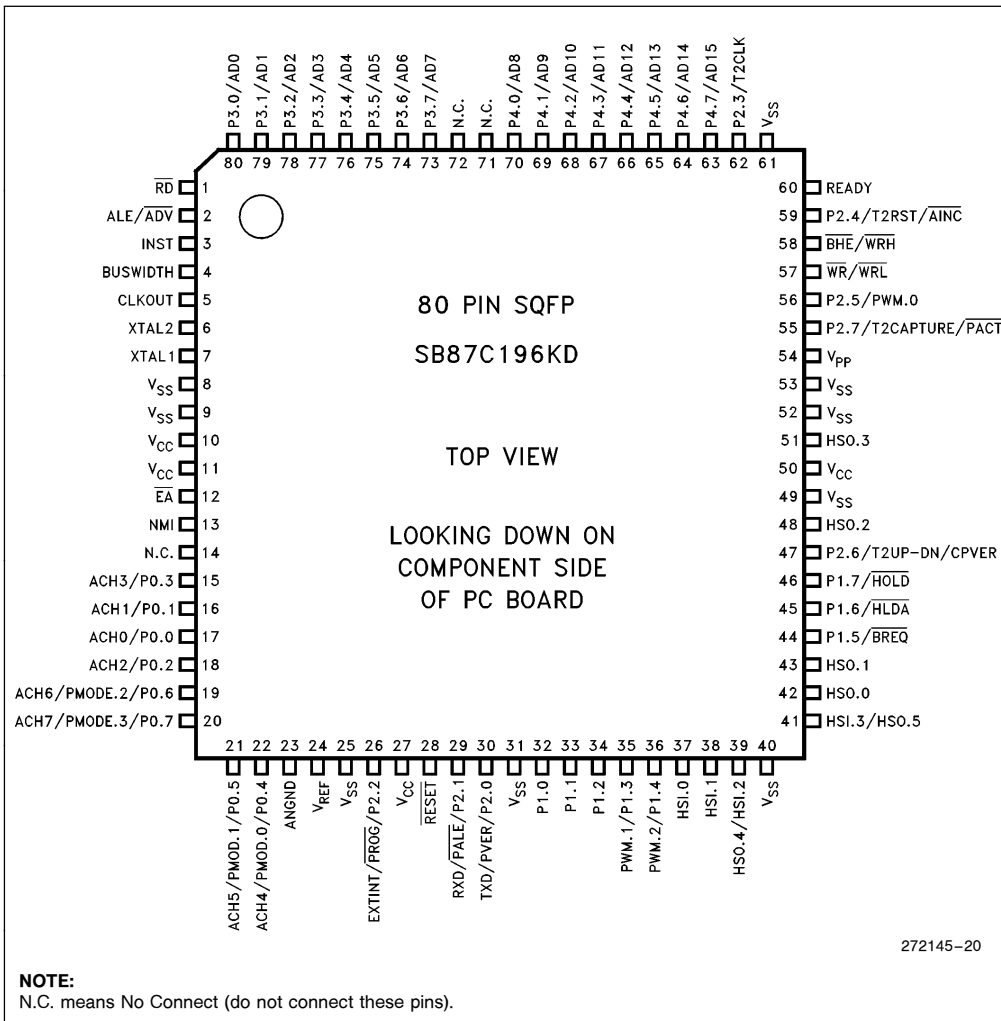


Figure 6. 80-Pin SQFP Package

## PIN DESCRIPTIONS

Symbol	Name and Function
V <sub>CC</sub>	Main supply voltage (5V).
V <sub>SS</sub>	Digital circuit ground (0V). There are multiple V <sub>SS</sub> pins, all of which must be connected.
V <sub>REF</sub>	Reference voltage for the A/D converter (5V). V <sub>REF</sub> is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V <sub>SS</sub> .
V <sub>PP</sub>	Timing pin for the return from powerdown circuit. This pin also supplies the programming voltage on the EPROM device.
XTAL1	Input of the oscillator inverter and of the internal clock generator.
XTAL2	Output of the oscillator inverter.
CLKOUT	Output of the internal clock generator. The frequency of CLKOUT is 1/2 the oscillator frequency.
RESET	Reset input and open drain output.
BUSWIDTH	Input for buswidth selection. If CCR bit 1 is a one, this pin selects the bus width for the bus cycle in progress. If BUSWIDTH is a 1, a 16-bit bus cycle occurs. If BUSWIDTH is a 0 an 8-bit cycle occurs. If CCR bit 1 is a 0, the bus is always an 8-bit bus.
NMI	A positive transition causes a vector through 203EH.
INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is activated only during external memory accesses and output low for a data fetch.
$\overline{EA}$	Input for memory select (External Access). $\overline{EA}$ equal high causes memory accesses to locations 2000H through 9FFFH to be directed to on-chip ROM/EPROM. $\overline{EA}$ equal low causes accesses to those locations to be directed to off-chip memory. Also used to enter programming mode.
ALE/ $\overline{ADV}$	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a signal to demultiplex the address from the address/data bus. When the pin is $\overline{ADV}$ , it goes inactive high at the end of the bus cycle. ALE/ $\overline{ADV}$ is activated only during external memory accesses.
$\overline{RD}$	Read signal output to external memory. $\overline{RD}$ is activated only during external memory reads.
$\overline{WR}/\overline{WRL}$	Write and Write Low output to external memory, as selected by the CCR. $\overline{WR}$ will go low for every external write, while $\overline{WRL}$ will go low only for external writes where an even byte is being written. $\overline{WR}/\overline{WRL}$ is activated only during external memory writes.
$\overline{BHE}/\overline{WRH}$	Bus High Enable or Write High output to external memory, as selected by the CCR. $\overline{BHE}$ will go low for external writes to the high byte of the data bus. $\overline{WRH}$ will go low for external writes where an odd byte is being written. $\overline{BHE}/\overline{WRH}$ is activated only during external memory writes.
READY	Ready input to lengthen external memory cycles, for interfacing to slow or dynamic memory, or for bus sharing. When the external memory is not being used, READY has no effect.
HSI	Inputs to High Speed Input Unit. Four HSI pins are available: HSI.0, HSI.1, HSI.2 and HSI.3. Two of them (HSI.2 and HSI.3) are shared with the HSO Unit.
HSO	Outputs from High Speed Output Unit. Six HSO pins are available: HSO.0, HSO.1, HSO.2, HSI.3, HSO.4 and HSO.5. Two of them (HSO.4 and HSO.5) are shared with the HSI Unit.



**PIN DESCRIPTIONS** (Continued)

Symbol	Name and Function
Port 0	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter.
Port 1	8-bit quasi-bidirectional I/O port.
Port 2	8-bit multi-functional port. All of its pins are shared with other functions in the 8XC196KD. Pins 2.6 and 2.7 are quasi-bidirectional.
Ports 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
$\overline{\text{HOLD}}$	Bus Hold input requesting control of the bus.
$\overline{\text{HLDA}}$	Bus Hold acknowledge output indicating release of the bus.
$\overline{\text{BREQ}}$	Bus Request output activated when the bus controller has a pending external memory cycle.
PMODE	Determines the EPROM programming mode.
$\overline{\text{PACT}}$	A low signal in Auto Programming mode indicates that programming is in process. A high signal indicates programming is complete.
$\overline{\text{PALE}}$	A falling edge in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates that ports 3 and 4 contain valid programming address/command information (input to slave).
$\overline{\text{PROG}}$	A falling edge in Slave Programming Mode indicates that ports 3 and 4 contain valid programming data (input to slave).
PVER	A high signal in Slave Programming Mode and Auto Configuration Byte Programming Mode indicates the byte programmed correctly.
CPVER	Cummulative Program Output Verification. Pin is high if all locations have programmed correctly since entering a programming mode.
$\overline{\text{AINC}}$	Auto Increment. Active low input enables the auto increment mode. Auto increment allows reading or writing sequential EPROM locations without address transactions across the PBUS for each read or write.



**ELECTRICAL CHARACTERISTICS**

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature  
 Under Bias ..... -55°C to +125°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage On Any Pin to V<sub>SS</sub>  
 Except EA and V<sub>PP</sub> ..... -0.5V to +7.0V(1)  
 Voltage from  $\overline{EA}$  or  
 V<sub>PP</sub> to V<sub>SS</sub> or ANGND ..... -0.5V to +13.00V  
 Power Dissipation ..... 1.5W(2)

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

*\*WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**NOTES:**

1. This includes V<sub>PP</sub> and  $\overline{EA}$  on ROM or CPU only devices.
2. Power dissipation is based on package heat transfer limitations, not device power consumption.

**OPERATING CONDITIONS**

Symbol	Description	Min	Max	Units
T <sub>A</sub>	Ambient Temperature Under Bias <b>Commercial</b> Temp.	0	+70	°C
V <sub>CC</sub>	Digital Supply Voltage	4.50	5.50	V
V <sub>REF</sub>	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V <sub>SS</sub> - 0.4	V <sub>SS</sub> + 0.4	V(1)
F <sub>OSC</sub>	Oscillator Frequency ( <b>8XC196KD</b> )	8	16	MHz
F <sub>OSC</sub>	Oscillator Frequency ( <b>8XC196KD20</b> )	8	20	MHz

**NOTE:**

1. ANGND and V<sub>SS</sub> should be nominally at the same potential.

**DC CHARACTERISTICS** (Over Specified Operating Conditions)

Symbol	Description	Min	Max	Units	Test Conditions
V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	V	
V <sub>IH</sub>	Input High Voltage (Note 1)	0.2 V <sub>CC</sub> + 1.0	V <sub>CC</sub> + 0.5	V	
V <sub>HYS</sub>	Hysteresis on $\overline{RESET}$	300		mV	V <sub>CC</sub> = 5.0V
V <sub>IH1</sub>	Input High Voltage on XTAL 1	0.7 V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V	
V <sub>IH2</sub>	Input High Voltage on RESET	2.2	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage		0.3 0.45 1.5	V V V	I <sub>OL</sub> = 200 μA I <sub>OL</sub> = 2.8 mA I <sub>OL</sub> = 7 mA
V <sub>OL1</sub>	Output Low Voltage in RESET on P2.5 (Note 2)		0.8	V	I <sub>OL</sub> = +0.4 mA
V <sub>OH</sub>	Output High Voltage (Standard Outputs) (Note 4)	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5		V V V	I <sub>OH</sub> = -200 μA I <sub>OH</sub> = -3.2 mA I <sub>OH</sub> = -7 mA
V <sub>OH1</sub>	Output High Voltage (Quasi-bidirectional Outputs) (Note 3)	V <sub>CC</sub> - 0.3 V <sub>CC</sub> - 0.7 V <sub>CC</sub> - 1.5		V V V	I <sub>OH</sub> = -10 μA I <sub>OH</sub> = -30 μA I <sub>OH</sub> = -60 μA

**DC CHARACTERISTICS** (Over Specified Operating Conditions) (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Conditions
I <sub>OH1</sub>	Logical 1 Output Current in Reset on P2.0. Do not exceed this or device may enter test modes.	-0.8			mA	V <sub>IH</sub> = V <sub>CC</sub> - 1.5V
I <sub>IL2</sub>	Logical 0 Input Current in Reset on P2.0. Maximum current that must be sunk by external device to ensure test mode entry.			-12.0	mA	V <sub>IN</sub> = 0.45V
I <sub>IH1</sub>	Logical 1 Input Current. Maximum current that external device must source to initiate NMI.			+200	μA	V <sub>IN</sub> = 2.4V
I <sub>LI</sub>	Input Leakage Current (Std. Inputs) (Note 5)			±10	μA	0 < V <sub>IN</sub> < V <sub>CC</sub> - 0.3V
I <sub>LI1</sub>	Input Leakage Current (Port 0)			±3	μA	0 < V <sub>IN</sub> < V <sub>REF</sub>
I <sub>TL</sub>	1 to 0 Transition Current (QBD Pins)			-650	μA	V <sub>IN</sub> = 2.0V
I <sub>IL</sub>	Logical 0 Input Current (QBD Pins)			-70	μA	V <sub>IN</sub> = 0.45V
I <sub>IL1</sub>	AD Bus in Reset			-70	μA	V <sub>IN</sub> = 0.45V
I <sub>CC</sub>	Active Mode Current in Reset ( <b>8XC196KD</b> )		65	75	mA	XTAL1 = 16 MHz V <sub>CC</sub> = V <sub>PP</sub> = V <sub>REF</sub> = 5.5V
I <sub>CC</sub>	Active Mode Current in Reset ( <b>8XC196KD20</b> )		80	92	mA	XTAL1 = 20 MHz V <sub>CC</sub> = V <sub>PP</sub> = V <sub>REF</sub> = 5.5V
I <sub>IDLE</sub>	Idle Mode Current ( <b>8XC196KD</b> )		17	25	mA	XTAL1 = 16 MHz V <sub>CC</sub> = V <sub>PP</sub> = V <sub>REF</sub> = 5.5V
I <sub>IDLE</sub>	Idle Mode Current ( <b>8XC196KD20</b> )		21	30	mA	XTAL1 = 20 MHz V <sub>CC</sub> = V <sub>PP</sub> = V <sub>REF</sub> = 5.5V
I <sub>PD</sub>	Powerdown Mode Current		8	15	μA	V <sub>CC</sub> = V <sub>PP</sub> = V <sub>REF</sub> = 5.5V
I <sub>REF</sub>	A/D Converter Reference Current		2	5	mA	V <sub>CC</sub> = V <sub>PP</sub> = V <sub>REF</sub> = 5.5V
R <sub>RST</sub>	Reset Pullup Resistor	6K		65K	Ω	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 4.0V
C <sub>S</sub>	Pin Capacitance (Any Pin to V <sub>SS</sub> )			10	pF	

**NOTES:**

- All pins except RESET and XTAL1.
- Violating these specifications in Reset may cause the part to enter test modes.
- QBD (Quasi-bidirectional) pins include Port 1, P2.6 and P2.7.
- Standard Outputs include AD0-15, RD, WR, ALE, BHE, INST, HSO pins, PWM/P2.5, CLKOUT, RESET, Ports 3 and 4, TXD/P2.0 and RXD (in serial mode 0). The V<sub>OH</sub> specification is not valid for RESET. Ports 3 and 4 are open-drain outputs.
- Standard Inputs include HSI pins, READY, BUSWIDTH, RXD/P2.1, EXTINT/P2.2, T2CLK/P2.3 and T2RST/P2.4.
- Maximum current per pin must be externally limited to the following values if V<sub>OL</sub> is held above 0.45V or V<sub>OH</sub> is held below V<sub>CC</sub> - 0.7V:
  - I<sub>OL</sub> on Output pins: 10 mA
  - I<sub>OH</sub> on quasi-bidirectional pins: self limiting
  - I<sub>OH</sub> on Standard Output pins: 10 mA
- Maximum current per bus pin (data and control) during normal operation is ±3.2 mA.
- During normal (non-transient) conditions the following total current limits apply:
 

Port 1, P2.6	I <sub>OL</sub> : 29 mA	I <sub>OH</sub> is self limiting
HSO, P2.0, RXD, RESET	I <sub>OL</sub> : 29 mA	I <sub>OH</sub> : 26 mA
P2.5, P2.7, WR, BHE	I <sub>OL</sub> : 13 mA	I <sub>OH</sub> : 11 mA
AD0-AD15	I <sub>OL</sub> : 52 mA	I <sub>OH</sub> : 52 mA
RD, ALE, INST-CLKOUT	I <sub>OL</sub> : 13 mA	I <sub>OH</sub> : 13 mA

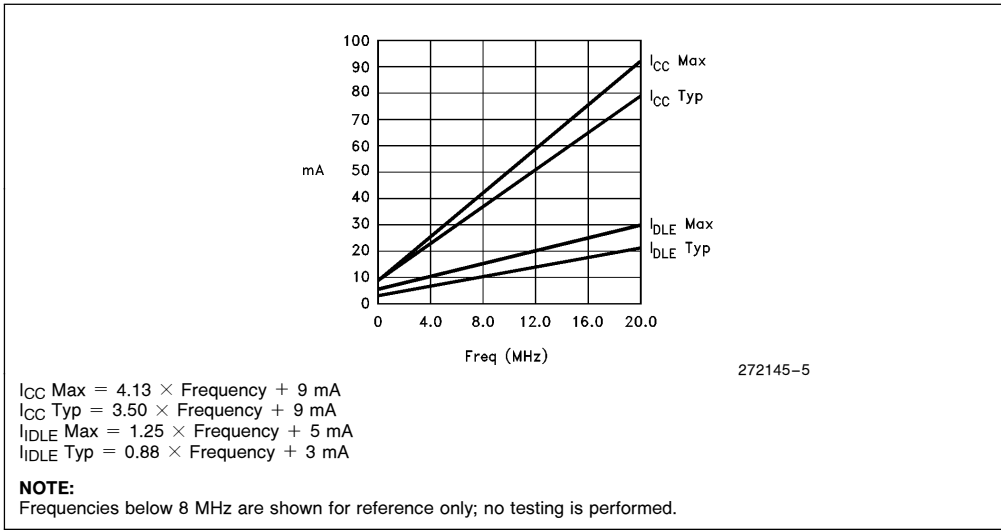


Figure 7. I<sub>CC</sub> and I<sub>IDLE</sub> vs Frequency

**AC CHARACTERISTICS**

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F<sub>OSC</sub> = 16/20 MHz

The system must meet these specifications to work with the 80C196KD:

Symbol	Description	Min	Max	Units	Notes
T <sub>AVYV</sub>	Address Valid to READY Setup		2 T <sub>OSC</sub> - 68	ns	
T <sub>YLYH</sub>	Non READY Time	No upper limit		ns	
T <sub>CLYX</sub>	READY Hold after CLKOUT Low	0	T <sub>OSC</sub> - 30	ns	(Note 1)
T <sub>LLYX</sub>	READY Hold after ALE Low	T <sub>OSC</sub> - 15	2 T <sub>OSC</sub> - 40	ns	(Note 1)
T <sub>AVGV</sub>	Address Valid to Buswidth Setup		2 T <sub>OSC</sub> - 68	ns	
T <sub>CLGX</sub>	Buswidth Hold after CLKOUT Low	0		ns	
T <sub>AVDV</sub>	Address Valid to Input Data Valid		3 T <sub>OSC</sub> - 55	ns	(Note 2)
T <sub>RLDV</sub>	$\overline{RD}$ Active to Input Data Valid		T <sub>OSC</sub> - 22	ns	(Note 2)
T <sub>CLDV</sub>	CLKOUT Low to Input Data Valid		T <sub>OSC</sub> - 45	ns	
T <sub>RHDZ</sub>	End of $\overline{RD}$ to Input Data Float		T <sub>OSC</sub>	ns	
T <sub>RXDX</sub>	Data Hold after $\overline{RD}$ Inactive	0		ns	

**NOTES:**

1. If max is exceeded, additional wait states will occur.
2. If wait states are used, add 2 T<sub>OSC</sub> \* N, where N = number of wait states.



**AC CHARACTERISTICS** (Continued)

For use over specified operating conditions.

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, F<sub>OSC</sub> = 16/20 MHz

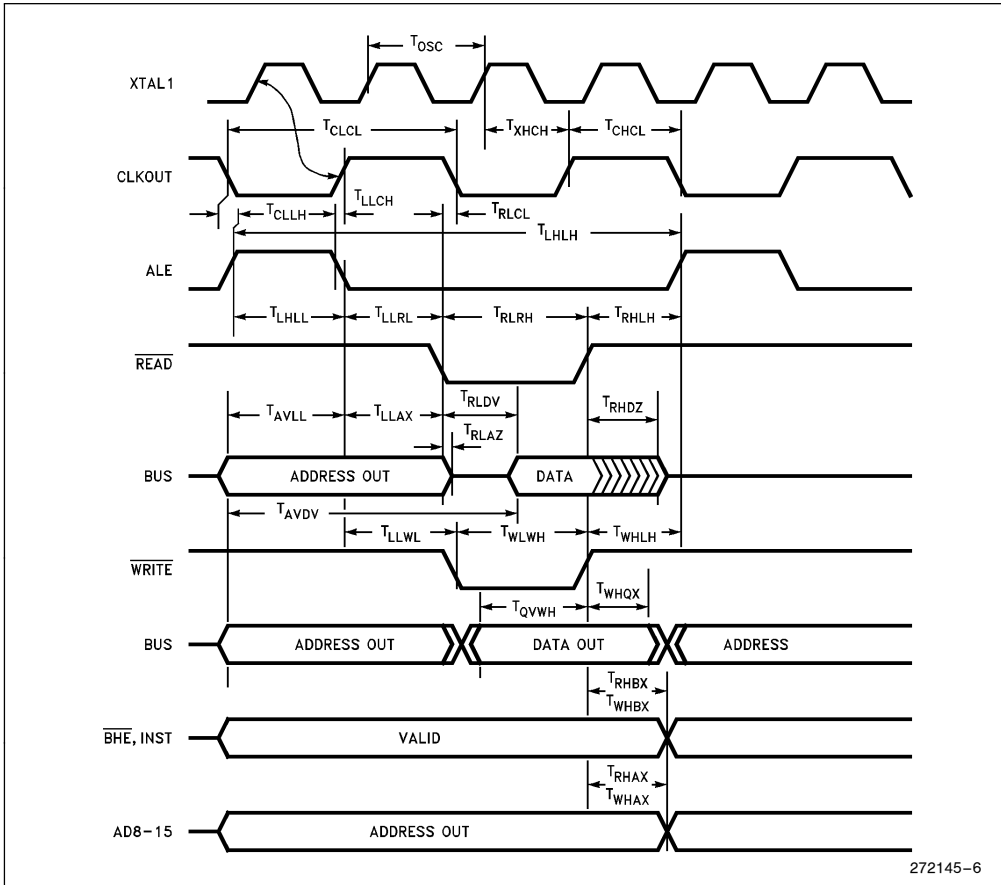
The 80C196KD will meet these specifications:

Symbol	Description	Min	Max	Units	Notes
F <sub>XTAL</sub>	Frequency on XTAL1 (8XC196KD)	8	16	MHz	(Note 1)
F <sub>XTAL</sub>	Frequency on XTAL1 (8XC196KD20)	8	20	MHz	(Note 1)
T <sub>OSC</sub>	1/F <sub>XTAL</sub> (8XC196KD)	62.5	125	ns	
T <sub>OSC</sub>	1/F <sub>XTAL</sub> (8XC196KD20)	50	125	ns	
T <sub>XHCH</sub>	XTAL1 High to CLKOUT High or Low	+ 20	+ 110	ns	
T <sub>CLCL</sub>	CLKOUT Cycle Time	2 T <sub>OSC</sub>		ns	
T <sub>CHCL</sub>	CLKOUT High Period	T <sub>OSC</sub> - 10	T <sub>OSC</sub> + 15	ns	
T <sub>CLLH</sub>	CLKOUT Falling Edge to ALE Rising	- 5	+ 15	ns	
T <sub>LLCH</sub>	ALE Falling Edge to CLKOUT Rising	- 20	+ 15	ns	
T <sub>LHLH</sub>	ALE Cycle Time	4 T <sub>OSC</sub>		ns	(Note 4)
T <sub>LHLL</sub>	ALE High Period	T <sub>OSC</sub> - 10	T <sub>OSC</sub> + 10	ns	
T <sub>AVLL</sub>	Address Setup to ALE Falling Edge	T <sub>OSC</sub> - 15			
T <sub>LLAX</sub>	Address Hold after ALE Falling Edge	T <sub>OSC</sub> - 35		ns	
T <sub>LLRL</sub>	ALE Falling Edge to $\overline{RD}$ Falling Edge	T <sub>OSC</sub> - 30		ns	
T <sub>RLCL</sub>	$\overline{RD}$ Low to CLKOUT Falling Edge	+ 4	+ 30	ns	
T <sub>RLRH</sub>	$\overline{RD}$ Low Period	T <sub>OSC</sub> - 5		ns	(Note 4)
T <sub>RHLH</sub>	$\overline{RD}$ Rising Edge to ALE Rising Edge	T <sub>OSC</sub>	T <sub>OSC</sub> + 25	ns	(Note 2)
T <sub>RLAZ</sub>	$\overline{RD}$ Low to Address Float		+ 5	ns	
T <sub>LLWL</sub>	ALE Falling Edge to $\overline{WR}$ Falling Edge	T <sub>OSC</sub> - 10		ns	
T <sub>CLWL</sub>	CLKOUT Low to $\overline{WR}$ Falling Edge	0	+ 25	ns	
T <sub>QVWH</sub>	Data Stable to $\overline{WR}$ Rising Edge	T <sub>OSC</sub> - 23			(Note 4)
T <sub>CHWH</sub>	CLKOUT High to $\overline{WR}$ Rising Edge	- 5	+ 15	ns	
T <sub>WLWH</sub>	$\overline{WR}$ Low Period	T <sub>OSC</sub> - 20		ns	(Note 4)
T <sub>WHQX</sub>	Data Hold after $\overline{WR}$ Rising Edge	T <sub>OSC</sub> - 25		ns	
T <sub>WHLH</sub>	$\overline{WR}$ Rising Edge to ALE Rising Edge	T <sub>OSC</sub> - 10	T <sub>OSC</sub> + 15	ns	(Note 2)
T <sub>WHBX</sub>	$\overline{BHE}$ , INST after $\overline{WR}$ Rising Edge	T <sub>OSC</sub> - 10		ns	
T <sub>WHAX</sub>	AD8-15 HOLD after $\overline{WR}$ Rising	T <sub>OSC</sub> - 30		ns	(Note 3)
T <sub>RHBX</sub>	$\overline{BHE}$ , INST after $\overline{RD}$ Rising Edge	T <sub>OSC</sub> - 10		ns	
T <sub>RHAX</sub>	AD8-15 HOLD after $\overline{RD}$ Rising	T <sub>OSC</sub> - 25		ns	(Note 3)

**NOTES:**

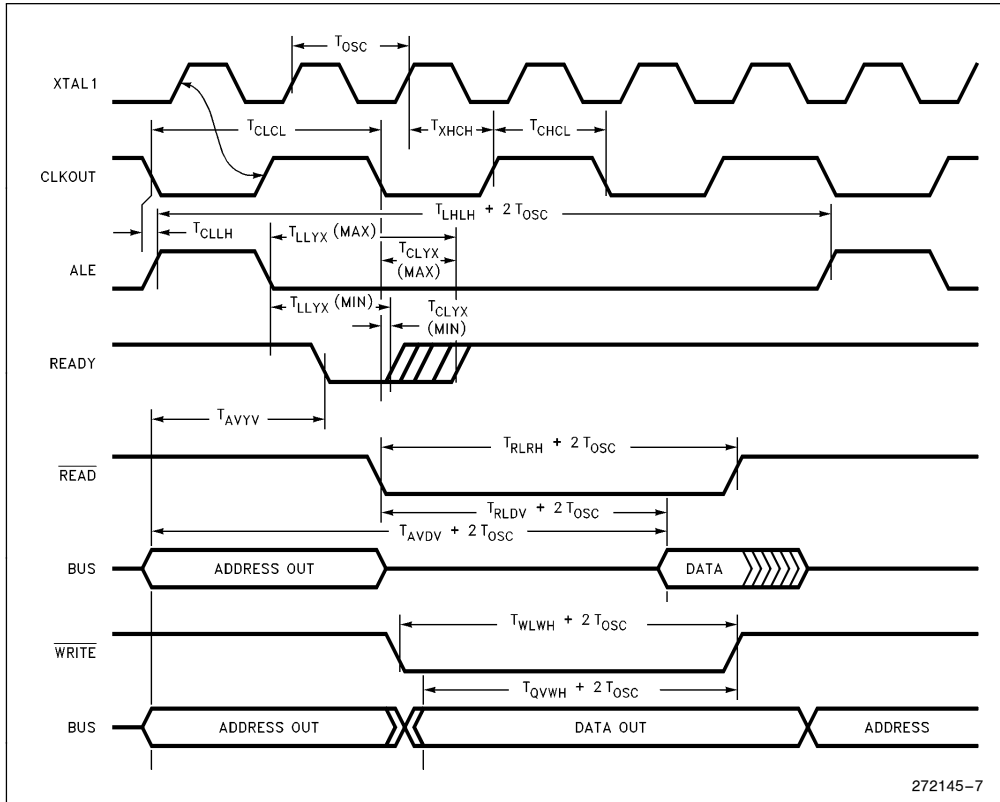
1. Testing performed at 8 MHz. However, the device is static by design and will typically operate below 1 Hz.
2. Assuming back-to-back bus cycles.
3. 8-Bit bus only.
4. If wait states are used, add 2 T<sub>OSC</sub> \* N, where N = number of wait states.

**System Bus Timings**

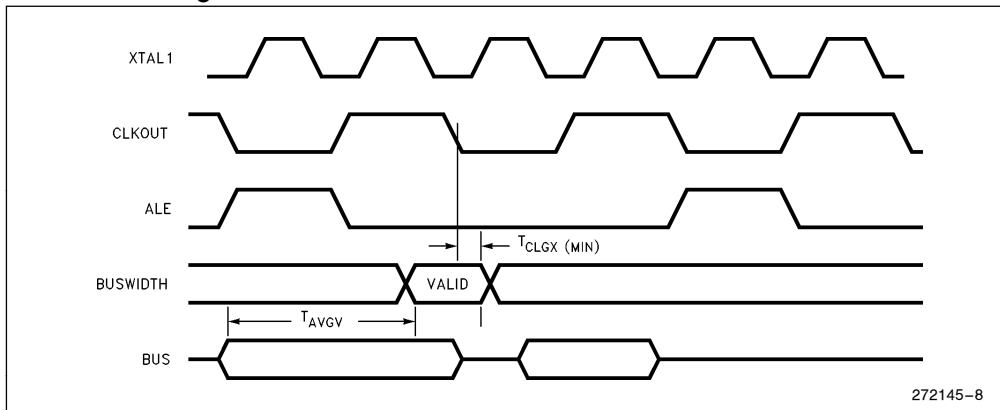


272145-6

**READY Timings (One Wait State)**



**Buswidth Timings**



**HOLD/HLDA TIMINGS**

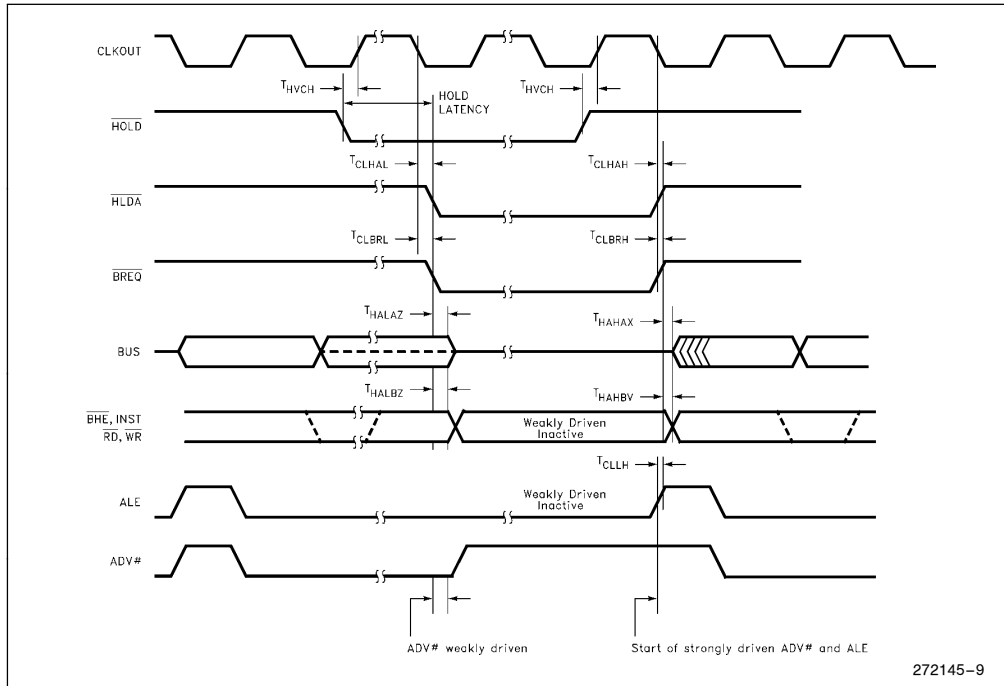
Symbol	Description	Min	Max	Units	Notes
$T_{HVCH}$	HOLD Setup	+ 55		ns	(Note 1)
$T_{CLHAL}$	CLKOUT Low to $\overline{HLDA}$ Low	- 15	+ 15	ns	
$T_{CLBRL}$	CLKOUT Low to $\overline{BREQ}$ Low	- 15	+ 15	ns	
$T_{HALAZ}$	$\overline{HLDA}$ Low to Address Float		+ 15	ns	
$T_{HALBZ}$	$\overline{HLDA}$ Low to $\overline{BHE}$ , $\overline{INST}$ , $\overline{RD}$ , $\overline{WR}$ Weakly Driven		+ 20	ns	
$T_{CLHAH}$	CLKOUT Low to $\overline{HLDA}$ High	- 15	+ 15	ns	
$T_{CLBRH}$	CLKOUT Low to $\overline{BREQ}$ High	- 15	+ 15	ns	
$T_{HAHAX}$	$\overline{HLDA}$ High to Address No Longer Float	- 15		ns	
$T_{HAHBV}$	$\overline{HLDA}$ High to $\overline{BHE}$ , $\overline{INST}$ , $\overline{RD}$ , $\overline{WR}$ Valid	- 10	+ 15	ns	
$T_{CLLH}$	CLKOUT Low to ALE High	- 5	+ 15	ns	

**NOTE:**

1. To guarantee recognition at next clock.

**DC SPECIFICATIONS IN HOLD**

Description	Min	Max	Units
Weak Pullups on $\overline{ADV}$ , $\overline{RD}$ , $\overline{WR}$ , $\overline{WRL}$ , $\overline{BHE}$	50K	250K	$V_{CC} = 5.5V, V_{IN} = 0.45V$
Weak Pulldowns on ALE, $\overline{INST}$	10K	50K	$V_{CC} = 5.5V, V_{IN} = 2.4$





**MAXIMUM HOLD LATENCY**

Bus Cycle Type	
Internal Execution	1.5 States
16-Bit External Execution	2.5 States
8-Bit External Execution	4.5 States

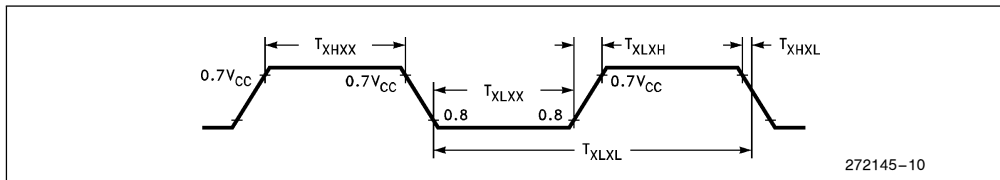
**EXTERNAL CLOCK DRIVE (8XC196KD)**

Symbol	Parameter	Min	Max	Units
1/T <sub>XLXL</sub>	Oscillator Frequency	8	16.0	MHz
T <sub>XLXL</sub>	Oscillator Period	62.5	125	ns
T <sub>XHXX</sub>	High Time	20		ns
T <sub>XLXX</sub>	Low Time	20		ns
T <sub>XLXH</sub>	Rise Time		10	ns
T <sub>XHXL</sub>	Fall Time		10	ns

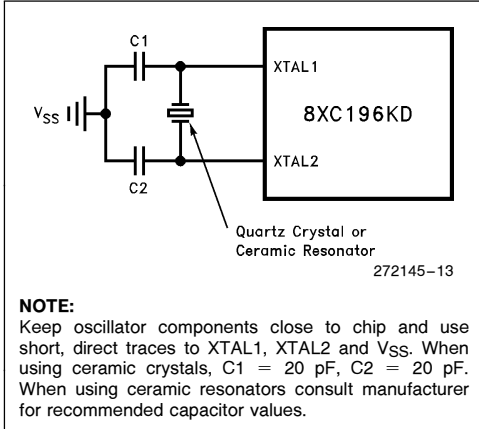
**EXTERNAL CLOCK DRIVE (8XC196KD20)**

Symbol	Parameter	Min	Max	Units
1/T <sub>XLXL</sub>	Oscillator Frequency	8	20.0	MHz
T <sub>XLXL</sub>	Oscillator Period	50	125	ns
T <sub>XHXX</sub>	High Time	17		ns
T <sub>XLXX</sub>	Low Time	17		ns
T <sub>XLXH</sub>	Rise Time		8	ns
T <sub>XHXL</sub>	Fall Time		8	ns

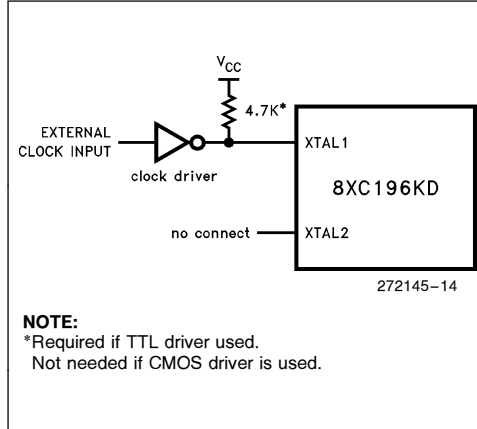
**EXTERNAL CLOCK DRIVE WAVEFORMS**



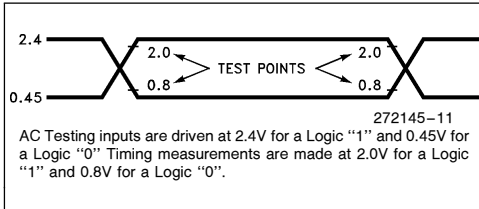
**EXTERNAL CRYSTAL CONNECTIONS**



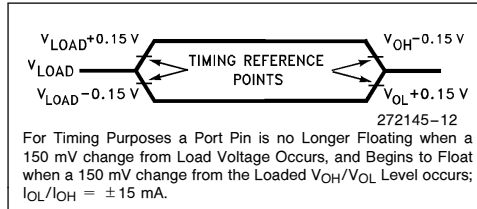
**EXTERNAL CLOCK CONNECTIONS**



**AC TESTING INPUT, OUTPUT WAVEFORMS**



**FLOAT WAVEFORMS**



**EXPLANATION OF AC SYMBOLS**

Each symbol is two pairs of letters prefixed by "T" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

**Conditions:**

- H— High
- L— Low
- V— Valid
- X— No Longer Valid
- Z— Floating

**Signals:**

- A— Address
- B— BHE
- C— CLKOUT
- D— DATA
- G— Buswidth
- H— HOLD
- HA— HLDA
- L— ALE/ $\overline{ADV}$
- BR—  $\overline{BREQ}$
- R—  $\overline{RD}$
- W—  $\overline{WR}/\overline{WRH}/\overline{WRL}$
- X— XTAL1
- Y— READY
- Q— Data Out

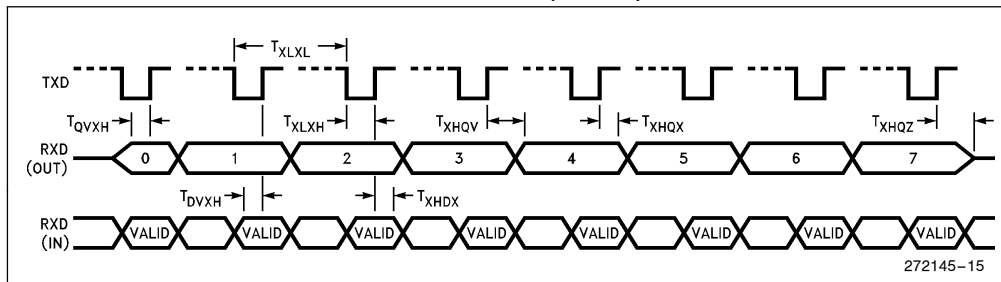
**AC CHARACTERISTICS—SERIAL PORT—SHIFT REGISTER MODE**

**SERIAL PORT TIMING—SHIFT REGISTER MODE (MODE 0)**

Symbol	Parameter	Min	Max	Units
$T_{XLXL}$	Serial Port Clock Period (BRR $\geq$ 8002H)	$6 T_{OSC}$		ns
$T_{XLXH}$	Serial Port Clock Falling Edge to Rising Edge (BRR $\geq$ 8002H)	$4 T_{OSC} - 50$	$4 T_{OSC} + 50$	ns
$T_{XLXL}$	Serial Port Clock Period (BRR = 8001H)	$4 T_{OSC}$		ns
$T_{XLXH}$	Serial Port Clock Falling Edge to Rising Edge (BRR = 8001H)	$2 T_{OSC} - 50$	$2 T_{OSC} + 50$	ns
$T_{QVXH}$	Output Data Valid to Clock Rising Edge	$2 T_{OSC} - 50$		ns
$T_{XHQX}$	Output Data Hold after Clock Rising Edge	$2 T_{OSC} - 50$		ns
$T_{XHQV}$	Next Output Data Valid after Clock Rising Edge		$2 T_{OSC} + 50$	ns
$T_{DVXH}$	Input Data Setup to Clock Rising Edge	$T_{OSC} + 50$		ns
$T_{XHDX}$	Input Data Hold after Clock Rising Edge	0		ns
$T_{XHQZ}$	Last Clock Rising to Output Float		$1 T_{OSC}$	ns

**WAVEFORM—SERIAL PORT—SHIFT REGISTER MODE**

**SERIAL PORT WAVEFORM—SHIFT REGISTER MODE (MODE 0)**



## A to D CHARACTERISTICS

The A/D converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of  $V_{REF}$ .

### 10-BIT MODE A/D OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
$T_A$	Ambient Temperature <b>Commercial</b> Temp.	0	+ 70	°C
$V_{CC}$	Digital Supply Voltage	4.50	5.50	V
$V_{REF}$	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	$V_{SS} - 0.40$	$V_{CC} + 0.40$	V
$T_{SAM}$	Sample Time	1.0		$\mu s^{(1)}$
$T_{CONV}$	Conversion Time	10	20	$\mu s^{(1)}$
$F_{OSC}$	Oscillator Frequency ( <b>8XC196KD</b> )	8.0	16.0	MHz
$F_{OSC}$	Oscillator Frequency ( <b>8XC196KD20</b> )	8.0	20.0	MHz

**NOTE:**

- The value of AD\_TIME is selected to meet these specifications.

### 10-BIT MODE A/D CHARACTERISTICS (Over Specified Operating Conditions)

Parameter	Typical <sup>(1)</sup>	Minimum	Maximum	Units*	Notes
Resolution		1024 10	1024 10	Levels Bits	
Absolute Error		0	$\pm 3$	LSBs	
Full Scale Error	$0.25 \pm 0.5$			LSBs	
Zero Offset Error	$0.25 \pm 0.5$			LSBs	
Non-Linearity	$1.0 \pm 2.0$	0	$\pm 3$	LSBs	
Differential Non-Linearity Error		$> -1$	+ 2	LSBs	
Channel-to-Channel Matching	$\pm 0.1$	0	$\pm 1$	LSBs	
Repeatability	$\pm 0.25$			LSBs	
Temperature Coefficients:					
Offset	0.009			LSB/°C	
Full Scale	0.009			LSB/°C	
Differential Non-Linearity	0.009			LSB/°C	
Off Isolation		- 60		dB	2, 3
Feedthrough	- 60			dB	2
$V_{CC}$ Power Supply Rejection	- 60			dB	2
Input Series Resistance		750	1.2K	$\Omega$	4
Voltage on Analog Input Pin		ANGND - 0.5	$V_{REF} + 0.5$	V	5, 6
DC Input Leakage		0	$\pm 3.0$	$\mu A$	
Sampling Capacitor	3			pF	

**NOTES:**

\*An "LSB" as used here has a value of approximately 5 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms.)

- These values are expected for most parts at 25°C but are not tested or guaranteed.
- DC to 100 KHz.
- Multiplexer Break-Before-Make is guaranteed.
- Resistance from device pin, through internal MUX, to sample capacitor.
- These values may be exceeded if the pin current is limited to  $\pm 2$  mA.
- Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
- All conversions performed with processor in IDLE mode.

**8-BIT MODE A/D OPERATING CONDITIONS**

Symbol	Description	Min	Max	Units
T <sub>A</sub>	Ambient Temperature <b>Commercial</b> Temp.	0	+70	°C
V <sub>CC</sub>	Digital Supply Voltage	4.50	5.50	V
V <sub>REF</sub>	Analog Supply Voltage	4.00	5.50	V
ANGND	Analog Ground Voltage	V <sub>SS</sub> - 0.40	V <sub>SS</sub> + 0.40	V
T <sub>SAM</sub>	Sample Time	1.0		μs <sup>(1)</sup>
T <sub>CONV</sub>	Conversion Time	7	20	μs <sup>(1)</sup>
F <sub>OSC</sub>	Oscillator Frequency ( <b>8XC196KD</b> )	8.0	16.0	MHz
F <sub>OSC</sub>	Oscillator Frequency ( <b>8XC196KD20</b> )	8.0	20.0	MHz

**NOTE:**

- The value of AD\_TIME is selected to meet these specifications.

**8-BIT MODE A/D CHARACTERISTICS** (Over Specified Operating Conditions)

Parameter	Typical <sup>(1)</sup>	Minimum	Maximum	Units*	Notes
Resolution		256 8	256 8	Levels Bits	
Absolute Error		0	±1	LSBs	
Full Scale Error	±0.5			LSBs	
Zero Offset Error	±0.5			LSBs	
Non-Linearity		0	±1	LSBs	
Differential Non-Linearity Error		> -1	+1	LSBs	
Channel-to-Channel Matching			±1	LSBs	
Repeatability	±0.25			LSBs	
Temperature Coefficients: Offset Full Scale Differential Non-Linearity	0.003 0.003 0.003			LSB/°C LSB/°C LSB/°C	
Off Isolation		-60		dB	2, 3
Feedthrough	-60			dB	2
V <sub>CC</sub> Power Supply Rejection	-60			dB	2
Input Series Resistance		750	1.2K	Ω	4
Voltage on Analog Input Pin		V <sub>SS</sub> - 0.5	V <sub>REF</sub> + 0.5	V	5, 6
DC Input Leakage		0	±3.0	μA	
Sampling Capacitor	3			pF	

**NOTES:**

\*An "LSB" as used here has a value of approximately 20 mV. (See Embedded Microcontrollers and Processors Handbook for A/D glossary of terms).

- These values are expected for most parts at 25°C but are not tested or guaranteed.
- DC to 100 KHz.
- Multiplexer Break-Before-Make is guaranteed.
- Resistance from device pin, through internal MUX, to sample capacitor.
- These values may be exceeded if pin current is limited to ±2 mA.
- Applying voltages beyond these specifications will degrade the accuracy of other channels being converted.
- All conversions performed with processor in IDLE mode.

## OTPROM SPECIFICATIONS

### OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
T <sub>A</sub>	Ambient Temperature During Programming	20	30	C
V <sub>CC</sub>	Supply Voltage During Programming	4.5	5.5	V <sup>(1)</sup>
V <sub>REF</sub>	Reference Supply Voltage During Programming	4.5	5.5	V <sup>(1)</sup>
V <sub>PP</sub>	Programming Voltage	12.25	12.75	V <sup>(2)</sup>
V <sub>EA</sub>	EA Pin Voltage	12.25	12.75	V <sup>(2)</sup>
F <sub>OSC</sub>	Oscillator Frequency during Auto and Slave Mode Programming	6.0	8.0	MHz
F <sub>OSC</sub>	Oscillator Frequency during Run-Time Programming (8XC196KD)	6.0	16.0	MHz
F <sub>OSC</sub>	Oscillator Frequency during Run-Time Programming (8XC196KD20)	6.0	20.0	MHz

#### NOTES:

- V<sub>CC</sub> and V<sub>REF</sub> should nominally be at the same voltage during programming.
- V<sub>PP</sub> and V<sub>EA</sub> must never exceed the maximum specification, or the device may be damaged.
- V<sub>SS</sub> and ANGND should nominally be at the same potential (0V).
- Load capacitance during Auto and Slave Mode programming = 150 pF.

### AC OTPROM PROGRAMMING CHARACTERISTICS (SLAVE MODE)

Symbol	Description	Min	Max	Units
T <sub>SHLL</sub>	Reset High to First $\overline{\text{PALE}}$ Low	1100		T <sub>OSC</sub>
T <sub>LLLH</sub>	$\overline{\text{PALE}}$ Pulse Width	50		T <sub>OSC</sub>
T <sub>AVLL</sub>	Address Setup Time	0		T <sub>OSC</sub>
T <sub>LLAX</sub>	Address Hold Time	100		T <sub>OSC</sub>
T <sub>PLDV</sub>	$\overline{\text{PROG}}$ Low to Word Dump Valid		50	T <sub>OSC</sub>
T <sub>PHDX</sub>	Word Dump Data Hold		50	T <sub>OSC</sub>
T <sub>DVPL</sub>	Data Setup Time	0		T <sub>OSC</sub>
T <sub>PLDX</sub>	Data Hold Time	400		T <sub>OSC</sub>
T <sub>PLPH</sub> <sup>(1)</sup>	$\overline{\text{PROG}}$ Pulse Width	50		T <sub>OSC</sub>
T <sub>PHLL</sub>	$\overline{\text{PROG}}$ High to Next $\overline{\text{PALE}}$ Low	220		T <sub>OSC</sub>
T <sub>LHPL</sub>	$\overline{\text{PALE}}$ High to $\overline{\text{PROG}}$ Low	220		T <sub>OSC</sub>
T <sub>PHPL</sub>	$\overline{\text{PROG}}$ High to Next $\overline{\text{PROG}}$ Low	220		T <sub>OSC</sub>
T <sub>PHIL</sub>	$\overline{\text{PROG}}$ High to AINC Low	0		T <sub>OSC</sub>
T <sub>ILIH</sub>	$\overline{\text{AINC}}$ Pulse Width	240		T <sub>OSC</sub>
T <sub>ILVH</sub>	PVER Hold after $\overline{\text{AINC}}$ Low	50		T <sub>OSC</sub>
T <sub>ILPL</sub>	$\overline{\text{AINC}}$ Low to $\overline{\text{PROG}}$ Low	170		T <sub>OSC</sub>
T <sub>PHVL</sub>	$\overline{\text{PROG}}$ High to PVER Valid		220	T <sub>OSC</sub>

#### NOTE:

- This specification is for the Word Dump Mode. For programming pulses, use the Modified Quick Pulse Algorithm.

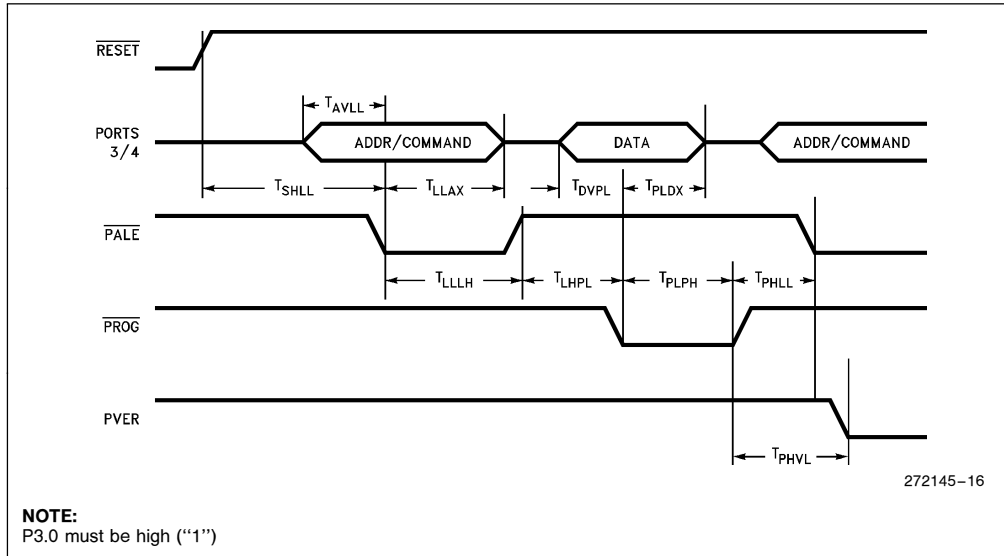
**DC OTPROM PROGRAMMING CHARACTERISTICS**

Symbol	Description	Min	Max	Units
$I_{PP}$	$V_{PP}$ Supply Current (When Programming)		100	mA

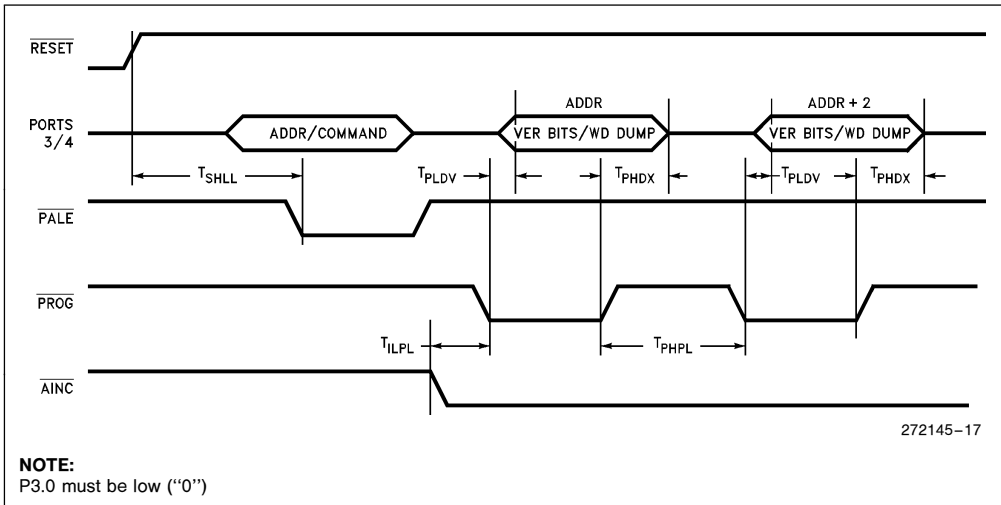
**NOTE:**  
Do not apply  $V_{PP}$  until  $V_{CC}$  is stable and within specifications and the oscillator/clock has stabilized or the device may be damaged.

**OTPROM PROGRAMMING WAVEFORMS**

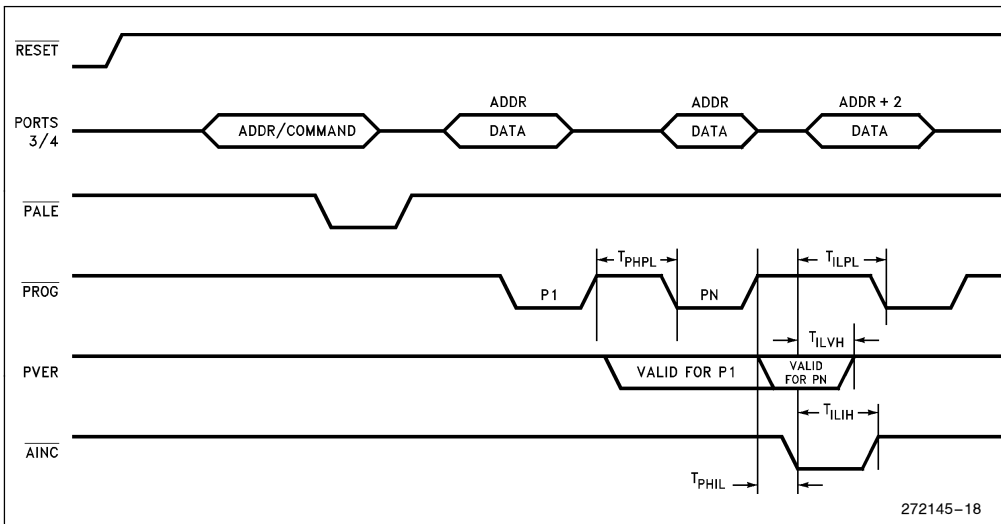
**SLAVE PROGRAMMING MODE DATA PROGRAM MODE WITH SINGLE PROGRAM PULSE**



**SLAVE PROGRAMMING MODE IN WORD DUMP WITH AUTO INCREMENT**



**SLAVE PROGRAMMING MODE TIMING IN DATA PROGRAM WITH REPEATED PROG PULSE AND AUTO INCREMENT**





**8XC196KC TO 8XC196KD DESIGN CONSIDERATIONS**

1. Memory Map. The 8XC196KD has 1024 bytes of RAM/SFRs and 32K of OTPROM. The extra 512 bytes of RAM reside in locations 0200H to 03FFH, and the extra 16 Kbytes of OTPROM reside in locations 6000H to 9FFFH. On the 87C196KC these locations are always external, so KC code may have to be modified to run on the KD.
2. The vertical window scheme has been extended to include all on-chip RAM.
3. IOC3.1 controls the CLKOUT signal. This bit must be 0 to enable CLKOUT.
4. The 87C196KD has a different autoprogramming algorithm to support 32K of on-chip OTPROM.

**8XC196KD ERRATA**

1. 83C196KD can possibly miss interrupts on P0.7. See techbit MC0893.

**DATA SHEET REVISION HISTORY**

This data sheet is valid for devices with a “D” and “E” at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following are important differences between the 272145-002 and 272145-003 data sheets:

1.  $I_{IL1}$  specification (logic 0 input current in reset) was misnamed. It is renamed  $I_{IL2}$ .
2.  $T_{LLYV}$  and  $T_{LLGV}$  were removed. These specifications are not necessary for high-speed system designs.
3. An errata with 83C196KD P0.7 EXTINT was added to the errata section.

The following are important differences between the 272145-001 and 272145-002 data sheets:

1. Added 20 MHz specifications.
2. Added 80-lead SQFP package pinout.

3. Changed QFP Package  $\theta_{JA}$  to 56°C/W from 42°C/W.
4. Changed  $V_{HYS}$  to 300 mV from 150 mV.
5. Changed  $I_{CC}$  Typical specification at 16 MHz to 65 mA from 50 mA.
6. Changed  $I_{CC}$  Maximum specification at 16 MHz to 75 mA from 70 mA.
7. Changed  $I_{IDLE}$  Typical specification to 17 mA from 15 mA.
8. Changed  $I_{IDLE}$  Maximum specification to 25 mA from 30 mA.
9. Changed  $I_{PD}$  Typical specification to 8  $\mu$ A from 15  $\mu$ A.
10. Added  $I_{PD}$  Maximum specification.
11. Changed  $T_{CLDV}$  Maximum specification to  $T_{OSC} - 45$  from  $T_{OSC} - 50$ .
12. Changed  $T_{LLAX}$  Minimum specification to  $T_{OSC} - 35$  from  $T_{OSC} - 40$ .
13. Changed  $T_{CHWH}$  Minimum specification to  $-5$  from  $-10$ .
14. Changed  $T_{RHAX}$  Minimum specification to  $T_{OSC} - 25$  from  $T_{OSC} - 30$ .
15. Changed  $T_{HALAZ}$  Maximum specification to  $+15$  from  $+10$ .
16. Changed  $T_{HALBZ}$  Maximum specification to  $+20$  from  $+15$ .
17. Added  $T_{HAHBV}$  Maximum specification.
18. Changed  $T_{SAM}$  for 10-bit mode to 1  $\mu$ s from 3  $\mu$ s.
19. Changed  $T_{SAM}$  for 8-bit mode to 1  $\mu$ s from 2  $\mu$ s.
20. Changed  $I_{IH1}$  test condition to  $V_{IN} = 2.4V$  from 5.5V.
21. Changed  $I_{IH1}$  maximum specification to  $+200 \mu$ A from  $+100 \mu$ A.
22. Removed NMI from list of standard inputs.
23. Updated  $I_{CC}$  and  $I_{IDLE}$  vs frequency graph.
24. Updated note under DC EPROM Programming Characteristics.
25. Changed  $I_{LL1}$  maximum specification to  $-12$  mA from  $-6$  mA.