



PRELIMINARY

# SMART 3 ADVANCED BOOT BLOCK BYTE-WIDE 8-MBIT (1024K x 8), 16-MBIT (2056K x 8) FLASH MEMORY FAMILY

*28F008B3, 28F016B3*

- **Flexible SmartVoltage Technology**
  - 2.7V–3.6V Program/Erase
  - 2.7V–3.6V Read Operation
  - 12V V<sub>PP</sub> Fast Production Programming
- **2.7V or 1.8V I/O Option**
  - Reduces Overall System Power
- **Optimized Block Sizes**
  - Eight 8-Kbyte Blocks for Data, Top or Bottom Locations
  - Up to Thirty-One 64-Kbyte Blocks for Code
- **High Performance**
  - 2.7V–3.6V: 120 ns Max Access Time
- **Block Locking**
  - V<sub>CC</sub>-Level Control through WP#
- **Low Power Consumption**
  - 20 mA Maximum Read Current
- **Absolute Hardware-Protection**
  - V<sub>PP</sub> = GND Option
  - V<sub>CC</sub> Lockout Voltage
- **Extended Temperature Operation**
  - -40°C to +85°C
- **Supports Code plus Data Storage**
  - Optimized for FDI, Flash Data Integrator Software
  - Fast Program Suspend Capability
  - Fast Erase Suspend Capability
- **Extended Cycling Capability**
  - 10,000 Block Erase Cycles
- **Automated Byte Program and Block Erase**
  - Command User Interface
  - Status Registers
- **SRAM-Compatible Write Interface**
- **Automatic Power Savings Feature**
- **Reset/Deep Power-Down**
  - 1  $\mu$ A I<sub>CC</sub> Typical
  - Spurious Write Lockout
- **Standard Surface Mount Packaging**
  - 48-Ball  $\mu$ BGA\* Package
  - 40-Lead TSOP Package
- **Footprint Upgradeable**
  - Upgradeable from 2-, 4- and 8-Mbit Boot Block
- **ETOX™ V (0.4  $\mu$ ) Flash Technology**
- **x8-Only Input/Output Architecture**
  - For Space-Constrained 8-bit Applications

The new Smart 3 Advanced Boot Block, manufactured on Intel's latest 0.4 $\mu$  technology, represents a feature-rich solution at overall lower system cost. Smart 3 flash memory devices incorporate low voltage capability (2.7V read, program and erase) with high-speed, low-power operation. Several new features have been added, including the ability to drive the I/O at 1.8V, which significantly reduces system active power and interfaces to 1.8V controllers. A new blocking scheme enables code and data storage within a single device. Add to this the Intel-developed Flash Data Integrator (FDI) software and you have the most cost-effective, monolithic code plus data storage solution on the market today. Smart 3 Advanced Boot Block Byte-Wide products will be available in 40-lead TSOP and 48-ball  $\mu$ BGA\* packages. Additional information on this product family can be obtained by accessing Intel's WWW page: <http://www.intel.com/design/flcomp>

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**REVISION HISTORY**

Number	Description
-001	Original version



1.0 INTRODUCTION

This preliminary datasheet contains the specifications for the Advanced Boot Block flash memory family, which is optimized for low power, portable systems. This family of products features 1.8V–2.2V or 2.7V–3.6V I/Os and a low VCC/VPP operating range of 2.7V–3.6V for read and program/erase operations. In addition this family is capable of fast programming at 12V. Throughout this document, the term “2.7V” refers to the full voltage range 2.7V–3.6V (except where noted otherwise) and “VPP = 12V” refers to 12V ±5%. Section 1 and 2 provides an overview of the flash memory family including applications, pinouts and pin descriptions. Section 3 describes the memory organization and operation for these products. Finally, Sections 4, 5, 6 and 7 contain the operating specifications.

1.1 Smart 3 Advanced Boot Block Flash Memory Enhancements

The new 8-Mbit and 16-Mbit Smart 3 Advanced Boot Block flash memory provides a convenient upgrade from and/or compatibility to previous 4-Mbit and 8-Mbit Boot Block products. The Smart 3 product functions are similar to lower density products in both command sets and operation, providing similar pinouts to ease density upgrades.

The Smart 3 Advanced Boot Block flash memory features

- Enhanced blocking for easy segmentation of code and data or additional design flexibility
- Program Suspend command which permits program suspend to read
- WP# pin to lock and unlock the upper two (or lower two, depending on location) 8-Kbyte blocks
- VCCQ input for 1.8V–2.2V on all I/Os. See Figures 1–3 for pinout diagrams and VCCQ location
- Maximum program time specification for improved data storage.

Table 1. Smart 3 Advanced Boot Block Feature Summary

Feature	28F016B3/28F008B3/28F004B3	Reference
VCC Read Voltage	2.7V– 3.6V	Table 9, Table 12
VCCQ I/O Voltage	1.8V–2.2V or 2.7V– 3.6V	Table 9, Table 12
VPP Program/Erase Voltage	2.7V– 3.6V or 11.4V– 12.6V	Table 9, Table 12
Bus Width	8 bits	Table 2
Speed	120 ns	Table 15
Memory Arrangement	1 Mbit x 8 (8 Mbit), 2 Mbit x 8 (16 Mbit)	
Blocking (top or bottom)	Eight 8-Kbyte parameter blocks (8/16 Mbit) & Fifteen 64-Kbyte blocks (8 Mbit) Thirty-one 64-Kbyte main blocks (16 Mbit)	Section 2.2 Figures 4 and 5
Locking	WP# locks/unlocks parameter blocks All other blocks protected using VPP switch	Section 3.3 Table 8
Operating Temperature	Extended: –40°C to +85°C	Table 9, Table 12
Program/Erase Cycling	10,000 cycles	Table 9, Table 12
Packages	40-Lead TSOP, 48-Ball μBGA* CSP	Figures 1, 2, and 3

## 1.2 Product Overview

Intel provides the most flexible voltage solution in the flash industry, providing three discrete voltage supply pins:  $V_{CC}$  for read operation,  $V_{CCQ}$  for output swing, and  $V_{PP}$  for program and erase operation. Discrete supply pins allow system designers to use the optimal voltage levels for their design. All Smart 3 Advanced Boot Block flash memory products provide program/erase capability at 2.7V or 12V and read with  $V_{CC}$  at 2.7V. Since many designs read from the flash memory a large percentage of the time, 2.7V  $V_{CC}$  operation can provide substantial power savings. The 12V  $V_{PP}$  option maximizes program and erase performance during production programming.

The Smart 3 Advanced Boot Block flash memory products are high-performance devices with low power operation. The available densities for the byte-wide devices (x8) are

- a. 8-Mbit (8,388,608-bit) flash memory organized as 1 Mbyte of 8 bits each
- b. 16-Mbit (16,777,216-bit) flash memory organized as 2 Mbytes of 8 bits each.

For word-wide devices (x16) see the *Smart 3 Advanced Boot Block Word-Wide Flash Memory Family* datasheet.

The parameter blocks are located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map in order to accommodate different microprocessor protocols for kernel code location. The upper two (or lower two) parameter blocks can be locked to provide complete code security for system initialization code. Locking and unlocking is controlled by WP# (see Section 3.3 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the flash memory. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verification, thereby unburdening the microprocessor or microcontroller. The status register indicates the status of the WSM by signifying block erase or byte program completion and status.

Program and erase automation allows program and erase operations to be executed using an industry-standard two-write command sequence to the CUI. Data writes are performed in byte increments. Each byte in the flash memory can be programmed independently of other memory locations; every erase operation erases all locations within a block simultaneously. Program suspend allows system software to suspend the program command in order to read from any other block. Erase suspend allows system software to suspend the block erase command in order to read from or program data to any other block.

The Smart 3 Advanced Boot Block flash memory is also designed with an Automatic Power Savings (APS) feature which minimizes system current drain, allowing for very low power designs. This mode is entered immediately following the completion of a read cycle.

When the CE# and RP# pins are at  $V_{CC}$ , the  $I_{CC}$  CMOS standby mode is enabled. A deep power-down mode is enabled when the RP# pin is at GND, minimizing power consumption and providing write protection.  $I_{CC}$  current in deep power-down is 1  $\mu$ A typical (2.7V  $V_{CC}$ ). A minimum reset time of  $t_{RHQV}$  is required from RP# switching high until outputs are valid to read attempts. With RP# at GND, the WSM is reset and Status Register is cleared. Section 3.5 contains additional information on using the deep power-down feature, along with other power consumption issues.

The RP# pin provides additional protection against unwanted command writes that may occur during system reset and power-up/down sequences due to invalid system bus conditions (see Section 3.6).

Refer to the DC Characteristics Table, Sections 5.1 and 6.1, for complete current and voltage specifications. Refer to the AC Characteristics Table, Section 7.0, for read, program and erase performance specifications.

## 2.0 PRODUCT DESCRIPTION

This section explains device pin description and package pinouts.

### 2.1 Package Pinouts

The Smart 3 Advanced Boot Block flash memory is available in 40-lead TSOP (see Figure 1) and 48-ball  $\mu$ BGA packages (see Figures 2 and 3). In Figure 1, pin changes from one density to the next are circled. Both packages, 40-lead TSOP and 48-ball  $\mu$ BGA package, are 8-bits wide and fully upgradeable across product densities (from 8 Mb to 16 Mb).

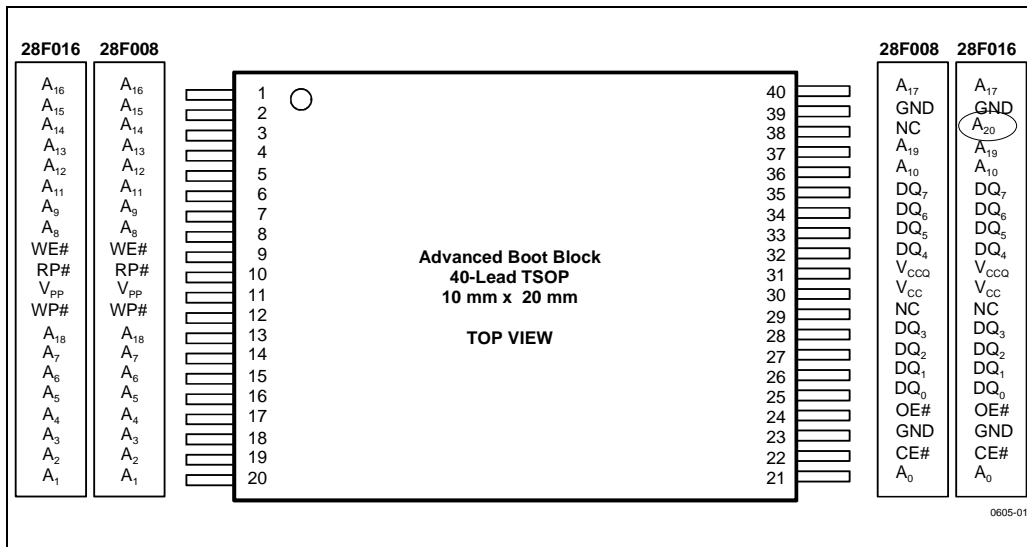


Figure 1. 40-Lead TSOP Package

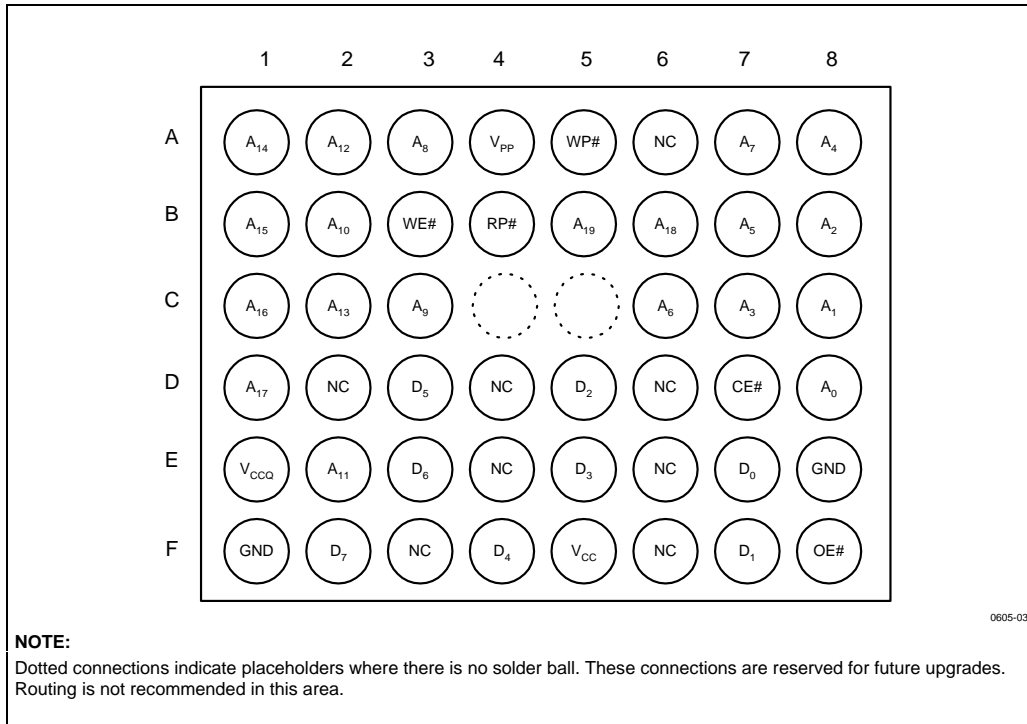


Figure 2. 8-Mbit 48-Ball  $\mu$ BGA\* Chip Size Package



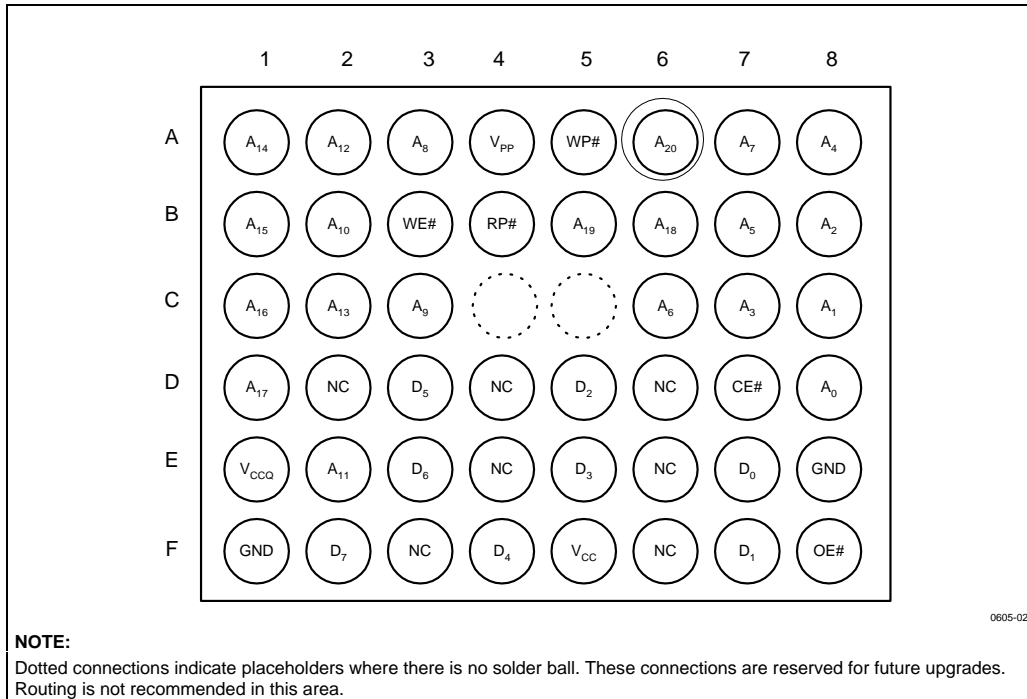


Figure 3. 16-Mbit 48-Ball μBGA\* Chip Size Package

The pin descriptions table details the usage of each device pin.

**Table 2. 16-Mbit Smart 3 Advanced Boot Block Pin Descriptions**

Symbol	Type	Name and Function
A <sub>0</sub> -A <sub>20</sub>	INPUT	<b>ADDRESS INPUTS</b> for memory addresses. Addresses are internally latched during a program or erase cycle. <b>28F008B3: A[0-19], 28F016B3: A[0-20]</b>
DQ <sub>0</sub> -DQ <sub>7</sub>	INPUT/OUTPUT	<b>DATA INPUTS/OUTPUTS:</b> Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched. Outputs array, Intelligent Identifier and Status Register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
CE#	INPUT	<b>CHIP ENABLE:</b> Activates the internal control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels. If CE# and RP# are high, but not at a CMOS high level, the standby current will increase due to current flow through the CE# and RP# inputs.
OE#	INPUT	<b>OUTPUT ENABLE:</b> Enables the device's outputs through the data buffers during an array or status register read. OE# is active low.
WE#	INPUT	<b>WRITE ENABLE:</b> Controls writes to the Command Register and memory array. WE# is active low. Addresses and data are latched on the rising edge of the second WE# pulse.
RP#	INPUT	<b>RESET/DEEP POWER-DOWN:</b> Uses two voltage levels (V <sub>IL</sub> , V <sub>IH</sub> ) to control reset/deep power-down mode.  <b>When RP# is at logic low, the device is in reset/deep power-down mode,</b> which drives the outputs to High-Z, resets the Write State Machine, and draws minimum current.  <b>When RP# is at logic high, the device is in standard operation.</b> When RP# transitions from logic-low to logic-high, the device defaults to the read array mode.
WP#	INPUT	<b>WRITE PROTECT:</b> Provides a method for locking and unlocking the two lockable parameter blocks.  <b>When WP# is at logic low, the lockable blocks are locked,</b> preventing program and erase operations to those blocks. If a program or erase operation is attempted on a locked block, SR.1 and either SR.4 [program] or SR.5 [erase] will be set to indicate the operation failed.  <b>When WP# is at logic high, the lockable blocks are unlocked</b> and can be programmed or erased.  See Section 3.3 for details on write protection.

**Table 2. 16-Mbit Smart 3 Advanced Boot Block Pin Descriptions (Continued)**

Symbol	Type	Name and Function
V <sub>CCQ</sub>	INPUT	<p><b>OUTPUT V<sub>CC</sub></b>: Enables all outputs to be driven to 2.0V ±10% while the V<sub>CC</sub> is at 2.7V. When this mode is used, the V<sub>CC</sub> <b>should</b> be regulated to 2.7V–2.85V to achieve lowest power operation (see Section 6.1: DC Characteristics: V<sub>CCQ</sub> = 1.8V–2.2V).</p> <p>This input may be tied directly to V<sub>CC</sub> (2.7V–3.6V).</p> <p>See the DC Characteristics for further details.</p>
V <sub>CC</sub>		<b>DEVICE POWER SUPPLY: 2.7V–3.6V</b>
V <sub>PP</sub>		<p><b>PROGRAM/ERASE POWER SUPPLY</b>: For erasing memory array blocks or programming data in each block, a voltage of either 2.7V–3.6V or 12V ± 5% must be applied to this pin. When V<sub>PP</sub> &lt; V<sub>PPLK</sub> all blocks are locked and protected against Program and Erase commands.</p> <p>Applying 11.4V–12.6V to V<sub>PP</sub> can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V<sub>PP</sub> may be connected to 12V for a total of 80 hours maximum (see Section 3.4 for details).</p>
GND		<b>GROUND</b> : For all internal circuitry. All ground inputs <b>must</b> be connected.
NC		<b>NO CONNECT</b> : Pin may be driven or left floating.

## 2.2 Block Organization

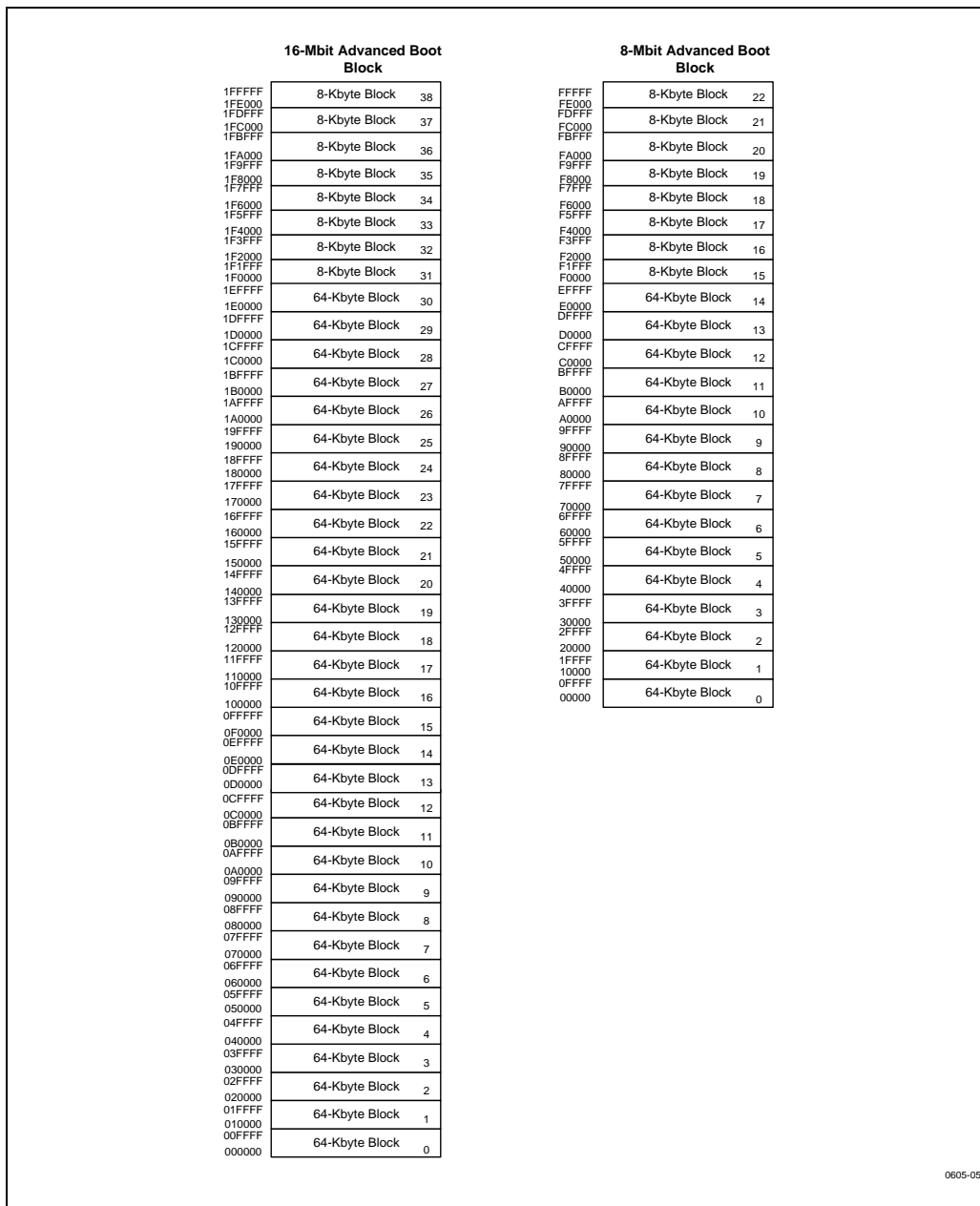
The Smart 3 Advanced Boot Block is an asymmetrically-blocked architecture that enables system integration of code and data within a single flash device. Each block can be erased independently of the others up to 10,000 times. For the address locations of each block, see the memory maps in Figure 4 (top boot blocking) and Figure 5 (bottom boot blocking).

### 2.2.1 PARAMETER BLOCKS

The Smart 3 Advanced Boot Block flash memory architecture includes parameter blocks to facilitate storage of frequently updated small parameters (e.g., data that would normally be stored in an EEPROM). By using software techniques, the byte-rewrite functionality of EEPROMs can be emulated. Each 8-/16-Mbit device contains eight parameter blocks of 8 Kbytes (8,192-bytes) each.

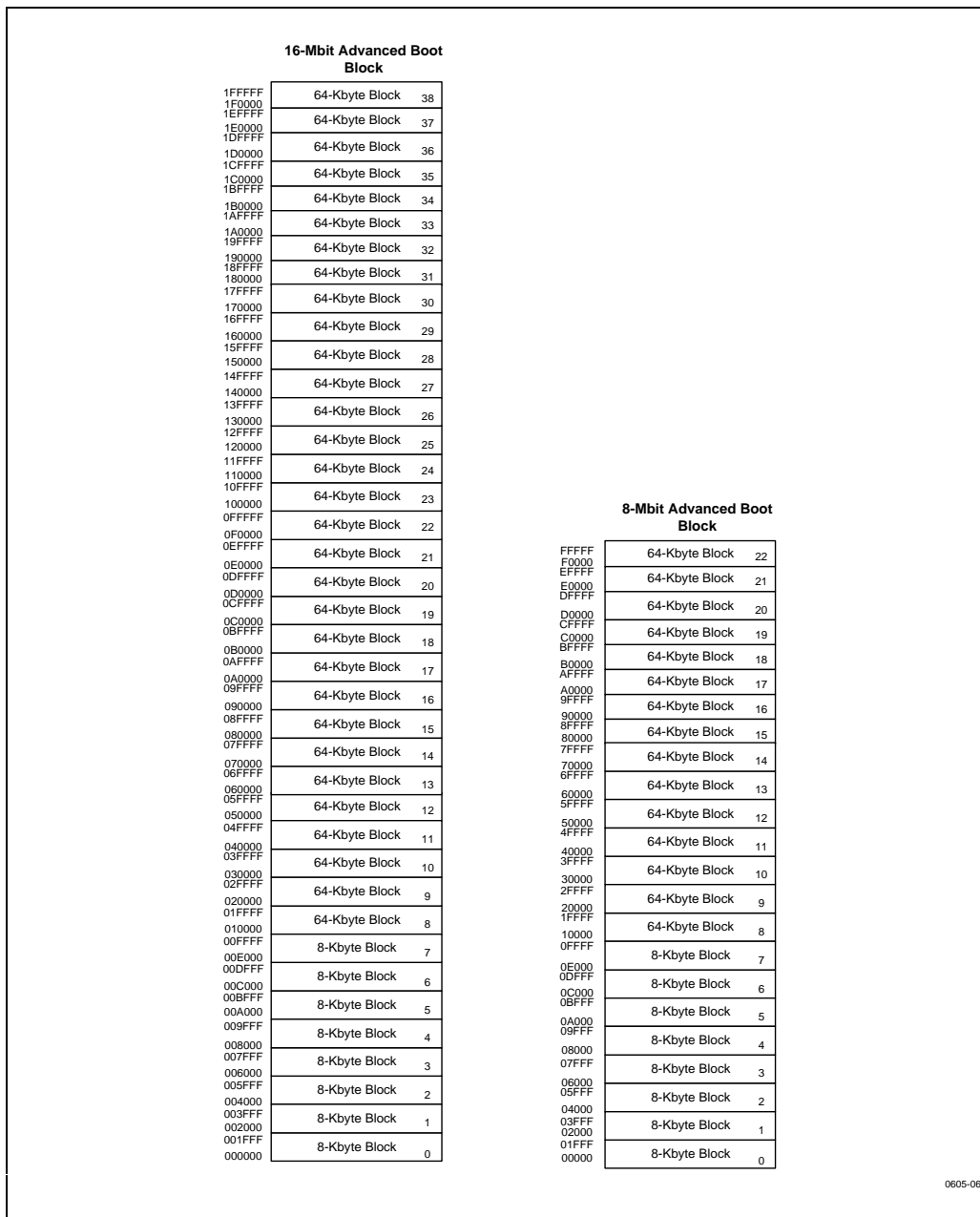
### 2.2.2 MAIN BLOCKS

After the parameter blocks, the remainder of the array is divided into equal size main blocks for data or code storage. Each 16-Mbit device contains thirty-one 64-Kbyte (65,536-byte) blocks. Each 8-Mbit device contains fifteen 64-Kbyte blocks.



0605-05

Figure 4. 8-/16-Mbit Advanced Boot Block Byte-Wide Top Boot Memory Maps



0605-06

Figure 5. 8-/16-Mbit Advanced Boot Block Byte-Wide Bottom Boot Memory Maps



**3.0 PRINCIPLES OF OPERATION**

Flash memory combines EEPROM functionality with in-circuit electrical program and erase capability. The Smart 3 Advanced Boot Block flash memory family utilizes a Command User Interface (CUI) and automated algorithms to simplify program and erase operations. The CUI allows for 100% CMOS-level control inputs, fixed power supplies during erasure and programming, and maximum EEPROM compatibility.

When  $V_{PP} < V_{PPLK}$ , the device will only execute the following commands successfully: Read Array, Read Status Register, Clear Status Register and Read Intelligent Identifier. The device provides standard EEPROM read, standby and output disable operations. Manufacturer identification and device identification data can be accessed through the CUI. In addition, 2.7V or 12V on  $V_{PP}$  allows program and erase of the device. All functions

associated with altering memory contents, namely program and erase, are accessible via the CUI. The internal Write State Machine (WSM) completely automates program and erase operations while the CUI signals the start of an operation and the status register reports status. The CUI handles the WE# interface to the data and address latches, as well as system status requests during WSM operation.

**3.1 Bus Operation**

Smart 3 Advanced Boot Block flash memory devices read, program and erase in-system via the local CPU or microcontroller. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles. Four control pins dictate the data flow in and out of the flash component: CE#, OE#, WE# and RP#. These bus operations are summarized in Table 3.

**Table 3. Bus Operations for Byte-Wide Mode**

Mode	Notes	RP#	CE#	OE#	WE#	WP#	A <sub>0</sub>	V <sub>PP</sub>	DQ <sub>0-7</sub>
Read	1,2,3	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	X	X	D <sub>OUT</sub>
Output Disable	2	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	High Z
Standby	2	V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	X	X	High Z
Deep Power-Down	2,9	V <sub>IL</sub>	X	X	X	X	X	X	High Z
Intelligent Identifier (Mfr.)	2,4	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	V <sub>IL</sub>	X	89 H
Intelligent Identifier (Dvc.)	2,4,5	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	V <sub>IH</sub>	X	See Table 5
Write	2,6,7,8	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	X	V <sub>PPH</sub>	D <sub>IN</sub>

**NOTES:**

1. Refer to DC Characteristics.
2. X must be V<sub>IL</sub>, V<sub>IH</sub> for control pins and addresses, V<sub>PPLK</sub>, V<sub>PPH1</sub> or V<sub>PPH2</sub> for V<sub>PP</sub>.
3. See DC Characteristics for V<sub>PPLK</sub>, V<sub>PPH1</sub>, V<sub>PPH2</sub> voltages.
4. Manufacturer and device codes may also be accessed via a CUI write sequence, A<sub>1</sub>–A<sub>20</sub> = X
5. See Table 5 for device IDs.
6. Refer to Table 6 for valid D<sub>IN</sub> during a write operation.
7. Command writes for block erase or byte program are only executed when V<sub>PP</sub> = V<sub>PPH1</sub> or V<sub>PPH2</sub>.
8. To program or erase the lockable blocks, hold WP# at V<sub>IH</sub>. See Section 3.3.
9. RP# must be at GND ± 0.2V to meet the maximum deep power-down current specified.

### 3.1.1 READ

The flash memory has three read modes available: read array, read identifier, and read status. These modes are accessible independent of the  $V_{PP}$  voltage. The appropriate read mode command must be issued to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from deep power-down mode, the device automatically defaults to read array mode.

CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control; when active it enables the flash memory device. OE# is the data output (DQ<sub>0</sub>–DQ<sub>7</sub>) control and it drives the selected memory data onto the I/O bus. For all read modes, WE# and RP# must be at  $V_{IH}$ . Figure 14 illustrates a read cycle.

### 3.1.2 OUTPUT DISABLE

With OE# at a logic-high level ( $V_{IH}$ ), the device outputs are disabled. Output pins DQ<sub>0</sub>–DQ<sub>7</sub> are placed in a high-impedance state.

### 3.1.3 STANDBY

Deselecting the device by bringing CE# to a logic-high level ( $V_{IH}$ ) places the device in standby mode, which substantially reduces device power consumption. In standby, outputs DQ<sub>0</sub>–DQ<sub>7</sub> are placed in a high-impedance state independent of OE#. If deselected during program or erase operation, the device continues to consume active power until the program or erase operation is complete.

### 3.1.4 DEEP POWER-DOWN/RESET

RP# at  $V_{IL}$  initiates the deep power-down mode, sometimes referred to as reset mode.

From read mode, RP# going low for time  $t_{PLPH}$  accomplishes the following:

1. deselects the memory
2. places output drivers in a high-impedance state

After return from power-down, a time  $t_{PHQV}$  is required until the initial memory access outputs are

valid. A delay ( $t_{PHWL}$  or  $t_{PHEL}$ ) is required after return from power-down before a write sequence can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read array mode, and the status register is set to 80H (ready).

If RP# is taken low for time  $t_{PLPH}$  during a program or erase operation, the operation will be aborted and the memory contents at the aborted location are no longer valid. After returning from an aborted operation, time  $t_{PHQV}$  or  $t_{PHWL}/t_{PHEL}$  must be met before a read or write operation is initiated respectively.

### 3.1.5 WRITE

A write is any command that alters the contents of the memory array. There are two write commands: Program (40H) and Erase (20H). Writing either of these commands to the internal Command User Interface (CUI) initiates a sequence of internally-timed functions that culminate in the completion of the requested task (unless that operation is aborted by either RP# being driven to  $V_{IL}$  for of  $t_{PLRH}$  or an appropriate suspend command).

The Command User Interface does not occupy an addressable memory location. Instead, commands are written into the CUI using standard microprocessor write timings when WE# and CE# are low, OE# =  $V_{IH}$ , and the proper address and data (command) are presented. The command is latched on the rising edge of the first WE# or CE# pulse, whichever occurs first. Figure 15 illustrates a write operation.

Device operations are selected by writing specific commands into the CUI. Table 4 defines the available commands. Appendix B provides detailed information on moving between the different modes of operation.

## 3.2 Modes of Operation

The flash memory has three read modes and two write modes. The read modes are read array, read identifier, and read status. The write modes are program and block erase. Three additional mode (erase suspend to program, erase suspend to read and program suspend to read) are available only during suspended operations. These modes are



reached using the commands summarized in Table 4. A comprehensive chart showing the state transitions is in Appendix B.

**3.2.1 READ ARRAY**

When RP# transitions from V<sub>IL</sub> (reset) to V<sub>IH</sub>, the device will be in the read array mode and will respond to the read control inputs (CE#, address inputs, and OE#) without any commands being written to the CUI.

When the device is in the read array mode, four control signals must be controlled to obtain data at the outputs.

- WE# must be logic high (V<sub>IH</sub>)
- CE# must be logic low (V<sub>IL</sub>)
- OE# must be logic low (V<sub>IL</sub>)
- RP# must be logic high (V<sub>IH</sub>)

In addition, the address of the desired location must be applied to the address pins.

If the device is not in read array mode, as would be the case after a program or erase operation, the Read Array command (FFH) must be written to the CUI before array reads can take place.

**Table 4. Command Codes and Descriptions**

Code	Device Mode	Description
00	Invalid/Reserved	Unassigned commands that should not be used. Intel reserves the right to redefine these codes for future functions.
FF	Read Array	Places the device in read array mode, such that array data will be output on the data pins.
40	Program Set-Up	This is a two-cycle command. The first cycle prepares the CUI for a program operation. The second cycle latches addresses and data information and initiates the WSM to execute the Program algorithm. The flash outputs status register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 3.2.4.
10	Alternate Program Set-Up	(See 40H/Program Set-Up)
20	Erase Set-Up	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will (a) set both SR.4 and SR.5 of the status register to a "1," (b) place the device into the read status register mode, and (c) wait for another command. See Section 3.2.5.
D0	Program Resume Erase Resume/ Erase Confirm	If the previous command was an Erase Set-Up command, then the CUI will close the address and data latches, and begin erasing the block indicated on the address pins. If a program or erase operation was previously suspended, this command will resume that operation.  During program/erase, the device will respond only to the Read Status Register, Program Suspend/Erase Suspend commands and will output status register data when CE# or OE# is toggled.



**Table 4. Command Codes and Descriptions (Continued)**

Code	Device Mode	Description
B0	Program Suspend Erase Suspend	Issuing this command will begin to suspend the currently executing program/erase operation. The status register will indicate when the operation has been successfully suspended by setting either the program suspend (SR.2) or erase suspend (SR.6) and the WSM Status bit (SR.7) to a "1" (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input control pins except RP#, which will immediately shut down the WSM and the remainder of the chip if it is driven to V <sub>IL</sub> . See Sections 3.2.4.1 and 3.2.5.1.
70	Read Status Register	This command places the device into read status register mode. Reading the device will output the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after a program or erase operation has been initiated. See Section 3.2.3.
50	Clear Status Register	The WSM can set the Block Lock Status (SR.1), V <sub>PP</sub> Status (SR.3), Program Status (SR.4), and Erase Status (SR.5) bits in the status register to "1," but it cannot clear them to "0." Issuing this command clears those bits to "0."
90	Intelligent Identifier	Puts the device into the intelligent identifier read mode, so that reading the device will output the manufacturer and device codes (A <sub>0</sub> = 0 for manufacturer, A <sub>0</sub> = 1 for device, all other address inputs are ignored). See Section 3.2.2.

**NOTE:**

See Appendix B for mode transition information.

**3.2.2 READ INTELLIGENT IDENTIFIER**

To read the manufacturer and device codes, the device must be in read intelligent identifier mode, which can be reached by writing the Intelligent Identifier command (90H). Once in intelligent identifier mode, A<sub>0</sub> = 0 outputs the manufacturer's identification code and A<sub>0</sub> = 1 outputs the device code. See Table 5 for product signatures. To return to read array mode, write the Read Array command (FFH).

**Table 5. Intelligent Identifier Table**

Size	Mfr. ID	Device ID	
		-T (Top Boot)	-B (Bottom Boot)
8-Mbit	89H	D2H	D3H
16-Mbit	89H	D0H	D1H

**3.2.3 READ STATUS REGISTER**

The device status register indicates when a program or erase operation is complete, and the success or failure of that operation. To read the status register issue the Read Status Register (70H) command to the CUI. This causes all subsequent read operations to output data from the status register until another command is written to the CUI. To return to reading from the array, issue the Read Array (FFH) command.

The status register bits are output on DQ<sub>0</sub>-DQ<sub>7</sub>.

The contents of the status register are latched on the falling edge of OE# or CE#. This prevents possible bus errors which might occur if status register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the status register will not indicate completion of a program or erase operation.

When the WSM is active, bit 7 (SR.7) of the status register will indicate the status of the WSM; the remaining bits in the status register indicate whether or not the WSM was successful in performing the desired operation (see Table 7).

### 3.2.3.1 Clearing the Status Register

The WSM sets status bits 1 through 7 to “1,” and clears bits 2, 6 and 7 to “0,” but cannot clear status bits 1 or 3 through 5 to “0.” Because bits 1, 3, 4, and 5 indicate various error conditions, these bits can only be cleared by the controlling CPU through the use of the Clear Status Register (50H) command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before reading the status register to determine if an error occurred during that series. Clear the Status Register before beginning another command or sequence. Note, again, that the Read Array command must be issued before data can be read from the memory array.

### 3.2.4 PROGRAM MODE

Programming is executed using a two-write sequence. The Program Setup command (40H) is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute the following sequence of internally timed events:

1. Program the desired bits of the addressed memory.
2. Verify that the desired bits are sufficiently programmed.

Programming of the memory results in specific bits within an address location being changed to a “0.” If the user attempts to program “1”s, there will be no change of the memory cell contents and no error occurs.

The status register indicates programming status: while the program sequence is executing, bit 7 of the status register is a “0.” The status register can be polled by toggling either CE# or OE#. While programming, the only valid commands are Read Status Register, Program Suspend, and Program Resume.

When programming is complete, the Program Status bits should be checked. If the programming operation was unsuccessful, bit SR.4 of the status register is set to indicate a program failure. If SR.3 is set then  $V_{PP}$  was not within acceptable limits, and the WSM did not execute the program command. If SR.1 is set, a program operation was attempted to a locked block and the operation was aborted.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent status register reads, be sure to reset the CUI to read array mode.

### 3.2.4.1 Suspending and Resuming Program

The Program Suspend command allows program suspension in order to read data in other locations of memory. Once the programming process starts, writing the Program Suspend command to the CUI requests that the WSM suspend the program sequence (at predetermined points in the program algorithm). The device continues to output status register data after the Program Suspend command is written. Polling status register bits SR.7 and SR.2 will determine when the program operation has been suspended (both will be set to “1”).  $t_{WHRH1}/t_{EHRH1}$  specify the program suspend latency.

A Read Array command can now be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands, while program is suspended, are Read Status Register and Program Resume. After the Program Resume command is written to the flash memory, the WSM will continue with the program process and status register bits SR.2 and SR.7 will automatically be cleared. After the Program Resume command is written, the device automatically outputs status register data when read (see Figure 7, Program Suspend/Resume Flowchart).  $V_{PP}$  must remain at the same  $V_{PP}$  level used for program while in program suspend mode. RP# must also remain at  $V_{IH}$ .

### 3.2.4.2 $V_{PP}$ Supply Voltage during Program

$V_{PP}$  supply voltage considerations are outlined in Section 3.4.

### 3.2.5 ERASE MODE

To erase a block, write the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1." Only one block can be erased at a time.

The WSM will execute the following sequence of internally timed events to:

1. Program all bits within the block to "0."
2. Verify that all bits within the block are sufficiently programmed to "0."
3. Erase all bits within the block to "1."
4. Verify that all bits within the block are sufficiently erased.

While the erase sequence is executing, bit 7 of the status register is a "0."

When the status register indicates that erasure is complete, check the Erase Status bit to verify that the erase operation was successful. If the Erase operation was unsuccessful, SR.5 of the status register will be set to a "1," indicating an erase error. If  $V_{PP}$  was not within acceptable limits after the Erase Confirm command was issued, the WSM will not execute the erase sequence; instead, SR.5 of the status register is set to indicate an erase error, and SR.3 is set to a "1" to identify that  $V_{PP}$  supply voltage was not within acceptable limits.

After an erase operation, clear the Status Register (50H) before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, to prevent inadvertent status register reads, it is advisable to reset the flash to read array after the erase is complete.

### 3.2.5.1 Suspending and Resuming Erase

Since an erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from or program data to another block in memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The status register will indicate if/when the erase operation has been suspended.

A Read Array/Program command can now be written to the CUI in order to read/write data from/to blocks other than that which is suspended. The Program command can subsequently be suspended to read yet another array location. The only valid commands while erase is suspended are Erase Resume, Program, Program Resume, Read Array, or Read Status Register.

During erase suspend mode, the chip can be placed in a pseudo-standby mode by taking CE# to  $V_{IH}$ . This reduces active current consumption.

Erase Resume continues the erase sequence when CE# =  $V_{IL}$ . As with the end of a standard erase operation, the status register must be read and cleared before the next instruction is issued.

### 3.2.5.2 $V_{PP}$ Supply Voltage during Erase

$V_{PP}$  supply voltage considerations are outlined in Section 3.4.

Table 6. Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array	5	Write	X	FFH			
Intelligent Identifier	2,3,5	Write	X	90H	Read	IA	ID
Read Status Register	5	Write	X	70H	Read	X	SRD
Clear Status Register	5	Write	X	50H			
Write (Program)	4,5	Write	X	40H	Write	PA	PD
Alternate Write (Program)	4,5	Write	X	10H	Write	PA	PD
Block Erase/Confirm	5	Write	X	20H	Write	BA	D0H
Program/Erase Suspend	5	Write	X	B0H			
Program/Erase Resume	5	Write	X	D0H			

**ADDRESS**

BA = Block Address  
 IA = Identifier Address  
 PA = Program Address  
 X = Don't Care

**DATA**

SRD = Status Register Data  
 ID = Identifier Data  
 PD = Program Data

**NOTES:**

1. Bus operations are defined in Table 3.
2. A<sub>0</sub> = 0 for manufacturer code, A<sub>0</sub> = 1 for device code.
3. Following the Intelligent Identifier command, two read operations access manufacturer and device codes.
4. Either 40H or 10H command is valid.

**Table 7. Status Register Bit Definition**

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0
<b>NOTES:</b>							
<b>SR.7 WRITE STATE MACHINE STATUS</b> 1 = Ready (WSMS) 0 = Busy				Check Write State Machine bit first to determine Byte Program or Block Erase completion, before checking Program or Erase Status bits.			
<b>SR.6 = ERASE-SUSPEND STATUS (ESS)</b> 1 = Erase Suspended 0 = Erase In Progress/Completed				When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an Erase Resume command is issued.			
<b>SR.5 = ERASE STATUS (ES)</b> 1 = Error In Block Erasure 0 = Successful Block Erase				When this bit is set to "1," WSM has applied the max. number of erase pulses to the block and is still unable to verify successful block erasure.			
<b>SR.4 = PROGRAM STATUS (PS)</b> 1 = Error in Byte Program 0 = Successful Byte Program				When this bit is set to "1," WSM has attempted but failed to program a byte.			
<b>SR.3 = V<sub>PP</sub> STATUS (VPPS)</b> 1 = V <sub>PP</sub> Low Detect, Operation Abort 0 = V <sub>PP</sub> OK				The V <sub>PP</sub> Status bit does not provide continuous indication of V <sub>PP</sub> level. The WSM interrogates V <sub>PP</sub> level only after the Program or Erase command sequences have been entered, and informs the system if V <sub>PP</sub> has not been switched on. The V <sub>PP</sub> is also checked before the operation is verified by the WSM. The V <sub>PP</sub> Status bit is not guaranteed to report accurate feedback between V <sub>PP</sub> and V <sub>PPH</sub> .			
<b>SR.2 = PROGRAM SUSPEND STATUS (PSS)</b> 1 = Program Suspended 0 = Program in Progress/Completed				When Program Suspend is issued, WSM halts execution and sets both WSMS and PSS bits to "1." PSS bit remains set to "1" until a Program Resume command is issued.			
<b>SR.1 = Block Lock Status</b> 1 = Program/Eraser attempted on locked block; Operation aborted 0 = No operation to locked blocks				If a program or erase operation is attempted to one of the locked blocks, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.			
<b>SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)</b>				These bits are reserved for future use and should be masked out when polling the Status Register.			

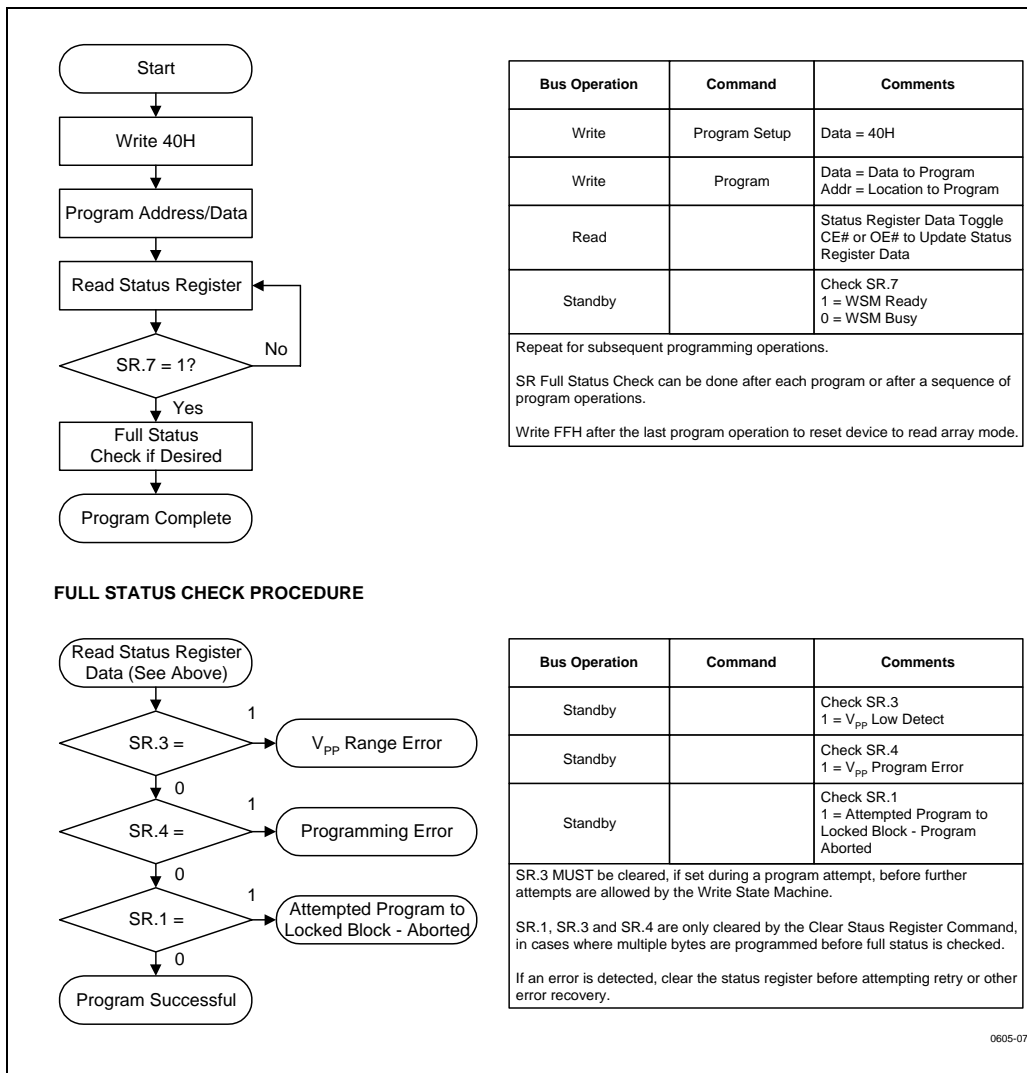


Figure 6. Automated Byte Programming Flowchart

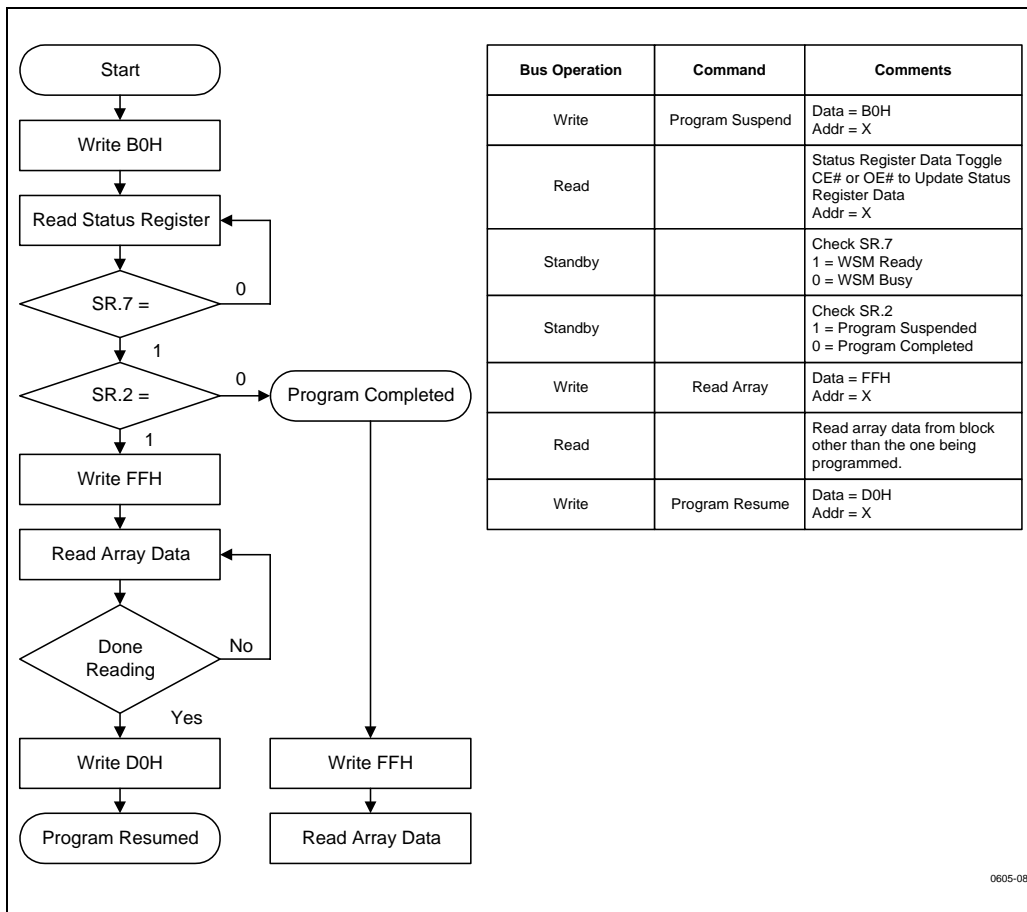


Figure 7. Program Suspend/Resume Flowchart

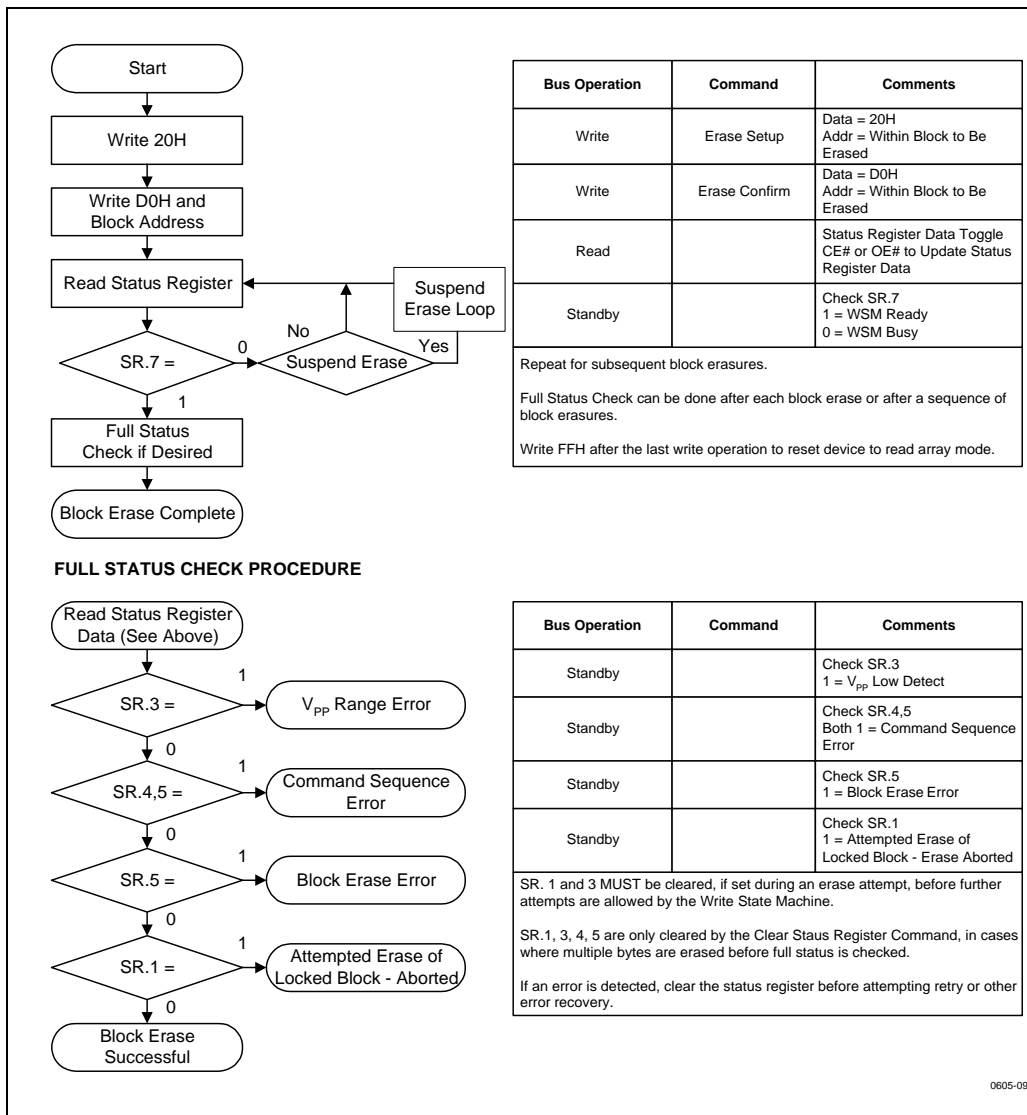


Figure 8. Automated Block Erase Flowchart



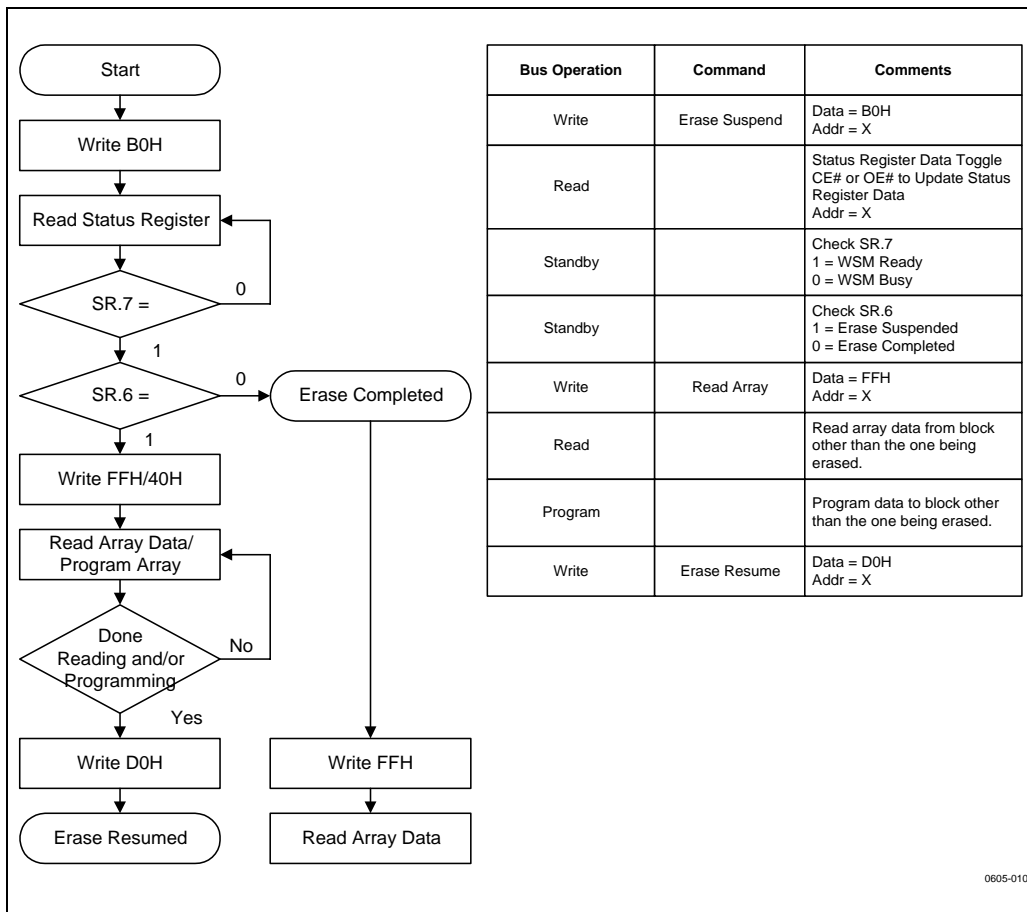


Figure 9. Erase Suspend/Resume Flowchart



### 3.3 Block Locking

The Smart 3 Advanced Boot Block flash memory architecture features two hardware-lockable parameter blocks so that the kernel code for the system can be kept secure while other parameter blocks are programmed or erased as necessary.

#### 3.3.1 $V_{PP} = V_{IL}$ FOR COMPLETE PROTECTION

The  $V_{PP}$  programming voltage can be held low for complete write protection of all blocks in the flash device. When  $V_{PP}$  is below  $V_{PPLK}$ , any program or erase operation will result in a error, prompting the corresponding Status Register bit (SR.3) to be set.

#### 3.3.2 $WP\# = V_{IL}$ FOR BLOCK LOCKING

The lockable blocks are locked when  $WP\# = V_{IL}$ ; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two parameter blocks (blocks #37 and #38 for the 16-Mbit, and blocks #21 and #22 for the 8-Mbit) are lockable. For the bottom configuration, the bottom two parameter blocks (blocks #0 and #1 for 8-/16-Mbit) are lockable. Unlocked blocks can be programmed or erased normally (unless  $V_{PP}$  is below  $V_{PPLK}$ ).

#### 3.3.3 $WP\# = V_{IH}$ FOR BLOCK UNLOCKING

$WP\# = V_{IH}$  unlocks all lockable blocks.

These blocks can now be programmed or erased.

Note that  $RP\#$  does not override  $WP\#$  locking as in previous Boot Block devices.  $WP\#$  controls all block locking and  $V_{PP}$  provides protection against spurious writes. Table 8 defines the write protection methods.

### 3.4 $V_{PP}$ Program and Erase Voltages

Intel's Smart 3 products provide in-system programming and erase at 2.7V–3.6V  $V_{PP}$ . For customers requiring fast programming in their manufacturing environment, Smart 3 Advanced Boot Block includes an additional low-cost, backward-compatible 12V programming feature.

The 12V  $V_{PP}$  mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12V may be applied to  $V_{PP}$  during program and erase operations for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks.  $V_{PP}$  may be connected to 12V for a total of 80 hours maximum. Stressing the device beyond these limits may cause permanent damage.

**Table 8. Write Protection Truth Table for Advanced Boot Block Flash Memory Family**

$V_{PP}$	$WP\#$	$RP\#$	Write Protection Provided
X	X	$V_{IL}$	All Blocks Locked
$V_{IL}$	X	$V_{IH}$	All Blocks Locked
$\geq V_{PPLK}$	$V_{IL}$	$V_{IH}$	Lockable Blocks Locked
$\geq V_{PPLK}$	$V_{IH}$	$V_{IH}$	All Blocks Unlocked

### 3.5 Power Consumption

While in operation, the flash device consumes active power. However, Intel flash devices have a three-tiered approach to power savings that can significantly reduce overall system power consumption. The Automatic Power Savings (APS) feature reduces power consumption when the device is idle. If the  $CE\#$  is deasserted, the flash enters its standby mode, where current consumption is even lower. If  $RP\# = V_{IL}$  the flash enters a deep power-down mode, where current is at a minimum. The combination of these features can minimize overall memory power consumption, and therefore, overall system power consumption.

#### 3.5.1 ACTIVE POWER

With  $CE\#$  at a logic-low level and  $RP\#$  at a logic-high level, the device is in the active mode. Refer to the DC Characteristics tables for  $I_{CC}$  current values. Active power is the largest contributor to overall system power consumption. Minimizing the active current could have a profound effect on system power consumption, especially for battery-operated devices.

### 3.5.2 AUTOMATIC POWER SAVINGS (APS)

Automatic Power Savings provides low-power operation during active mode. Power Reduction Control (PRC) circuitry allows the flash to put itself into a low current state when not being accessed. After data is read from the memory array, PRC logic controls the device's power consumption by entering the APS mode where typical  $I_{CC}$  current is comparable to  $I_{CCS}$ . The flash stays in this static state with outputs valid until a new location is read.

APS reduces active current to standby current levels for 2.7V–3.6V CMOS input levels.

### 3.5.3 STANDBY POWER

With  $CE\#$  at a logic-high level ( $V_{IH}$ ) and the CUI in read mode, the flash memory is in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs ( $DQ_0$ – $DQ_7$ ) are placed in a high-impedance state independent of the status of the  $OE\#$  signal. If  $CE\#$  transitions to a logic-high level during erase or program operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

System engineers should analyze the breakdown of standby time versus active time and quantify the respective power consumption in each mode for their specific application. This will provide a more accurate measure of application-specific power and energy requirements.

### 3.5.4 DEEP POWER-DOWN MODE

The deep power-down mode of the Smart 3 Advanced Boot Block products switches the device into a low power savings mode, which is especially important for battery-based devices. This mode is activated when  $RP\# = V_{IL}$ . ( $GND \pm 0.2V$ ).

During read modes,  $RP\#$  going low de-selects the memory and places the output drivers in a high impedance state. Recovery from the deep power-down state, requires a minimum time equal to  $t_{PHQV}$  (see AC Characteristics table).

During program or erase modes,  $RP\#$  transitioning low will abort the operation, but the memory contents of the address being programmed or the block being erased are no longer valid as the data integrity has been compromised by the abort.

During deep power-down, all internal circuits are switched to a low power savings mode ( $RP\#$  transitioning to  $V_{IL}$  or turning off power to the device clears the status register).

## 3.6 Power-Up/Down Operation

The device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required, since the device is indifferent as to which power supply,  $V_{PP}$  or  $V_{CC}$ , powers-up first.

### 3.6.1 $RP\#$ CONNECTED TO SYSTEM RESET

The use of  $RP\#$  during system reset is important with automated program/erase devices since the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. Intel recommends connecting  $RP\#$  to the system CPU  $RESET\#$  signal to allow proper CPU/flash initialization following system reset.

System designers must guard against spurious writes when  $V_{CC}$  voltages are above  $V_{LKO}$  and  $V_{PP}$  is active. Since both  $WE\#$  and  $CE\#$  must be low for a command write, driving either signal to  $V_{IH}$  will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until  $RP\#$  is brought to  $V_{IH}$ , regardless of the state of its control inputs. By holding the device in reset ( $RP\#$  connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

### 3.6.2 $V_{CC}$ , $V_{PP}$ AND $RP\#$ TRANSITIONS

The CUI latches commands as issued by system software and is not altered by  $V_{PP}$  or  $CE\#$  transitions or WSM actions. Its default state upon power-up, after exit from deep power-down mode or after  $V_{CC}$  transitions above  $V_{LKO}$  (Lockout voltage), is read array mode.

After any program or block erase operation is complete (even after  $V_{PP}$  transitions down to  $V_{PPLK}$ ), the CUI must be reset to read array mode via the Read Array command if access to the flash memory array is desired.

Refer to *AP-617 Additional Flash Data Protection Using  $V_{PP}$ ,  $RP\#$ , and  $WP\#$*  for a circuit-level description of how to implement the protection schemes discussed in Section 3.5.

### 3.7 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling. System designers should consider three supply current issues:

1. Standby current levels ( $I_{CCS}$ )
2. Active current levels ( $I_{CCR}$ )
3. Transient peaks produced by falling and rising edges of  $CE\#$ .

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1  $\mu\text{F}$  ceramic capacitor connected between each  $V_{CC}$  and GND, and between its  $V_{PP}$  and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

#### 3.7.1 $V_{PP}$ TRACE ON PRINTED CIRCUIT BOARDS

Designing for in-system writes to the flash memory requires special consideration of the  $V_{PP}$  power supply trace by the printed circuit board designer. The  $V_{PP}$  pin supplies the flash memory cells current for programming and erasing.  $V_{PP}$  trace widths and layout should be similar to that of  $V_{CC}$ . Adequate  $V_{PP}$  supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.



**4.0 ABSOLUTE MAXIMUM RATINGS\***

- Extended Operating Temperature
  - During Read ..... -40°C to +85°C
  - During Block Erase and Program..... -40°C to +85°C
  - Temperature Under Bias ..... -40°C to +85°C
- Storage Temperature..... -65°C to +125°C
- Voltage on Any Pin (except V<sub>CC</sub>, V<sub>CCQ</sub> and V<sub>PP</sub>) with Respect to GND ..... -0.5V to +5.0V<sup>1</sup>
- V<sub>PP</sub> Voltage (for Block Erase and Program) with Respect to GND ..... -0.5V to +13.5V<sup>1,2,4</sup>
- V<sub>CC</sub> and V<sub>CCQ</sub> Supply Voltage with Respect to GND ..... -0.2V to +5.0V<sup>1</sup>
- Output Short Circuit Current..... 100 mA<sup>3</sup>

NOTICE: This datasheet contains preliminary information on products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

\* **WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

**NOTES:**

1. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods < 20 ns. Maximum DC voltage on input/output pins is V<sub>CC</sub> + 0.5V which, during transitions, may overshoot to V<sub>CC</sub> + 2.0V for periods < 20 ns.
2. Maximum DC voltage on V<sub>PP</sub> may overshoot to +14.0V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. V<sub>PP</sub> Program voltage is normally 2.7V-3.6V. Connection to supply of 11.4V-12.6V can only be done for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase. V<sub>PP</sub> may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.

**5.0 OPERATING CONDITIONS (V<sub>CCQ</sub> = 2.7V-3.6V)**

Table 9. Temperature and Voltage Operating Conditions<sup>4</sup>

Symbol	Parameter	Notes	Min	Max	Units
T <sub>A</sub>	Operating Temperature		-40	+85	°C
V <sub>CC</sub>	2.7V-3.6V V <sub>CC</sub> Supply Voltage	1,4	2.7	3.6	Volts
V <sub>CCQ</sub>	2.7V-3.6V I/O Supply Voltage	1,2,4	2.7	3.6	Volts
V <sub>PP1</sub>	Program and Erase Voltage	4	2.7	3.6	Volts
V <sub>PP2</sub>		3	11.4	12.6	Volts
Cycling	Block Erase Cycling	5	10,000		Cycles

**NOTES:**

1. See DC Characteristics tables for voltage range-specific specifications.
2. The voltage swing on the inputs, V<sub>IN</sub> is required to match V<sub>CCQ</sub>.
3. Applying V<sub>PP</sub> = 11.4V-12.6V during a program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V<sub>PP</sub> may be connected to 12V for a total of 80 hours maximum. See section 3.4 for details.
4. V<sub>CC</sub>, V<sub>CCQ</sub> and V<sub>PP1</sub> must share the same supply when all three are between 2.7V and 3.6V.
5. For operating temperatures of -25°C- +85°C the device is projected to have a minimum block erase cycling of 10,000 to 30,000 cycles.

5.1 DC Characteristics:  $V_{CCQ} = 2.7V-3.6V$

Table 10. DC Characteristics

Sym	Parameter	Notes	$V_{CC} = 2.7V-3.6V$		Unit	Test Conditions
			Typ	Max		
$I_{LI}$	Input Load Current	1		$\pm 1.0$	$\mu A$	$V_{CC} = V_{CCMax} = V_{CCQMax}$ $V_{IN} = V_{CCQ}$ or GND
$I_{LO}$	Output Leakage Current	1		$\pm 10$	$\mu A$	$V_{CC} = V_{CCMax} = V_{CCQMax}$ $V_{IN} = V_{CCQ}$ or GND
$I_{CCS}$	$V_{CC}$ Standby Current	1,7	20	50	$\mu A$	<b>CMOS INPUTS</b> $V_{CC} = V_{CCMax} = V_{CCQMax}$ $CE\# = RP\# = V_{CCQ}$
$I_{CCD}$	$V_{CC}$ Deep Power-Down Current	1,7	1	10	$\mu A$	<b>CMOS INPUTS</b> $V_{CC} = V_{CCMax} = V_{CCQMax}$ $V_{IN} = V_{CCQ}$ or GND $RP\# = GND \pm 0.2V$
$I_{CCR}$	$V_{CC}$ Read Current	1,5,7	10	20	mA	<b>CMOS INPUTS</b> $V_{CC} = V_{CCMax} = V_{CCQMax}$ $OE\# = V_{IH}$ , $CE\# = V_{IL}$ $f = 5$ MHz, $I_{OUT} = 0$ mA Inputs = $V_{IL}$ or $V_{IH}$
$I_{CCW}$	$V_{CC}$ Program Current	1,4,7	8	20	mA	$V_{PP} = V_{PPH1}$ (3V) Program in Progress
			8	20	mA	$V_{PP} = V_{PPH2}$ (12V) Program in Progress
$I_{CCE}$	$V_{CC}$ Erase Current	1,4,7	8	20	mA	$V_{PP} = V_{PPH1}$ (3V) Erase in Progress
			8	20	mA	$V_{PP} = V_{PPH2}$ (12V) Erase in Progress
$I_{CCES}$	$V_{CC}$ Erase Suspend Current	1,2,4,7	20	50	$\mu A$	$CE\# = V_{IH}$ Erase Suspend in Progress
$I_{CCWS}$	$V_{CC}$ Program Suspend Current	1,2,4,7	20	50	$\mu A$	$CE\# = V_{IH}$ Program Suspend in Progress
$I_{PPD}$	$V_{PP}$ Deep Power-Down Current	1	0.2	5	$\mu A$	$RP\# = GND \pm 0.2V$
$I_{PPR}$	$V_{PP}$ Read Current	1	2	$\pm 50$	$\mu A$	$V_{PP} \leq V_{CC}$

**Table 10. DC Characteristics (Continued)**

Sym	Parameter	Notes	V <sub>CC</sub> = 2.7V–3.6V		Unit	Test Conditions
			Typ	Max		
I <sub>PPW</sub>	V <sub>PP</sub> Program Current	1,4	15	40	mA	V <sub>PP</sub> = V <sub>PPH1</sub> (3V) Program in Progress
			10	25	mA	V <sub>PP</sub> = V <sub>PPH2</sub> (12V) Program in Progress
I <sub>PPE</sub>	V <sub>PP</sub> Erase Current	1,4	13	25	mA	V <sub>PP</sub> = V <sub>PPH1</sub> (3V) Erase in Progress
			8	25	mA	V <sub>PP</sub> = V <sub>PPH2</sub> (12V) Erase in Progress
I <sub>PPES</sub>	V <sub>PP</sub> Erase Suspend Current	1,4	50	200	μA	V <sub>PP</sub> = V <sub>PPH1</sub> or V <sub>PPH2</sub> Erase Suspend in Progress
I <sub>PPWS</sub>	V <sub>PP</sub> Program Suspend Current	1,4	50	200	μA	V <sub>PP</sub> = V <sub>PPH1</sub> or V <sub>PPH2</sub> Program Suspend in Progress

Table 10. DC Characteristics (Continued)

Sym	Parameter	Notes	V <sub>CC</sub> = 2.7V–3.6V		Unit	Test Conditions
			Min	Max		
V <sub>IL</sub>	Input Low Voltage		-0.4	0.4	V	
V <sub>IH</sub>	Input High Voltage		V <sub>CCQ</sub> - 0.4V		V	
V <sub>OL</sub>	Output Low Voltage			0.10	V	V <sub>CC</sub> = V <sub>CCMin</sub> = V <sub>CCQMin</sub> I <sub>OL</sub> = 100 μA
V <sub>OH</sub>	Output High Voltage		V <sub>CCQ</sub> - 0.1V		V	V <sub>CC</sub> = V <sub>CCMin</sub> = V <sub>CCQMin</sub> I <sub>OH</sub> = -100 μA
V <sub>PPLK</sub>	V <sub>PP</sub> Lock-Out Voltage	3	1.5		V	Complete Write Protection
V <sub>PPH1</sub>	V <sub>PP</sub> during Prog/Erase Operations	3	2.7	3.6	V	
V <sub>PPH2</sub>		3,6	11.4	12.6	V	
V <sub>LKO</sub>	V <sub>CC</sub> Program/Erase Lock Voltage		1.5		V	
V <sub>LKO2</sub>	V <sub>CCQ</sub> Program/Erase Lock Voltage		1.2		V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V<sub>CC</sub>, T<sub>A</sub> = +25°C.
2. I<sub>CCES</sub> and I<sub>CCWS</sub> are specified with device de-selected. If device is read while in erase suspend, current draw is I<sub>CCR</sub>. If the device is read while in program suspend, current draw is I<sub>CCR</sub>.
3. Erase and Program are inhibited when V<sub>PP</sub> < V<sub>PPLK</sub> and not guaranteed outside the valid V<sub>PP</sub> ranges of V<sub>PPH1</sub> and V<sub>PPH2</sub>.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I<sub>CCR</sub> to approximately standby levels in static operation (CMOS inputs).
6. Applying V<sub>PP</sub> = 11.4V–12.6V during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V<sub>PP</sub> may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.
7. Includes the sum of V<sub>CC</sub> and V<sub>CCQ</sub> current.

Table 11. Capacitance (T<sub>A</sub> = 25°C, f = 1 MHz)

Sym	Parameter	Notes	Typ	Max	Units	Conditions
C <sub>IN</sub>	Input Capacitance	1	6	8	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub>	Output Capacitance	1	10	12	pF	V <sub>OUT</sub> = 0V

NOTE:

1. Sampled, not 100% tested.



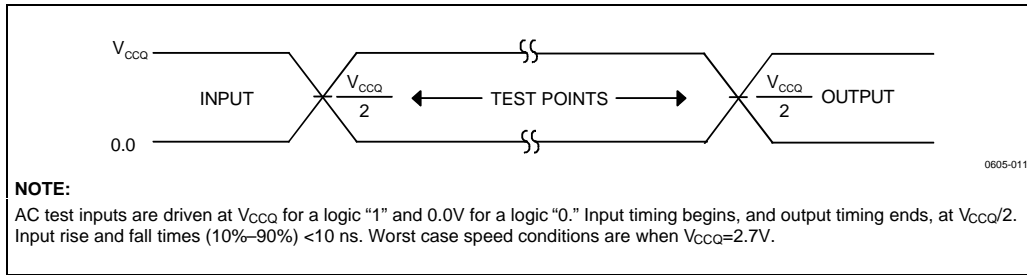


Figure 10. 2.7V–3.6V Input Range and Measurement Points

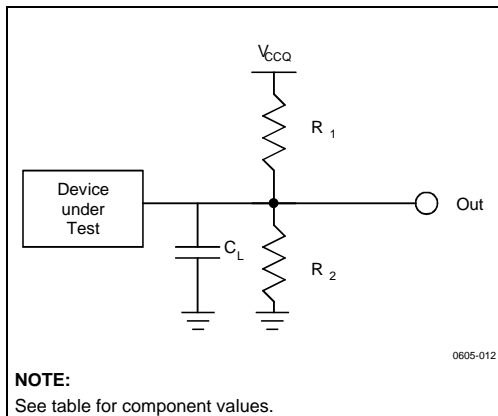


Figure 11. Test Configuration

Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	$C_L$ (pF)	$R_1$ ( $\Omega$ )	$R_2$ ( $\Omega$ )
2.7V Standard Test	50	25K	25K

## 6.0 OPERATING CONDITIONS ( $V_{CCQ} = 1.8V-2.2V$ )

Table 12. Temperature and  $V_{CC}$  Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
$T_A$	Operating Temperature		-40	+85	°C
$V_{CC1}$	2.7V–2.85V $V_{CC}$ Supply Voltage	1	2.7	2.85	Volts
$V_{CC2}$	2.7V–3.3V $V_{CC}$ Supply Voltage	1	2.7	3.3	Volts
$V_{CCQ}$	1.8V–2.2V I/O Supply Voltage	1,4	1.8	2.2	Volts
$V_{PP1}$	Program and Erase Voltage	1	2.7	2.85	Volts
$V_{PP2}$		1	2.7	3.3	Volts
$V_{PP3}$		1,2	11.4	12.6	Volts
Cycling	Block Erase Cycling	3	10,000		Cycles

### NOTES:

- See DC Characteristics tables for voltage range-specific specifications.
- Applying  $V_{PP} = 11.4V-12.6V$  during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter.  $V_{PP}$  may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.
- For operating temperatures of  $-25^{\circ}C-+85^{\circ}C$  the device is projected to have a minimum block erase cycling of 10,000 to 30,000 cycles.
- The voltage swing on the inputs,  $V_{IN}$  is required to match  $V_{CCQ}$ .

## 6.1 DC Characteristics: $V_{CCQ} = 1.8V-2.2V$

These tables are valid for the following power supply combinations only:

- $V_{CC1}$  and  $V_{CCQ}$  and ( $V_{PP1}$  or  $V_{PP3}$ )
- $V_{CC2}$  and  $V_{CCQ}$  and ( $V_{PP2}$  or  $V_{PP3}$ )

Wherever the input voltage  $V_{IN}$  is mentioned, it is required that  $V_{IN}$  matches the chosen  $V_{CCQ}$ .

**Table 13. DC Characteristics:  $V_{CCQ} = 1.8V-2.2V$** 

Sym	Parameter	Notes	$V_{CC1}$ : 2.7V–2.85V $V_{CC2}$ : 2.7V–3.3V		Unit	Test Conditions
			Typ	Max		
$I_{LI}$	Input Load Current	1		$\pm 1.0$	$\mu A$	$V_{CC} = V_{CCMax}$ $V_{CCQ} = V_{CCQMax}$ $V_{IN} = V_{CCQ}$ or GND
$I_{LO}$	Output Leakage Current	1		$\pm 10$	$\mu A$	$V_{CC} = V_{CCMax}$ $V_{CCQ} = V_{CCQMax}$ $V_{IN} = V_{CCQ}$ or GND
$I_{CCS}$	$V_{CC}$ Standby Current	1,7	20	50	$\mu A$	<b>CMOS INPUTS</b> $V_{CC} = V_{CC1Max}$ (2.7V–2.85V) $V_{CCQ} = V_{CCQMax}$ $CE\# = RP\# = V_{CCQ}$
			150	250	$\mu A$	<b>CMOS INPUTS</b> $V_{CC} = V_{CC2Max}$ (2.7V–3.3V) $V_{CCQ} = V_{CCQMax}$ $CE\# = RP\# = V_{CCQ}$
$I_{CCD}$	$V_{CC}$ Deep Power-Down Current	1,7	1	10	$\mu A$	<b>CMOS INPUTS</b> $V_{CC} = V_{CCMax}$ ( $V_{CC1}$ or $V_{CC2}$ ) $V_{CCQ} = V_{CCQMax}$ $V_{IN} = V_{CCQ}$ or GND $RP\# = GND \pm 0.2V$
$I_{CCR}$	$V_{CC}$ Read Current	1,5,7	8	18	mA	<b>CMOS INPUTS</b> $V_{CC} = V_{CC1Max}$ (2.7V–2.85V) $V_{CCQ} = V_{CCQMax}$ $OE\# = V_{IH}$ , $CE\# = V_{IL}$ $f = 5$ MHz, $I_{OUT} = 0$ mA Inputs = $V_{IL}$ or $V_{IH}$
			12	23	mA	<b>CMOS INPUTS</b> $V_{CC} = V_{CC2Max}$ (2.7V–3.3V) $V_{CCQ} = V_{CCQMax}$ $OE\# = V_{IH}$ , $CE\# = V_{IL}$ $f = 5$ MHz, $I_{OUT} = 0$ mA Inputs = GND $\pm 0.2V$ or $V_{CCQ}$

Table 13. DC Characteristics:  $V_{CCQ} = 1.8V-2.2V$  (Continued)

Sym	Parameter	Notes	$V_{CC1}$ : 2.7V–2.85V $V_{CC2}$ : 2.7V–3.3V		Unit	Test Conditions
			Typ	Max		
$I_{CCW}$	$V_{CC}$ Program Current	1,4,7	8	20	mA	$V_{PP} = V_{PPH1}$ or $V_{PPH2}$ Program in Progress
			8	20	mA	$V_{PP} = V_{PPH3}$ (12V) Program in Progress
$I_{CCE}$	$V_{CC}$ Erase Current	1,4,7	8	20	mA	$V_{PP} = V_{PPH1}$ or $V_{PPH2}$ Erase in Progress
			8	20	mA	$V_{PP} = V_{PPH3}$ (12V) Erase in Progress
$I_{CCES}$	$V_{CC}$ Erase Suspend Current	1,2,4,7	20	50	$\mu A$	$CE\# = V_{IH}$ Erase Suspend in Progress
$I_{CCWS}$	$V_{CC}$ Program Suspend Current	1,2,4,7	20	50	$\mu A$	$CE\# = V_{IH}$ Program Suspend in Progress
$I_{PPD}$	$V_{PP}$ Deep Power-Down Current	1	0.2	5	$\mu A$	$RP\# = GND \pm 0.2V$
$I_{PPR}$	$V_{PP}$ Read and Standby Current	1	2	$\pm 50$	$\mu A$	$V_{PP} \leq V_{CC}$
$I_{PPW}$	$V_{PP}$ Program Current	1,4	15	40	mA	$V_{PP} = V_{PPH1}$ or $V_{PPH2}$ Program in Progress
			10	25	mA	$V_{PP} = V_{PPH3}$ (12V) Program in Progress
$I_{PPE}$	$V_{PP}$ Erase Current	1,4	13	25	mA	$V_{PP} = V_{PPH1}$ or $V_{PPH2}$ Erase in Progress
			8	25	mA	$V_{PP} = V_{PPH3}$ (12V) Erase in Progress
$I_{PPES}$	$V_{PP}$ Erase Suspend Current	1	50	200	$\mu A$	$V_{PP} = V_{PPH1}$ , $V_{PPH2}$ , or $V_{PPH3}$ Erase Suspend in Progress
$I_{PPWS}$	$V_{PP}$ Program Suspend Current	1	50	200	$\mu A$	$V_{PP} = V_{PPH1}$ , $V_{PPH2}$ , or $V_{PPH3}$ Program Suspend in Progress

**Table 13. DC Characteristics:  $V_{CCQ} = 1.8V-2.2V$  (Continued)**

Sym	Parameter	Notes	$V_{CC1}$ : 2.7V–2.85V $V_{CC2}$ : 2.7V–3.3V		Unit	Test Conditions
			Typ	Max		
$V_{IL}$	Input Low Voltage		-0.2	0.2	V	
$V_{IH}$	Input High Voltage		$V_{CCQ} - 0.2V$		V	
$V_{OL}$	Output Low Voltage		-0.10	0.10	V	$V_{CC} = V_{CCMin}$ $V_{CCQ} = V_{CCQMin}$ $I_{OL} = 100 \mu A$
$V_{OH}$	Output High Voltage		$V_{CCQ} - 0.1V$		V	$V_{CC} = V_{CCMin}$ $V_{CCQ} = V_{CCQMin}$ $I_{OH} = -100 \mu A$
$V_{PPLK}$	$V_{PP}$ Lock-Out Voltage	3	1.5		V	Complete Write Protection
$V_{PPH1}$	$V_{PP}$ during Prog./Erase Operations	3	2.7	2.85	V	
$V_{PPH2}$		3	2.7	3.3	V	
$V_{PPH3}$		3,6	11.4	12.6	V	
$V_{LKO1}$	$V_{CC}$ Program/Erase Lock Voltage		1.5		V	
$V_{LKO2}$	$V_{CCQ}$ Program/Erase Lock Voltage		1.2		V	

**NOTES:**

1. All currents are in RMS unless otherwise noted. Typical values at nominal  $V_{CC}$ ,  $T_A = +25^\circ C$ .
2.  $I_{CCES}$  and  $I_{CCWS}$  are specified with device de-selected. If device is read while in erase suspend, current draw is  $I_{CCR}$ . If the device is read while in program suspend, current draw is  $I_{CCR}$ .
3. Erases and Writes inhibited when  $V_{PP} \leq V_{PPLK}$ , and not guaranteed outside the valid  $V_{PP}$  ranges of  $V_{PPH1}$ ,  $V_{PPH2}$ , or  $V_{PPH3}$ .
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces  $I_{CCR}$  to approximately standby levels in static operation (CMOS inputs).
6. Applying  $V_{PP} = 11.4V-12.6V$  during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks.  $V_{PP}$  may be connected to 12V for a total of 80 hours maximum. See Section 3.4 for details.
7. Includes the sum of  $V_{CC}$  and  $V_{CCQ}$  current

**Table 14. Capacitance ( $T_A = 25^\circ C$ ,  $f = 1 MHz$ )**

Sym	Parameter	Notes	Typ	Max	Units	Conditions
$C_{IN}$	Input Capacitance	1	6	8	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	1	10	12	pF	$V_{OUT} = 0V$

**NOTE:**

1. Sampled, not 100% tested.

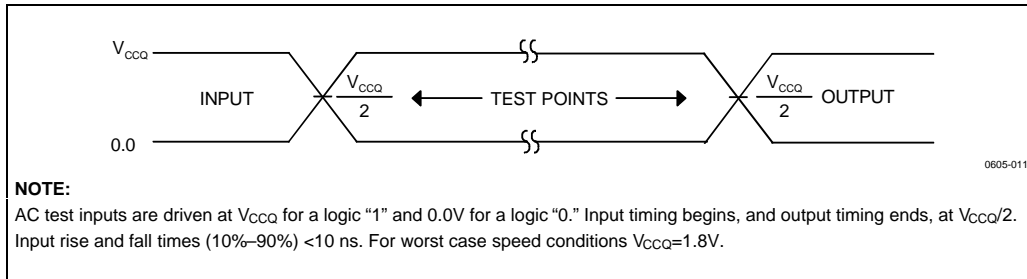


Figure 12. 1.8V–2.2V Input Range and Measurement Points

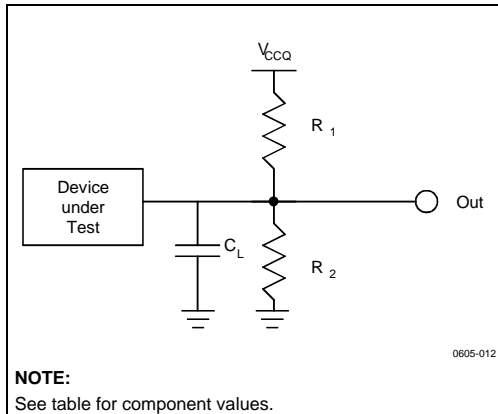


Figure 13. Test Configuration

Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	$C_L$ (pF)	$R_1$ ( $\Omega$ )	$R_2$ ( $\Omega$ )
1.8V Standard Test	50	16.7K	16.7K

**NOTE:**  
 $C_L$  includes jig capacitance.

### 7.0 AC CHARACTERISTICS

AC Characteristics are applicable to both  $V_{CCQ}$  ranges.

**Table 15. AC Characteristics: Read Operations (Extended Temperature)**

#	Symbol	Parameter	Load	$C_L = 50 \text{ pF}$				Units
			$V_{CC}$	2.7V–3.6V <sup>4</sup>				
			Prod	120 ns		150 ns		
			Notes	Min	Max	Min	Max	
R1	$t_{AVAV}$	Read Cycle Time		120		150		ns
R2	$t_{AVQV}$	Address to Output Delay			120		150	ns
R3	$t_{ELQV}$	CE# to Output Delay	2		120		150	ns
R4	$t_{GLQV}$	OE# to Output Delay	2		65		65	ns
R5	$t_{PHQV}$	RP# to Output Delay			600		600	ns
R6	$t_{ELQX}$	CE# to Output in Low Z	3	0		0		ns
R7	$t_{GLQX}$	OE# to Output in Low Z	3	0		0		ns
R8	$t_{EHQZ}$	CE# to Output in High Z	3		40		40	ns
R9	$t_{GHQZ}$	OE# to Output in High Z	3		40		40	ns
R10	$t_{OH}$	Output Hold from Address, CE#, or OE# Change, Whichever Occurs First	3	0		0		ns

**NOTES:**

1. See AC Input/Output Reference Waveform for timing measurements.
2. OE# may be delayed up to  $t_{ELQV} - t_{GLQV}$  after the falling edge of CE# without impact on  $t_{ELQV}$ .
3. Sampled, but not 100% tested.
4. See Test Configuration (Figures 11 and 13), 2.7V–3.6V and 1.8V–2.2V Standard Test component values.

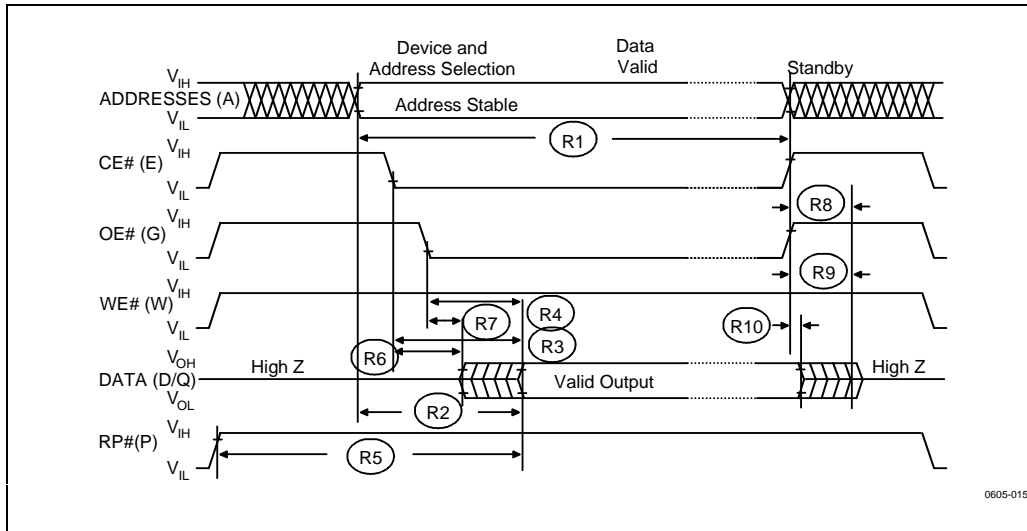


Figure 14. AC Waveform: Read Operations



**Table 16. AC Characteristics: Write Operations (Extended Temperature)<sup>1</sup>**

#	Symbol	Parameter	Load	50 pF				Units
			V <sub>CC</sub>	2.7V–3.6V <sup>5</sup>		2.7V–3.6V <sup>5</sup>		
			Prod	120 ns		150 ns		
			Notes	Min	Max	Min	Max	
W1	t <sub>PHWL</sub> t <sub>PHEL</sub>	RP# High Recovery to WE# (CE#) Going Low		600		600		ns
W2	t <sub>ELWL</sub> t <sub>WLEL</sub>	CE# (WE#) Setup to WE# (CE#) Going Low		0		0		ns
W3	t <sub>WLWH</sub> t <sub>ELEH</sub>	WE# (CE#) Pulse Width		90		90		ns
W4	t <sub>DVWH</sub> t <sub>DVEH</sub>	Data Setup to WE# (CE#) Going High	3	70		70		ns
W5	t <sub>AVWH</sub> t <sub>AVEH</sub>	Address Setup to WE# (CE#) Going High	2	90		90		ns
W6	t <sub>WHEH</sub> t <sub>EHWH</sub>	CE# (WE#) Hold Time from WE# (CE#) High		0		0		ns
W7	t <sub>WHDX</sub> t <sub>EHDX</sub>	Data Hold Time from WE# (CE#) High	3	0		0		ns
W8	t <sub>WHAX</sub> t <sub>EHAX</sub>	Address Hold Time from WE# (CE#) High	2	0		0		ns
W9	t <sub>WHWL</sub> t <sub>EHEL</sub>	WE# (CE#) Pulse Width High		30		30		ns
W10	t <sub>VPWH</sub> t <sub>VPEH</sub>	V <sub>PP</sub> Setup to WE# (CE#) Going High	4	200		200		ns
W11	t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid SRD	4	0		0		ns
	t <sub>LOCK</sub>	Block Unlock / Lock Delay	4, 6		200		200	ns

**NOTES:**

1. Read timing characteristics during program suspend and erase suspend are the same as during read-only operations. Refer to AC Characteristics during read mode.
2. Refer to command definition table for valid A<sub>N</sub> (Table 6).
3. Refer to command definition table for valid D<sub>N</sub> (Table 6).
4. Sampled, but not 100% tested.
5. See Test Configuration (Figure 11 and 13), 2.7V–3.6V and 1.8V–2.2V Standard Test component values.
6. Time t<sub>LOCK</sub> is required for successful locking and unlocking of all lockable blocks.

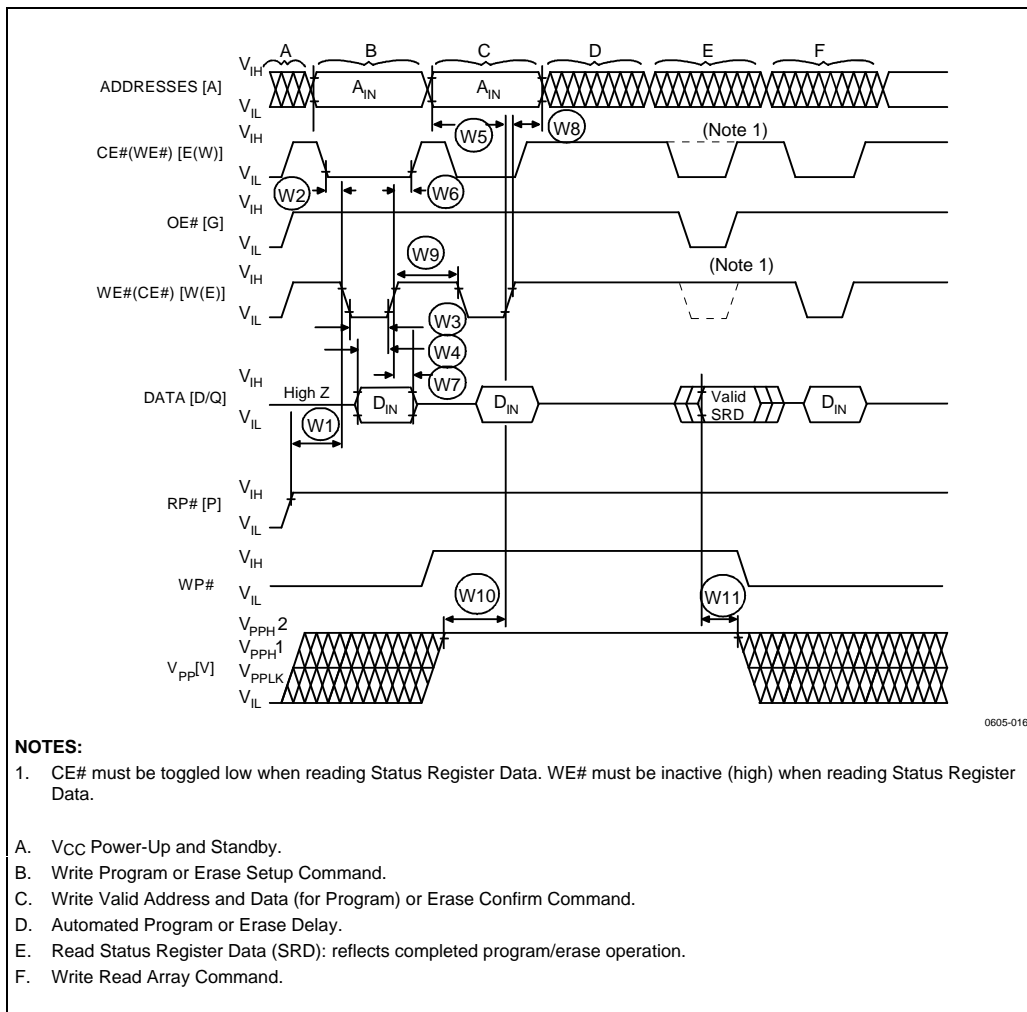


Figure 15. AC Waveform: Program and Erase Operations

7.1 Reset Operations

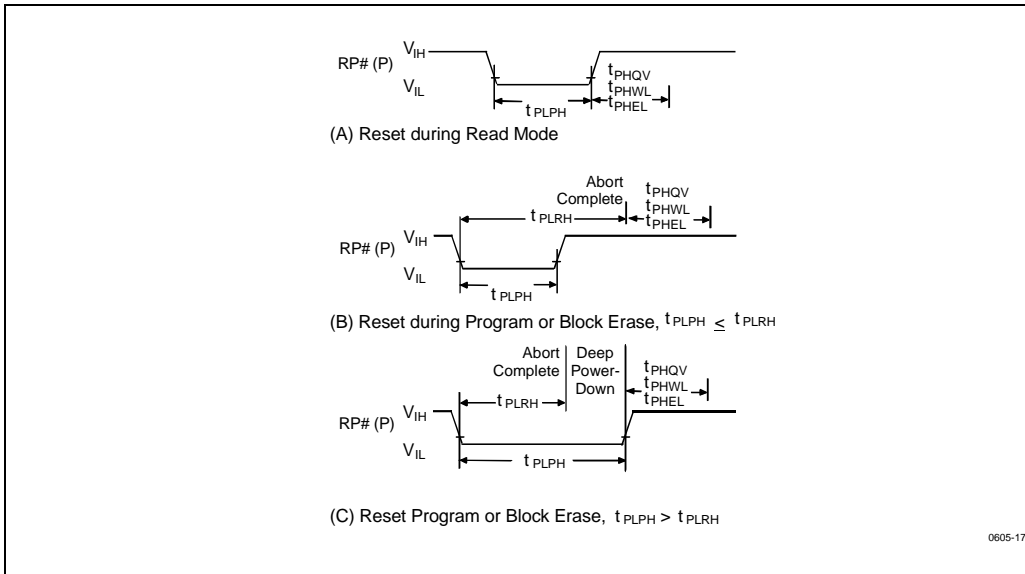


Figure 16. AC Waveform: Deep Power-Down/Reset Operation

Reset Specifications

Symbol	Parameter	Notes	V <sub>CC</sub> = 2.7–3.6V		Unit
			Min	Max	
$t_{PLPH}$	RP# Low to Reset during Read (If RP# is tied to V <sub>CC</sub> , this specification is not applicable)	1,3	100		ns
$t_{PLRH}$	RP# Low to Reset during Block Erase or Program	2,3		22	μs

NOTES:

1. If  $t_{PLPH}$  is < 100 ns the device may still RESET but this is not guaranteed.
2. If RP# is asserted while a block erase or byte program operation is not executing, the reset will complete within 100 ns.
3. Sampled but not 100% tested.

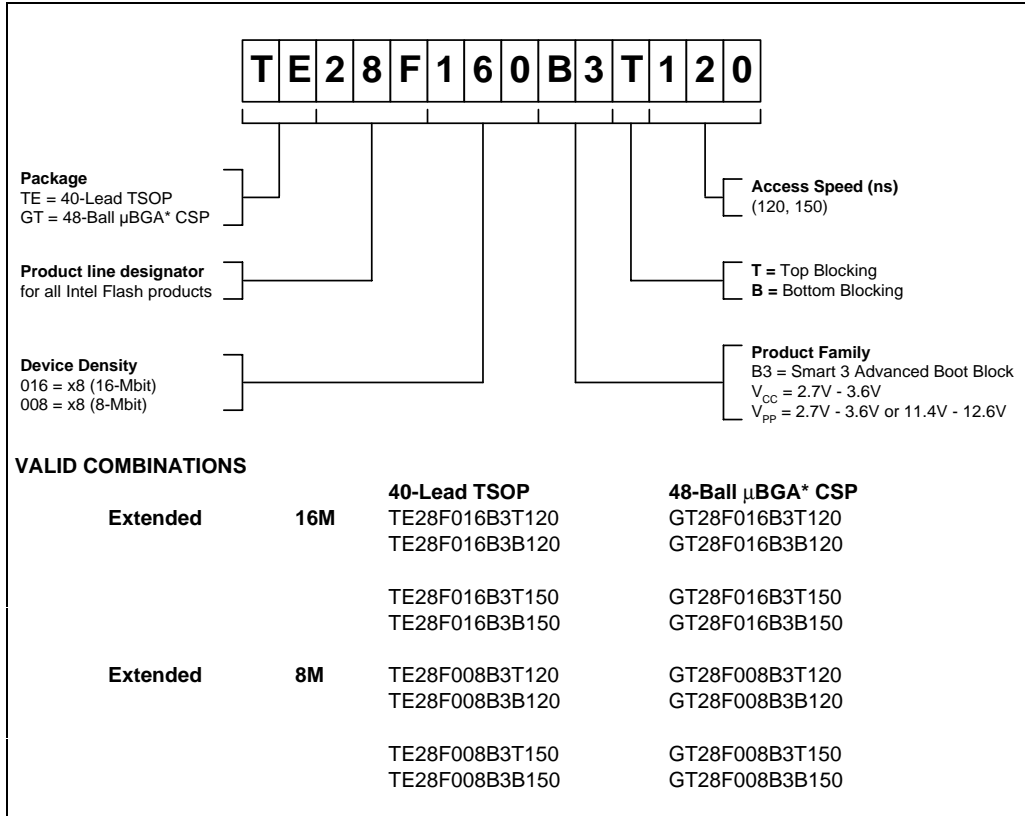
Table 17. Erase and Program Timings

Sym	Parameter	Notes	V <sub>PP</sub> = 2.7V		V <sub>PP</sub> = 12V		Unit
			Typ <sup>1</sup>	Max <sup>3</sup>	Typ <sup>1</sup>	Max <sup>3</sup>	
t <sub>BWPB</sub>	Block Program Time (Parameter)	2	.16	.48	.08	.24	sec
t <sub>BWMB</sub>	Block Program Time (Main)	2	1.23	3.69	.58	1.74	sec
t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Program Time	2	17	165	8	185	μs
t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Block Erase Time (Parameter)	2	1	5.0	0.8	4.8	sec
t <sub>WHQV3</sub> t <sub>EHQV3</sub>	Block Erase Time (Main)	2	1.8	8.0	1.1	7.0	sec
t <sub>WHRH1</sub> t <sub>EHRH1</sub>	Program Suspend Latency	3	5	10	5	10	μs
t <sub>WHRH2</sub> t <sub>EHRH2</sub>	Erase Suspend Latency	3	5	20	6	12	μs

**NOTES:**

1. Typical values measured at T<sub>A</sub> = +25°C and nominal voltages.
2. Excludes external system-level overhead.
3. Sampled but not 100% tested.

## APPENDIX A ORDERING INFORMATION



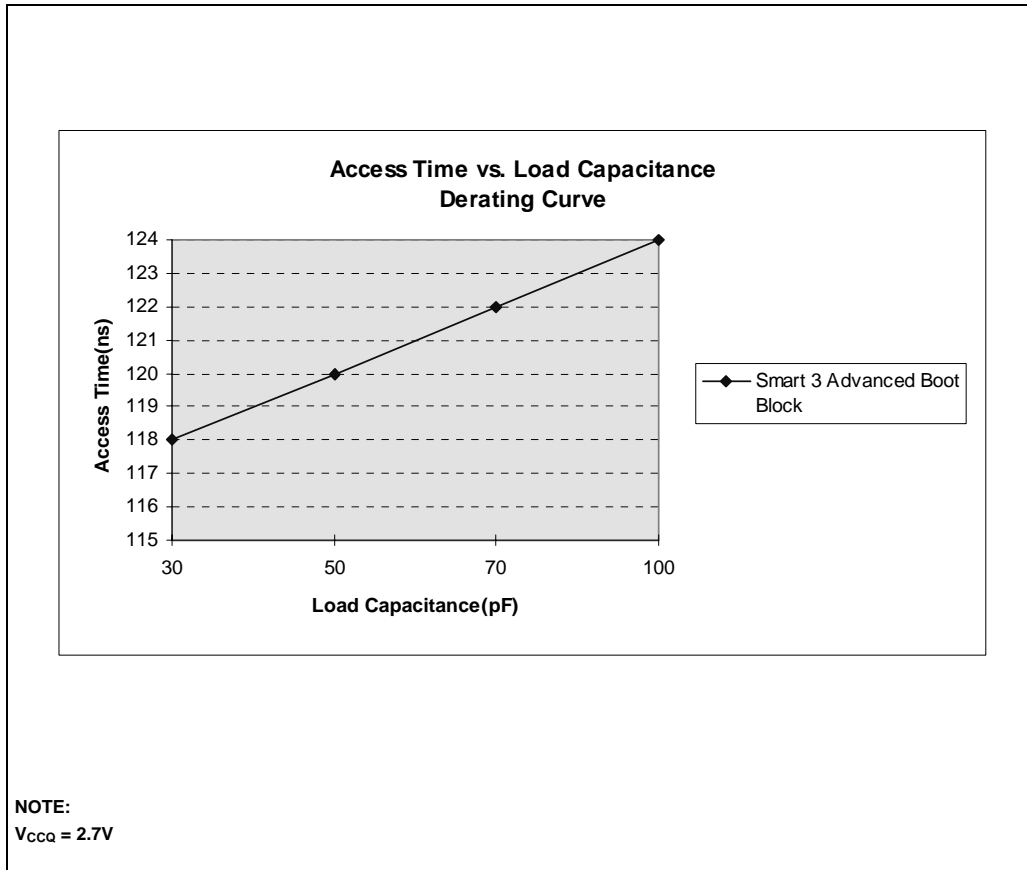


## APPENDIX B WRITE STATE MACHINE CURRENT/NEXT STATES

Current State	SR.7	Data When Read	Command Input (and Next State)								
			Read Array (FFH)	Program Setup (40/10H)	Erase Setup (20H)	Erase Confirm (D0H)	Program / Erase Susp. (B0H)	Program / Erase Resume (D0)	Read Status (70H)	Clear Status (50H)	Read ID (90H)
Read Array	"1"	Array	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Program Setup	"1"	Status	Pgm. <sup>1</sup>	Program (Command input = Data to be programmed)							
Program (Not Comp.)	"0"	Status	Program			Pgm Susp. to Status	Program				
Program (Complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Program Suspend to Status	"1"	Status	Prog. Susp. to Array	Program Suspend to Array		Program	Program Susp. to Array	Program	Prog. Susp. to Status	Program Suspend to Array	
Program Suspend to Array	"1"	Array	Prog. Susp. to Array	Program Suspend to Array		Program	Program Susp. to Array	Program	Prog. Susp. to Status	Prog. Susp. to Array	Prog. Susp. to Array
Erase Setup	"1"	Status	Erase Command Error			Erase	Erase Cmd. Err.	Erase	Erase Command Error		
Erase Cmd. Error	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase (Not Comp)	"0"	Status	Erase			Ers. Susp. to Status	Erase				
Erase (Complete)	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Erase Suspend to Status	"1"	Status	Erase Susp. to Array	Program Setup	Erase Susp. to Array	Erase	Erase Susp. to Array	Erase	Erase Susp. to Status	Erase Suspend to Array	
Erase. Susp. to Array	"1"	Array	Erase Susp. to Array	Program Setup	Erase Susp. to Array	Erase	Erase Susp. to Array	Erase	Erase Susp. to Status	Erase Suspend to Array	
Read Status	"1"	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier
Read Identifier	"1"	ID	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array	Read Identifier

1. You cannot program "1"s to the flash. Writing FFH following the Program Setup will initiate the internal program algorithm of the WSM. Although the algorithm will execute, array data is not changed. The WSM returns to read status mode without reporting any error. Assuming  $V_{PP} > V_{PPLK}$  writing a second FFH while in read status mode will return the flash to read array mode.

## APPENDIX C ACCESS TIME VS. CAPACITIVE LOAD ( $t_{AVQV}$ VS. $C_L$ )



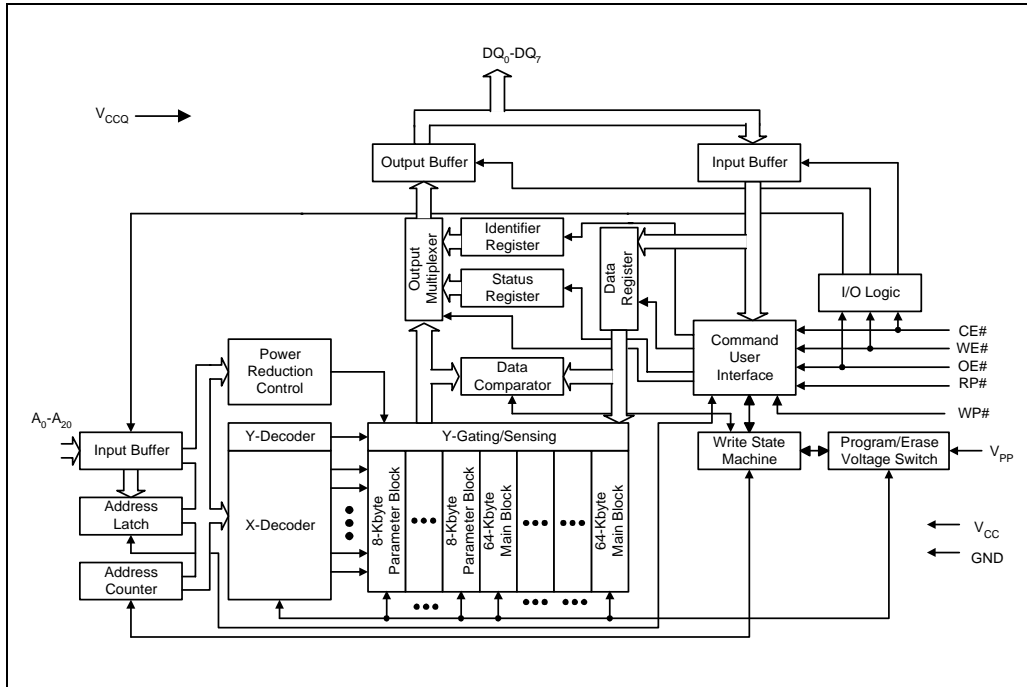
This chart shows a derating curve for device access time with respect to capacitive load. The value in the DC characteristics section of the specification corresponds to  $C_L = 50$  pF.

**NOTE:**

1. Sampled, but not 100% tested

**PRELIMINARY**

## APPENDIX D ARCHITECTURE BLOCK DIAGRAM







## APPENDIX E ADDITIONAL INFORMATION(1,2)

Order Number	Document/Tool
210830	<i>1997 Flash Memory Databook</i>
290580	<i>Smart 3 Advanced Boot Block Word-Wide 4-Mbit (256K x 16), 8-Mbit (512K x 16), 16-Mbit (1024K x 16) Flash Memory Family Datasheet</i>
292172	<i>AP-617 Additional Flash Data Protection Using V<sub>PP</sub>, RP# and WP#</i>

**NOTE:**

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at <http://www.Intel.com> for technical documentation and tools.