



PRELIMINARY

## INTEL® StrataFlash™ MEMORY TECHNOLOGY 32 AND 64 MBIT

28F320J5 and 28F640J5

- **High-Density Symmetrically-Blocked Architecture**
  - 64 128-Kbyte Erase Blocks (64 M)
  - 32 128-Kbyte Erase Blocks (32 M)
- **4.5 V–5.5 V V<sub>CC</sub> Operation**
  - 2.7 V–3.6 V and 4.5 V–5.5 V I/O Capable
- **Configurable x8 or x16 I/O**
- **100 ns Read Access Time (32 M)  
150 ns Read Access Time (64 M)**
- **Enhanced Data Protection Features**
  - Absolute Protection with V<sub>PEN</sub> = GND
  - Flexible Block Locking
  - Block Erase/Program Lockout during Power Transitions
- **Industry-Standard Packaging**
  - µBGA\* Package (64 M), SSOP and TSOP Packages (32 M)
- **Cross-Compatible Command Support**
  - Intel Basic Command Set
  - Common Flash Interface
  - Scaleable Command Set
- **32-Byte Write Buffer**
  - 6.3 µs per Byte Effective Programming Time
- **6,400,000 Total Erase Cycles (64 M)  
3,200,000 Total Erase Cycles (32 M)**
  - 100,000 Erase Cycles per Block
- **Automation Suspend Options**
  - Block Erase Suspend to Read
  - Block Erase Suspend to Program
- **System Performance Enhancements**
  - STS Status Output
- **Expanded Temperature Operation**
  - -20 °C to +70 °C
- **Intel® StrataFlash™ Memory Flash Technology**

Capitalizing on two-bit-per-cell technology, Intel® StrataFlash™ memory products provide 2X the bits in 1X the space. Offered in 64-Mbit (8-Mbyte) and 32-Mbit (4-Mbyte) densities, Intel StrataFlash memory devices are the first to bring reliable, two-bit-per-cell storage technology to the flash market.

Intel StrataFlash memory benefits include: more density in less space, lowest cost-per-bit NOR devices, support for code and data storage, and easy migration to future devices.

Using the same NOR-based ETOX™ technology as Intel's one-bit-per-cell products, Intel StrataFlash memory devices take advantage of 400 million units of manufacturing experience since 1988. As a result, Intel StrataFlash components are ideal for code or data applications where high density and low cost are required. Examples include networking, telecommunications, audio recording, and digital imaging.

By applying FlashFile™ memory family pinouts, Intel StrataFlash memory components allow easy design migrations from existing 28F016SA/SV, 28F032SA, and Word-Wide FlashFile memory devices (28F160S5 and 28F320S5).

Intel StrataFlash memory components deliver a new generation of forward-compatible software support. By using the Common Flash Interface (CFI) and the Scaleable Command Set (SCS), customers can take advantage of density upgrades and optimized write capabilities of future Intel StrataFlash memory devices.

Manufactured on Intel's 0.4 micron ETOX™ V process technology, Intel StrataFlash memory provides the highest levels of quality and reliability.

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

The 28F320J5 and 28F640J4 may contain design defects or errors known as errata. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation  
P.O. Box 5937  
Denver, CO 8021-9808

or call 1-800-548-4725  
or visit Intel's website at <http://www.intel.com>

COPYRIGHT © INTEL CORPORATION 1997, 1998

CG-041493

\*Third-party brands and names are the property of their respective owners.





## CONTENTS

	PAGE		PAGE
<b>1.0 PRODUCT OVERVIEW</b> .....	<b>5</b>	4.8 Write to Buffer Command .....	28
<b>2.0 PRINCIPLES OF OPERATION</b> .....	<b>11</b>	4.9 Byte/Word Program Commands .....	28
2.1 Data Protection .....	12	4.10 Configuration Command .....	29
<b>3.0 BUS OPERATION</b> .....	<b>12</b>	4.11 Set Block and Master Lock-Bit Commands .....	29
3.1 Read .....	13	4.12 Clear Block Lock-Bits Command .....	30
3.2 Output Disable .....	13	<b>5.0 DESIGN CONSIDERATIONS</b> .....	<b>40</b>
3.3 Standby .....	13	5.1 Three-Line Output Control .....	40
3.4 Reset/Power-Down .....	13	5.2 STS and Block Erase, Program, and Lock- Bit Configuration Polling .....	40
3.5 Read Query .....	14	5.3 Power Supply Decoupling .....	40
3.6 Read Identifier Codes .....	14	5.4 V <sub>CC</sub> , V <sub>PEN</sub> , RP# Transitions .....	40
3.7 Write .....	14	5.5 Power-Up/Down Protection .....	41
<b>4.0 COMMAND DEFINITIONS</b> .....	<b>14</b>	5.6 Power Dissipation .....	41
4.1 Read Array Command .....	18	<b>6.0 ELECTRICAL SPECIFICATIONS</b> .....	<b>42</b>
4.2 Read Query Mode Command .....	18	6.1 Absolute Maximum Ratings .....	42
4.2.1 Query Structure Output .....	18	6.2 Operating Conditions .....	42
4.2.2 Query Structure Overview .....	20	6.3 Capacitance .....	42
4.2.3 Block Status Register .....	21	6.4 DC Characteristics .....	43
4.2.4 CFI Query Identification String .....	22	6.5 AC Characteristics—Read-Only Operations .....	46
4.2.5 System Interface Information .....	23	6.6 AC Characteristics— Write Operations .....	48
4.2.6 Device Geometry Definition .....	24	6.7 Block Erase, Program, and Lock-Bit Configuration Performance .....	51
4.2.7 Primary-Vendor Specific Extended Query Table .....	25	<b>7.0 ORDERING INFORMATION</b> .....	<b>52</b>
4.3 Read Identifier Codes Command .....	26	<b>8.0 ADDITIONAL INFORMATION</b> .....	<b>53</b>
4.4 Read Status Register Command .....	27		
4.5 Clear Status Register Command .....	27		
4.6 Block Erase Command .....	27		
4.7 Block Erase Suspend Command .....	27		

## REVISION HISTORY

Date of Revision	Version	Description
09/01/97	-001	Original Version
09/17/97	-002	Modifications made to cover sheet
12/01/97	-003	V <sub>CC</sub> /GND Pins Converted to No Connects specification change added I <sub>CCS</sub> , I <sub>CCD</sub> , I <sub>CCW</sub> , and I <sub>CCF</sub> specification change added Order Codes specification change added
1/31/98	-004	The $\mu$ BGA* chip-scale package in Figure 2 was changed to a 52-ball package and appropriate documentation added. The 64-Mb $\mu$ BGA package dimensions were changed in Figure 2. Changed Figure 4 to read SSOP instead of TSOP.
3/23/98	-005	32-Mbit Intel StrataFlash memory read access time added. The number of block erase cycles was changed. The write buffer program time was changed. The operating temperature was changed. A read parameter was added. Several program, erase, and lock-bit specifications were changed. Minor documentation changes were made as well. Datasheet designation changed from Advance Information to Preliminary.
7/13/98	-006	Intel StrataFlash memory 32-Mb $\mu$ BGA package removed. t <sub>EH</sub> read specification reduced. Table 4 was modified. The <i>Ordering Information</i> was updated.

## 1.0 PRODUCT OVERVIEW

The Intel® StrataFlash™ memory family contains high-density memories organized as 8 Mbytes or 4 Mwords (64-Mbit) and 4 Mbytes or 2 Mwords (32-Mbit). These devices can be accessed as 8- or 16-bit words. The 64-Mbit device is organized as sixty-four 128-Kbyte (131,072 bytes) erase blocks while the 32-Mbit device contains thirty-two 128-Kbyte erase blocks. Blocks are selectively and individually lockable and unlockable in-system. See the memory map in Figure 5.

A Common Flash Interface (CFI) permits software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

Scaleable Command Set (SCS) allows a single, simple software driver in all host systems to work with all SCS-compliant flash memory devices, independent of system-level packaging (e.g., memory card, SIMM, or direct-to-board placement). Additionally, SCS provides the highest system/device data transfer rates and minimizes device and system-level implementation costs.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, program, and lock-bit configuration operations.

A block erase operation erases one of the device's 128-Kbyte blocks typically within one second— independent of other blocks. Each block can be independently erased 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or program data from any other block.

Each device incorporates a Write Buffer of 32 bytes (16 words) to allow optimum programming performance. By using the Write Buffer, data is programmed in buffer increments. This feature can improve system program performance by up to 20 times over non Write Buffer writes.

Individual block locking uses a combination of bits, block lock-bits and a master lock-bit, to lock and unlock blocks. Block lock-bits gate block erase and program operations while the master lock-bit gates block lock-bit modification. Three lock-bit configuration operations set and clear lock-bits (Set Block Lock-Bit, Set Master Lock-Bit, and Clear Block Lock-Bits commands).

The status register indicates when the WSM's block erase, program, or lock-bit configuration operation is finished.

The STS (STATUS) output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status indication using STS minimizes both CPU overhead and system power consumption. When configured in level mode (default mode), it acts as a RY/BY# pin. When low, STS indicates that the WSM is performing a block erase, program, or lock-bit configuration. STS-high indicates that the WSM is ready for a new command, block erase is suspended (and programming is inactive), or the device is in reset/power-down mode. Additionally, the configuration command allows the STS pin to be configured to pulse on completion of programming and/or block erases.

Three CE pins are used to enable and disable the device. A unique CE logic design (see Table 2, *Chip Enable Truth Table*) reduces decoder logic typically required for multi-chip designs. External logic is not required when designing a single chip, a dual chip, or a 4-chip miniature card or SIMM module.

The BYTE# pin allows either x8 or x16 read/writes to the device. BYTE# at logic low selects 8-bit mode; address  $A_0$  selects between the low byte and high byte. BYTE# at logic high enables 16-bit operation; address  $A_1$  becomes the lowest order address and address  $A_0$  is not used (don't care). A device block diagram is shown in Figure 1.

When the device is disabled (see Table 2, *Chip Enable Truth Table*) and the RP# pin is at  $V_{CC}$ , the standby mode is enabled. When the RP# pin is at GND, a further power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time ( $t_{PHQV}$ ) is required from RP# switching high until outputs



Table 1. Lead Descriptions

Symbol	Type	Name and Function
A <sub>0</sub>	INPUT	<b>BYTE-SELECT ADDRESS:</b> Selects between high and low byte when the device is in x8 mode. This address is latched during a x8 program cycle. Not used in x16 mode (i.e., the A <sub>0</sub> input buffer is turned off when BYTE# is high).
A <sub>1</sub> –A <sub>22</sub>	INPUT	<b>ADDRESS INPUTS:</b> Inputs for addresses during read and program operations. Addresses are internally latched during a program cycle. 32-Mbit: A <sub>0</sub> –A <sub>21</sub> 64-Mbit: A <sub>0</sub> –A <sub>22</sub>
DQ <sub>0</sub> –DQ <sub>7</sub>	INPUT/ OUTPUT	<b>LOW-BYTE DATA BUS:</b> Inputs data during buffer writes and programming, and inputs commands during Command User Interface (CUI) writes. Outputs array, query, identifier, or status data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled. Outputs DQ <sub>6</sub> –DQ <sub>0</sub> are also floated when the Write State Machine (WSM) is busy. Check SR.7 (Status Register bit 7) to determine WSM status.
DQ <sub>8</sub> –DQ <sub>15</sub>	INPUT/ OUTPUT	<b>HIGH-BYTE DATA BUS:</b> Inputs data during x16 buffer writes and programming operations. Outputs array, query, or identifier data in the appropriate read mode; not used for Status Register reads. Floated when the chip is de-selected, the outputs are disabled, or the WSM is busy.
CE <sub>0</sub> , CE <sub>1</sub> , CE <sub>2</sub>	INPUT	<b>CHIP ENABLES:</b> Activates the device's control logic, input buffers, decoders, and sense amplifiers. When the device is de-selected (see Table 2, <i>Chip Enable Truth Table</i> ), power reduces to standby levels.  All timing specifications are the same for these three signals. Device selection occurs with the first edge of CE <sub>0</sub> , CE <sub>1</sub> , or CE <sub>2</sub> that enables the device. Device deselection occurs with the first edge of CE <sub>0</sub> , CE <sub>1</sub> , or CE <sub>2</sub> that disables the device (see Table 2, <i>Chip Enable Truth Table</i> ).
RP#	INPUT	<b>RESET/ POWER-DOWN:</b> Resets internal automation and puts the device in power-down mode. RP#-high enables normal operation. Exit from reset sets the device to read array mode. When driven low, RP# inhibits write operations which provides data protection during power transitions.  RP# at V <sub>HH</sub> enables master lock-bit setting and block lock-bits configuration when the master lock-bit is set. RP# = V <sub>HH</sub> overrides block lock-bits thereby enabling block erase and programming operations to locked memory blocks. Do not permanently connect RP# to V <sub>HH</sub> .
OE#	INPUT	<b>OUTPUT ENABLE:</b> Activates the device's outputs through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	<b>WRITE ENABLE:</b> Controls writes to the Command User Interface, the Write Buffer, and array blocks. WE# is active low. Addresses and data are latched on the rising edge of the WE# pulse.
STS	OPEN DRAIN OUTPUT	<b>STATUS:</b> Indicates the status of the internal state machine. When configured in level mode (default mode), it acts as a RY/BY# pin. When configured in one of its pulse modes, it can pulse to indicate program and/or erase completion. For alternate configurations of the STATUS pin, see the Configurations command. Tie STS to V <sub>CCQ</sub> with a pull-up resistor.

Table 1. Lead Descriptions (Continued)

Symbol	Type	Name and Function
BYTE#	INPUT	<b>BYTE ENABLE:</b> BYTE# low places the device in x8 mode. All data is then input or output on DQ <sub>0</sub> –DQ <sub>7</sub> , while DQ <sub>8</sub> –DQ <sub>15</sub> float. Address A <sub>0</sub> selects between the high and low byte. BYTE# high places the device in x16 mode, and turns off the A <sub>0</sub> input buffer. Address A <sub>1</sub> then becomes the lowest order address.
V <sub>PEN</sub>	INPUT	<b>ERASE / PROGRAM / BLOCK LOCK ENABLE:</b> For erasing array blocks, programming data, or configuring lock-bits.  With $V_{PEN} \leq V_{PENLK}$ , memory contents cannot be altered.
V <sub>CC</sub>	SUPPLY	<b>DEVICE POWER SUPPLY:</b> With $V_{CC} \leq V_{LKO}$ , all write attempts to the flash memory are inhibited.
V <sub>CCQ</sub>	OUTPUT BUFFER SUPPLY	<b>OUTPUT BUFFER POWER SUPPLY:</b> This voltage controls the device's output voltages. To obtain output voltages compatible with system data bus voltages, connect V <sub>CCQ</sub> to the system supply voltage.
GND	SUPPLY	<b>GROUND:</b> Do not float any ground pins.
NC		<b>NO CONNECT:</b> Lead is not internally connected; it may be driven or floated.



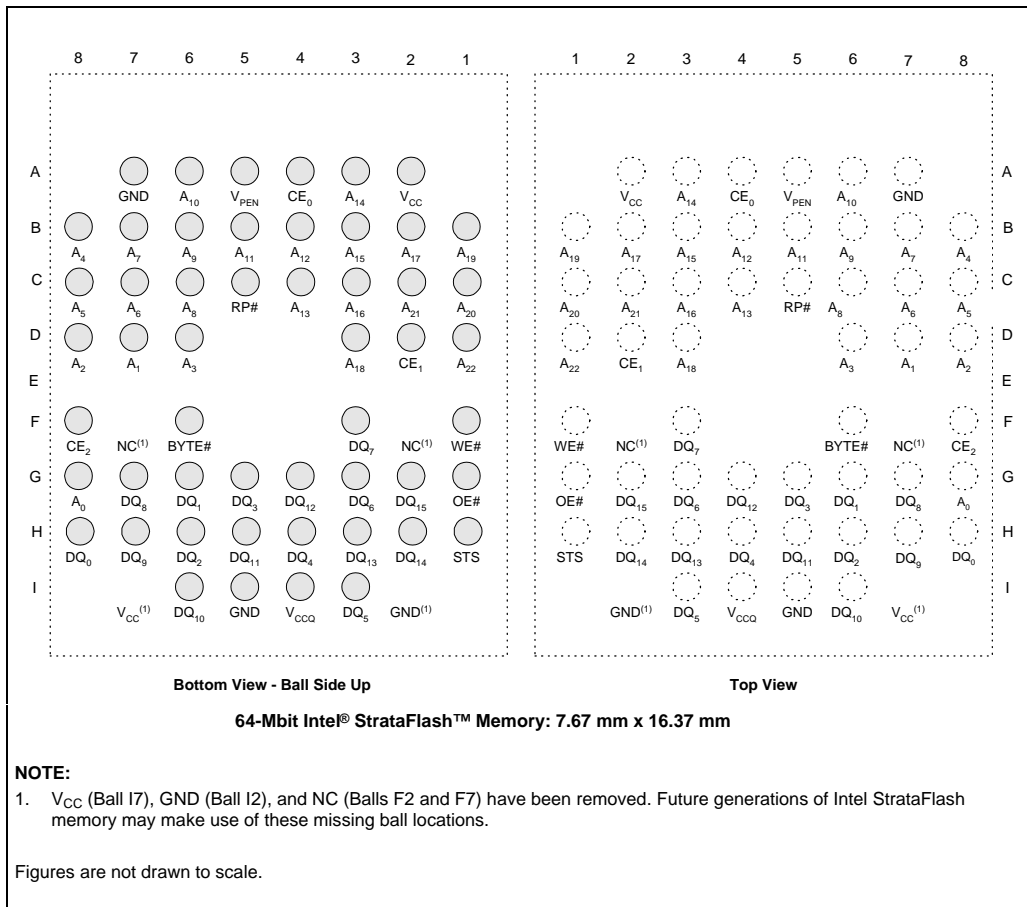


Figure 2. μBGA\* Package (64 Mbit)

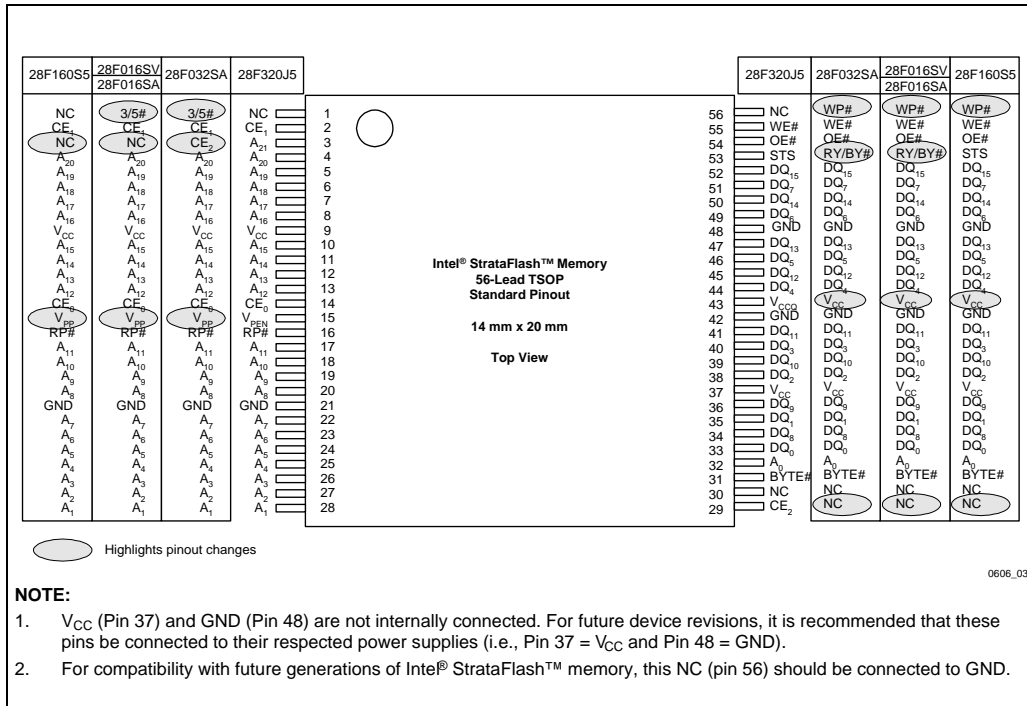


Figure 3. TSOP Lead Configuration (32 Mbit)

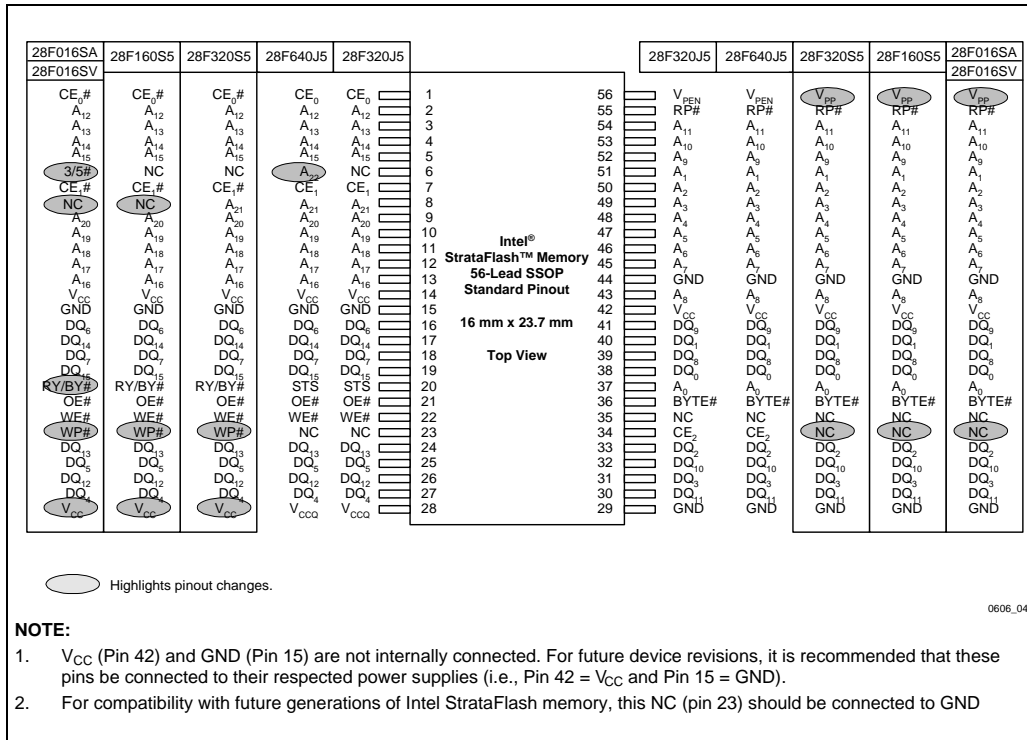


Figure 4. SSOP Lead Configuration (64 Mbit and 32 Mbit)

## 2.0 PRINCIPLES OF OPERATION

The Intel StrataFlash memory devices include an on-chip WSM to manage block erase, program, and lock-bit configuration functions. It allows for 100% TTL-level control inputs, fixed power supplies during block erasure, program, lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from reset/power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allows array read, standby, and output disable operations.

Read array, status register, query, and identifier codes can be accessed through the CUI (Command User Interface) independent of the V<sub>PEN</sub> voltage.

V<sub>PENH</sub> on V<sub>PEN</sub> enables successful block erasure, programming, and lock-bit configuration. All functions associated with altering memory contents—block erase, program, lock-bit configuration—are accessed via the CUI and verified through the status register.

Commands are written using standard micro-processor write timings. The CUI contents serve as input to the WSM, which controls the block erase, program, and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latched during program cycles.

Interface software that initiates and polls progress of block erase, program, and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or program data from/to any other block.

### 2.1 Data Protection

Depending on the application, the system designer may choose to make the V<sub>PEN</sub> switchable (available only when memory block erases, programs, or lock-bit configurations are required) or hardwired to V<sub>PENH</sub>. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When V<sub>PEN</sub> ≤ V<sub>PENLK</sub>, memory contents cannot be altered. The CUI's two-step block erase, byte/word program, and lock-bit configuration command sequences provide protection from unwanted operations even when V<sub>PENH</sub> is applied to V<sub>PEN</sub>. All program functions are disabled when V<sub>CC</sub> is below the write lockout voltage V<sub>LKO</sub> or when RP# is V<sub>IL</sub>. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating erase and program operations.

### 3.0 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

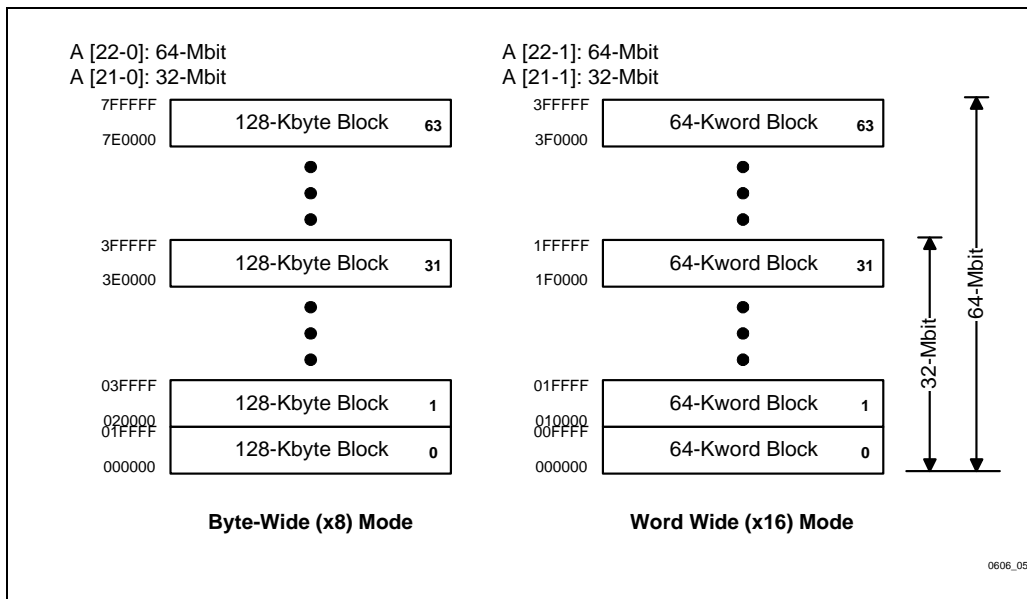


Figure 5. Memory Map

**Table 2. Chip Enable Truth Table<sup>(1,2)</sup>**

CE <sub>2</sub>	CE <sub>1</sub>	CE <sub>0</sub>	DEVICE
V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	Enabled
V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Disabled
V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Disabled
V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Disabled
V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	Enabled
V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Enabled
V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Enabled
V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Disabled

**NOTE:**

1. See Application Note AP-647 *Intel StrataFlash™ Memory Design Guide* for typical CE configurations.
2. For single-chip applications CE<sub>2</sub> and CE<sub>1</sub> can be strapped to GND.

### 3.1 Read

Information can be read from any block, query, identifier codes, or status register independent of the V<sub>PEN</sub> voltage. RP# can be at either V<sub>IH</sub> or V<sub>HH</sub>.

Upon initial device power-up or after exit from reset/power-down mode, the device automatically resets to read array mode. Otherwise, write the appropriate read mode command (Read Array, Read Query, Read Identifier Codes, or Read Status Register) to the CUI. Six control pins dictate the data flow in and out of the component: CE<sub>0</sub>, CE<sub>1</sub>, CE<sub>2</sub>, OE#, WE#, and RP#. The device must be enabled (see Table 2, *Chip Enable Truth Table*), and OE# must be driven active to obtain data at the outputs. CE<sub>0</sub>, CE<sub>1</sub>, and CE<sub>2</sub> are the device selection controls and, when enabled (see Table 2, *Chip Enable Truth Table*), select the memory device. OE# is the data output (DQ<sub>0</sub>–DQ<sub>15</sub>) control and, when active, drives the selected memory data onto the I/O bus. WE# must be at V<sub>IH</sub>.

### 3.2 Output Disable

With OE# at a logic-high level (V<sub>IH</sub>), the device outputs are disabled. Output pins DQ<sub>0</sub>–DQ<sub>15</sub> are placed in a high-impedance state.

### 3.3 Standby

CE<sub>0</sub>, CE<sub>1</sub>, and CE<sub>2</sub> can disable the device (see Table 2, *Chip Enable Truth Table*) and place it in standby mode which substantially reduces device power consumption. DQ<sub>0</sub>–DQ<sub>15</sub> outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, program, or lock-bit configuration, the WSM continues functioning, and consuming active power until the operation completes.

### 3.4 Reset/Power-Down

RP# at V<sub>IL</sub> initiates the reset/power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state, and turns off numerous internal circuits. RP# must be held low for a minimum of t<sub>PLPH</sub>. Time t<sub>PHQV</sub> is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, program, or lock-bit configuration modes, RP#-low will abort the operation. In default mode, STS transitions low and remains low for a maximum time of t<sub>PLPH</sub> + t<sub>PHRH</sub> until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after a program or partially altered after an erase or lock-bit configuration. Time t<sub>PHWL</sub> is required after RP# goes to logic-high (V<sub>IH</sub>) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, program, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper initialization may not occur because the flash memory may be providing status information instead of array data. Intel's flash memories allow proper initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.



### 3.5 Read Query

The read query operation outputs block status information, CFI (Common Flash Interface) ID string, system interface information, device geometry information, and Intel-specific extended query information.

### 3.6 Read Identifier Codes

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and the master lock configuration code (see Figure 6). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and master lock-bit setting.

### 3.7 Write

Writing commands to the CUI enables reading of device data, query, identifier codes, inspection and clearing of the status register, and, when  $V_{PEN} = V_{PENH}$ , block erasure, program, and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Byte/Word Program command requires the command and address of the location to be written. Set Master and Block Lock-Bit commands require the command and address within the device (Master Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when the device is enabled and  $WE\#$  is active. The address and data needed to execute a command are latched on the rising edge of  $WE\#$  or the first edge of  $CE_0$ ,  $CE_1$ , or  $CE_2$  that disables the device (see Table 2, *Chip Enable Truth Table*). Standard microprocessor write timings are used.

### 4.0 COMMAND DEFINITIONS

When the  $V_{PEN}$  voltage  $\leq V_{PENLK}$ , only read operations from the status register, query, identifier codes, or blocks are enabled. Placing  $V_{PENH}$  on

$V_{PEN}$  additionally enables block erase, program, and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

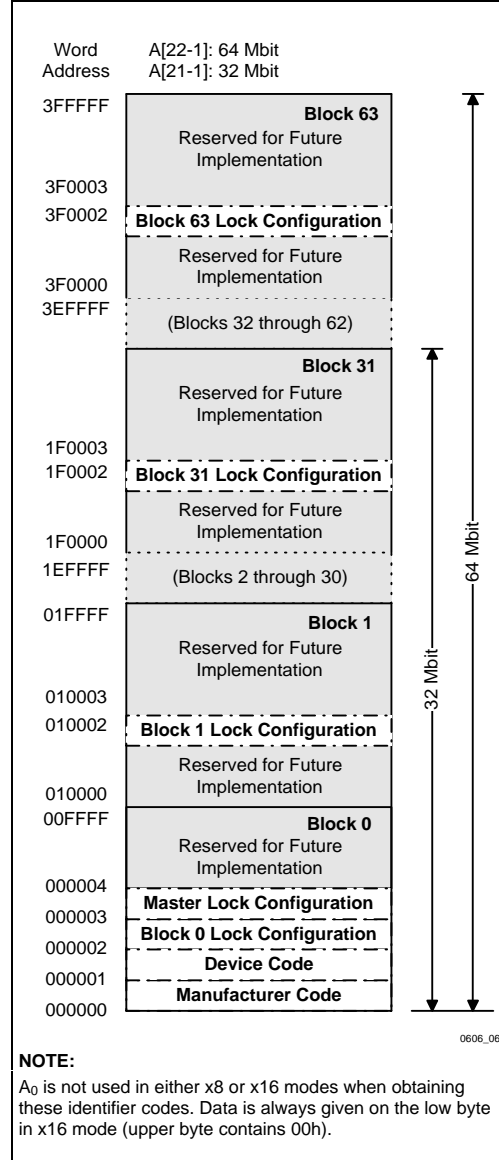


Figure 6. Device Identifier Code Memory Map

PRELIMINARY

**Table 3. Bus Operations**

Mode	Notes	RP#	CE <sub>0,1,2</sub> ( <sup>10</sup> )	OE#( <sup>11</sup> )	WE#( <sup>11</sup> )	Address	V <sub>PEN</sub>	DQ <sup>(8)</sup>	STS (default mode)
Read Array	1,2,3	V <sub>IH</sub> or V <sub>HH</sub>	Enabled	V <sub>IL</sub>	V <sub>IH</sub>	X	X	D <sub>OUT</sub>	High Z <sup>(9)</sup>
Output Disable		V <sub>IH</sub> or V <sub>HH</sub>	Enabled	V <sub>IH</sub>	V <sub>IH</sub>	X	X	High Z	X
Standby		V <sub>IH</sub> or V <sub>HH</sub>	Disabled	X	X	X	X	High Z	X
Reset/Power-Down Mode		V <sub>IL</sub>	X	X	X	X	X	High Z	High Z <sup>(9)</sup>
Read Identifier Codes		V <sub>IH</sub> or V <sub>HH</sub>	Enabled	V <sub>IL</sub>	V <sub>IH</sub>	See Figure 6	X	Note 4	High Z <sup>(9)</sup>
Read Query		V <sub>IH</sub> or V <sub>HH</sub>	Enabled	V <sub>IL</sub>	V <sub>IH</sub>	See Table 7	X	Note 5	High Z <sup>(9)</sup>
Read Status (WSM off)		V <sub>IH</sub> or V <sub>HH</sub>	Enabled	V <sub>IL</sub>	V <sub>IH</sub>	X	X	D <sub>OUT</sub>	
Read Status (WSM on)		V <sub>IH</sub> or V <sub>HH</sub>	Enabled	V <sub>IL</sub>	V <sub>IH</sub>	X	V <sub>PENH</sub>	DQ <sub>7</sub> = D <sub>OUT</sub> DQ <sub>45-8</sub> = High Z DQ <sub>6-0</sub> = High Z	
Write	3,6,7	V <sub>IH</sub> or V <sub>HH</sub>	Enabled	V <sub>IH</sub>	V <sub>IL</sub>	X	X	D <sub>IN</sub>	X

**NOTES:**

1. Refer to *DC Characteristics*. When  $V_{PEN} \leq V_{PENLK}$ , memory contents can be read, but not altered.
2. X can be V<sub>IL</sub> or V<sub>IH</sub> for control and address pins, and V<sub>PENLK</sub> or V<sub>PENH</sub> for V<sub>PEN</sub>. See *DC Characteristics* for V<sub>PENLK</sub> and V<sub>PENH</sub> voltages.
3. In default mode, STS is V<sub>OL</sub> when the WSM is executing internal block erase, program, or lock-bit configuration algorithms. It is V<sub>OH</sub> when the WSM is not busy, in block erase suspend mode (with programming inactive), or reset/power-down mode.
4. See *Read Identifier Codes Command* section for read identifier code data.
5. See *Read Query Mode Command* section for read query data.
6. Command writes involving block erase, program, or lock-bit configuration are reliably executed when V<sub>PEN</sub> = V<sub>PENH</sub> and V<sub>CC</sub> is within specification. Block erase, program, or lock-bit configuration with V<sub>IH</sub> < RP# < V<sub>HH</sub> produce spurious results and should not be attempted.
7. Refer to Table 4 for valid D<sub>IN</sub> during a write operation.
8. DQ refers to DQ<sub>0</sub>–DQ<sub>7</sub> if BYTE# is low and DQ<sub>0</sub>–DQ<sub>15</sub> if BYTE# is high.
9. High Z will be V<sub>OH</sub> with an external pull-up resistor.
10. See Table 2 for valid CE configurations.
11. OE# and WE# should never be enabled simultaneously.

Table 4. Intel® StrataFlash™ Memory Command Set Definitions<sup>(14)</sup>

Command	Scaleable or Basic Command Set <sup>(15)</sup>	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
				Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3,4)</sup>	Oper <sup>(1)</sup>	Addr <sup>(2)</sup>	Data <sup>(3,4)</sup>
Read Array	SCS/BCS	1		Write	X	FFH			
Read Identifier Codes	SCS/BCS	≥2	5	Write	X	90H	Read	IA	ID
Read Query	SCS	≥ 2		Write	X	98H	Read	QA	QD
Read Status Register	SCS/BCS	2	6	Write	X	70H	Read	X	SRD
Clear Status Register	SCS/BCS	1		Write	X	50H			
Write to Buffer	SCS/BCS	> 2	7,8,9	Write	BA	E8H	Write	BA	N
Word/Byte Program	SCS/BCS	2	10,11	Write	PA	40H or 10H	Write	PA	PD
Block Erase	SCS/BCS	2	9,10	Write	BA	20H	Write	BA	D0H
Block Erase Suspend	SCS/BCS	1	9,10	Write	X	B0H			
Block Erase Resume	SCS/BCS	1	10	Write	X	D0H			
Configuration	SCS	2		Write	X	B8H	Write	X	CC
Set Block Lock-Bit	SCS	2	12	Write	BA	60H	Write	BA	01H
Clear Block Lock-Bits	SCS	2	13	Write	X	60H	Write	X	D0H
Set Master Lock-Bit		2	12,13	Write	X	60H	Write	X	F1H



**NOTES:**

1. Bus operations are defined in Table 3.
2. X = Any valid address within the device.  
BA = Address within the block.  
IA = Identifier Code Address: see Figure 6 and Table 13.  
QA = Query database Address.  
PA = Address of memory location to be programmed.
3. ID = Data read from Identifier Codes.  
QD = Data read from Query database.  
SRD = Data read from status register. See Table 16 for a description of the status register bits.  
PD = Data to be programmed at location PA. Data is latched on the rising edge of WE#.  
CC = Configuration Code.
4. The upper byte of the data bus (DQ<sub>8</sub>–DQ<sub>15</sub>) during command writes is a “Don’t Care” in x16 operation.
5. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. See *Read Identifier Codes Command* section for read identifier code data.
6. If the WSM is running, only DQ<sub>7</sub> is valid; DQ<sub>15</sub>–DQ<sub>8</sub> and DQ<sub>6</sub>–DQ<sub>0</sub> float, which places them in a high-impedance state.
7. After the Write to Buffer command is issued check the XSR to make sure a buffer is available for writing.
8. The number of bytes/words to be written to the Write Buffer = N + 1, where N = byte/word count argument. Count ranges on this device for byte mode are N = 00H to N = 1FH and for word mode are N = 0000H to N = 000FH. The third and consecutive bus cycles, as determined by N, are for writing data into the Write Buffer. The Confirm command (D0H) is expected after exactly N + 1 write cycles; any other command at that point in the sequence aborts the write to buffer operation. Please see Figure 7, *Write to Buffer Flowchart*, for additional information.
9. Programming the write buffer to flash or initiating the erase operation does not begin until a confirm command (D0h) is issued.
10. If the block is locked, RP# must be at V<sub>H</sub>H to enable block erase or program operations. Attempts to issue a block erase or program to a locked block while RP# is V<sub>I</sub>H will fail.
11. Either 40H or 10H are recognized by the WSM as the byte/word program setup.
12. If the master lock-bit is set, RP# must be at V<sub>H</sub>H to set a block lock-bit. RP# must be at V<sub>H</sub>H to set the master lock-bit. If the master lock-bit is not set, a block lock-bit can be set while RP# is V<sub>I</sub>H.
13. If the master lock-bit is set, RP# must be at V<sub>H</sub>H to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits. If the master lock-bit is not set, the Clear Block Lock-Bits command can be done while RP# is V<sub>I</sub>H.
14. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.
15. The Basic Command Set (BCS) is the same as the 28F008SA Command Set or Intel Standard Command Set. The Scaleable Command Set (SCS) is also referred to as the Intel Extended Command Set.

## 4.1 Read Array Command

Upon initial device power-up and after exit from reset/power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, program, or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend command. The Read Array command functions independently of the  $V_{PEN}$  voltage and  $RP\#$  can be  $V_{IH}$  or  $V_{HH}$ .

## 4.2 Read Query Mode Command

This section defines the data structure or “database” returned by the SCS (Scaleable Command Set) Query command. System software should parse this structure to gain critical information to enable programming, block erases, and otherwise control the flash component. The SCS Query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI. The Query can only be accessed when the WSM is off or the device is suspended.

### 4.2.1 QUERY STRUCTURE OUTPUT

The Query “database,” described later, allows system software to gain critical information for controlling the flash component. This section describes the device’s CFI-compliant interface that allows the host system to access Query data.

Query data are always presented on the lowest-order data outputs  $DQ_0$ – $DQ_7$  only. The Query table device starting address is a 10h word address.

The first two bytes of the Query structure, “Q” and “R” in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00H data on upper bytes. Thus, the device outputs ASCII “Q” in the low byte  $DQ_0$ – $DQ_7$  and 00h in the high byte  $DQ_8$ – $DQ_{15}$ .

Since the device is x8/x16 capable, the x8 data is still presented in word-relative (16-bit) addresses. However, the “fill data” (00h) is not the same as driven by the upper bytes in the x16 mode. As in x16 mode, the byte address ( $A_0$  or  $A_1$  depending on pinout) is ignored for Query output so that the “odd byte address” ( $A_0$  or  $A_1$  high) repeats the “even byte address” data ( $A_0$  or  $A_1$  low). Therefore, in x8 mode using byte addressing, the device will output the sequence “Q,” “Q,” “R,” “R,” “Y,” “Y,” and so on, beginning at byte-relative address 20h (which is equivalent to word offset 10h in x16 mode).

In Query addresses where two or more bytes of information are located, the least significant data byte is presented on the lower address, and the most significant data byte is presented on the higher address.



Table 5. Summary of Query Structure Output as a Function of Device and Mode

Device type/ mode	Query start location in maximum device bus width addresses	Query data with maximum device bus width addressing "x" = ASCII equivalent	Query start address in bytes	Query data with byte addressing
x16 device/ x16 mode	10h	10h: 0051h "Q" 11h: 0052h "R" 12h: 0059h "Y"	20h	20h: 51h "Q" 21h: 00h null 22h: 52h "R"
x16 device/ x8 mode	N/A <sup>(1)</sup>	N/A <sup>(1)</sup>	20h	20h: 51h "Q" 21h: 51h "Q" 22h: 52h "R"

**NOTE:**

1. The system must drive the lowest order addresses to access all the device's array data when the device is configured in x8 mode. Therefore, word addressing where these lower addresses not toggled by the system is "Not Applicable" for x8-configured devices.

Table 6. Example of Query Structure Output of a x16- and x8-Capable Device

Device Address	Word Addressing: Query Data	Byte Address	Byte Addressing: Query Data
A <sub>16</sub> -A <sub>1</sub>	D <sub>15</sub> -D <sub>0</sub>	A <sub>7</sub> -A <sub>0</sub>	D <sub>7</sub> -D <sub>0</sub>
0010h	0051h "Q"	20h	51h "Q"
0011h	0052h "R"	21h	51h "Q"
0012h	0059h "Y"	22h	52h "R"
0013h	P_ID <sub>LO</sub> PrVendor	23h	52h "R"
0014h	P_ID <sub>HI</sub> ID #	24h	59h "Y"
0015h	P <sub>LO</sub> PrVendor	25h	59h "Y"
0016h	P <sub>HI</sub> TblAdr	26h	P_ID <sub>LO</sub> PrVendor
0017h	A_ID <sub>LO</sub> AltVendor	27h	P_ID <sub>LO</sub> ID #
0018h	A_ID <sub>HI</sub> ID #	28h	P_ID <sub>HI</sub> "
...	...	...	...

#### 4.2.2 QUERY STRUCTURE OVERVIEW

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or "database." The structure sub-sections and address locations are summarized below. See *AP-646 Common Flash Interface (CFI) and Command Sets* (order number 292204) for a full description of CFI.

The following sections describe the Query structure sub-sections in detail.

**Table 7. Query Structure**

Offset	Sub-Section Name	Description
00h		Manufacturer Code
01h		Device Code
(BA+2)h <sup>(2)</sup>	Block Status Register	Block-Specific Information
04–0Fh	Reserved	Reserved for Vendor-Specific Information
10h	CFI Query Identification String	Command Set ID and Vendor Data Offset
1Bh	System Interface Information	Device Timing and Voltage Information
27h	Device Geometry Definition	Flash Device Layout
P <sup>(3)</sup>	Primary Vendor-Specific Extended Query table	Vendor-Defined Additional Information Specific to the Primary Vendor Algorithm

**NOTES:**

1. Refer to Query Data Output section of Device Hardware interface for the detailed definition of offset address as a function of device word width and mode.
2. BA = The beginning location of a Block Address (i.e., 2000h is the beginning location of block 2 when the block size is 128 KB).
3. The Primary Vendor-Specific Extended Query table (P) address may change among SCS-compliant devices. Software should retrieve this address from address 15 to guarantee compatibility with future SCS-compliant devices.



#### 4.2.3 BLOCK STATUS REGISTER

The Block Status Register indicates whether a given block is locked and can be accessed for program/erase operations. The Block Status Register is accessed from word address 02h within each block.

Table 8. Block Status Register

Offset	Length (bytes)	Description	Intel® StrataFlash™ Memory x16 device/mode
(BA +2)h <sup>1</sup>	01h	Block Status Register	BA+2: 0000h or 0001h
		BSR.0 = Block Lock Status (Optional) 1 = Locked 0 = Unlocked	BA+2 (bit 0): 0 or 1
		BSR.1 = Block Erase Status <sup>(2)</sup> (Optional)  1 = Last erase operation did not complete successfully 0 = Last erase operation completed successfully	BA+2 (bit 1): 0  (The device does not support Block Erase Status)
		BSR 2–7 Reserved for future use	BA+2 (bits 2–7): 0

**NOTES:**

1. BA = The beginning location of a Block Address (i.e., 2000h is the beginning location of block 2).
2. Block Erase Status is an optional part of the SCS definition and is not incorporated on this device.

#### 4.2.4 CFI QUERY IDENTIFICATION STRING

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version of the spec and which vendor-specified command set(s) is(are) supported.

**Table 9. CFI Identification**

Offset	Length (bytes)	Description	Intel® StrataFlash™ Memory
10h	03h	Query-unique ASCII string "QRY"	10: 0051h 11: 0052h 12: 0059h
13h	02h	Primary Vendor Command Set and Control Interface ID Code 16-bit ID code for vendor-specified algorithms	13: 0001h 14: 0000h
15h	02h	Address for Primary Algorithm Extended Query table Offset value = $P = 31h$	15: 0031h 16: 0000h
17h	02h	Alternate Vendor Command Set and Control Interface ID Code second vendor-specified algorithm supported <b>Note: 0000h means none exists</b>	17: 0000h 18: 0000h
19h	02h	Address for Secondary Algorithm Extended Query table <b>Note: 0000h means none exists</b>	19: 0000h 1A: 0000h



## 4.2.5 SYSTEM INTERFACE INFORMATION

The following device information can optimize system interface software.

Table 10. System Interface Information

Offset	Length (bytes)	Description	Intel® StrataFlash™ Memory
1Bh	01h	V <sub>CC</sub> Logic Supply Minimum Program/Erase voltage bits 7–4 BCD volts bits 3–0 BCD 100 mv	1B: 0045h
1Ch	01h	V <sub>CC</sub> Logic Supply Maximum Program/Erase voltage bits 7–4 BCD volts bits 3–0 BCD 100 mv	1C: 0055h
1Dh	01h	V <sub>PP</sub> [Programming] Supply Minimum Program/Erase voltage bits 7–4 HEX volts bits 3–0 BCD 100 mv	1D: 0000h
1Eh	01h	V <sub>PP</sub> [Programming] Supply Maximum Program/Erase voltage bits 7–4 HEX volts bits 3–0 BCD 100 mv	1E: 0000h
1Fh	01h	Typical time-out per single byte/word program, 2 <sup>N</sup> μs	1F: 0007h
20h	01h	Typical time-out for max. buffer write, 2 <sup>N</sup> μs	20: 0007h
21h	01h	Typical time-out per individual block erase, 2 <sup>N</sup> ms	21: 000Ah
22h	01h	Typical time-out for full chip erase, 2 <sup>N</sup> ms ( <b>0000h = not supported</b> )	22: 0000h
23h	01h	Maximum time-out for byte/word program, 2 <sup>N</sup> times typical	23: 0004h
24h	01h	Maximum time-out for buffer write, 2 <sup>N</sup> times typical	24: 0004h
25h	01h	Maximum time-out per individual block erase, 2 <sup>N</sup> times typical	25: 0004h
26h	01h	Maximum time-out for chip erase, 2 <sup>N</sup> times typical ( <b>00h = not supported</b> )	26: 0000h



4.2.6 DEVICE GEOMETRY DEFINITION

This field provides critical details of the flash device geometry.

Table 11. Device Geometry Definition

Offset	Length (bytes)	Description	Intel® StrataFlash™ Memory						
27h	01h	Device Size = 2 <sup>N</sup> in number of bytes.	27: 0017h (64-Mbit) 27: 0016h (32-Mbit)						
28h	02h	Flash Device Interface description  <table border="0"> <tr> <td><u>value</u></td> <td><u>meaning</u></td> </tr> <tr> <td>0000h</td> <td>x8 asynchronous</td> </tr> <tr> <td>0002h</td> <td>x8/x16 asynchronous</td> </tr> </table>	<u>value</u>	<u>meaning</u>	0000h	x8 asynchronous	0002h	x8/x16 asynchronous	28: 0002h 29: 0000h
<u>value</u>	<u>meaning</u>								
0000h	x8 asynchronous								
0002h	x8/x16 asynchronous								
2Ah	02h	Maximum number of bytes in write buffer = 2 <sup>N</sup>	2A: 0005h 2B: 0000h						
2Ch	01h	Number of Erase Block Regions within device:  <b>bits 7–0 = x = # of Erase Block Regions</b>	2C: 0001h						
2Dh	04h	Erase Block Region Information  <b>bits 15–0 = y</b> , where y+1 = Number of Erase Blocks of identical size within region  <b>bits 31–16 = z</b> , where the Erase Block(s) within this Region are (z) times 256 bytes	y: 64 Blocks (64-Mbit) 2D: 003Fh 2E: 0000h  y: 32 Blocks (32-Mbit) 2D: 001Fh 2E: 0000h  z: (128 KB size) 2F: 0000h 30: 0002h						





4.2.7 PRIMARY-VENDOR SPECIFIC EXTENDED QUERY TABLE

Certain flash features and commands are optional. The *Primary Vendor-Specific Extended Query* table specifies this and other similar information.

Table 12. Primary Vendor-Specific Extended Query

Offset <sup>(1)</sup>	Length (bytes)	Description	Intel® StrataFlash™ Memory
(P)h	03h	Primary extended Query table unique ASCII string "PRI"	31: 0050h 32: 0052h 33: 0049h
(P +3)h	01h	Major version number, ASCII	34: 0031
(P +4)h	01h	Minor version number, ASCII	35: 0031
(P +5)h	04h	Optional Feature and Command Support  bit 0 Chip Erase Supported (1=yes, 0=no) bit 1 Suspend Erase Supported (1=yes, 0=no) bit 2 Suspend Program Supported (1=yes, 0=no) bit 3 Lock/Unlock Supported (1=yes, 0=no) bit 4 Queued Erase Supported (1=yes, 0=no)  <i>bits 5–31 Reserved for future use; undefined bits are "0"</i>	36: 000Ah 37: 0000h 38: 0000h 39: 0000h
(P +9)h	01h	Supported functions after Suspend  Read Array, Status, and Query are always supported during suspended Erase. This field defines other operations supported.  bit 0 Program supported after Erase Suspend (1=yes, 0=no)  <i>bits 1–7 Reserved for future use; undefined bits are "0"</i>	3A: 0001h
(P +A)h	02h	Block Status Register Mask  Defines which bits in the Block Status Register section of Query are implemented.  bit 0 Block Status Register Lock Bit [BSR.0] active (1=yes, 0=no) bit 1 Block Status Register Valid Bit [BSR.1] active (1=yes, 0=no)  <i>bits 2–15 Reserved for future use; undefined bits are "0"</i>	3B: 0001h 3C: 0000h

NOTE:

1. The Primary Vendor-Specific Extended Query table (P) address may change among SCS-compliant devices. Software should retrieve this address from address 15 to guarantee compatibility with future SCS-compliant devices.



Table 12. Primary Vendor-Specific Extended Query (Continued)

Offset <sup>(1)</sup>	Length (bytes)	Description	Intel® StrataFlash™ Memory
(P +C)h	01h	V <sub>CC</sub> Optimum Program/Erase voltage (highest performance)  bits 7–4      BCD value in volts bits 3–0      BCD value in 100 millivolts	3D:      0050h
(P +D)h	01h	V <sub>PP</sub> [Programming] Optimum Program/Erase voltage  bits 7–4      HEX value in volts bits 3–0      BCD value in 100 millivolts  <i>Note: This value is 0000h; no V<sub>PP</sub> pin is present</i>	3E:      0000h
(P +E)h	<i>reserved</i>	<i>Reserved for future use</i>	

**NOTE:**

1. The Primary Vendor-Specific Extended Query table (P) address may change among SCS-compliant devices. Software should retrieve this address from address 15 to guarantee compatibility with future SCS-compliant devices.

**4.3 Read Identifier Codes Command**

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 6 retrieve the manufacturer, device, block lock configuration and master lock configuration codes (see Table 13 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V<sub>PEN</sub> voltage and RP# can be V<sub>IH</sub> or V<sub>HH</sub>. This command is valid only when the WSM is off or the device is suspended. Following the Read Identifier Codes command, the following information can be read:

Table 13. Identifier Codes<sup>(1)</sup>

Code	Address <sup>(1)</sup>	Data	
Manufacture Code	00000	(00) 89	
Device Code	32-Mbit	00001	(00) 14
	64-Mbit	00001	(00) 15
Block Lock Configuration	X0002 <sup>(2)</sup>		
• Block Is Unlocked		DQ <sub>0</sub> = 0	
• Block Is Locked		DQ <sub>0</sub> = 1	
• Reserved for Future Use		DQ <sub>1–7</sub>	
Master Lock Configuration	00003		
• Device Is Unlocked		DQ <sub>0</sub> = 0	
• Device Is Locked		DQ <sub>0</sub> = 1	
• Reserved for Future Use		DQ <sub>1–7</sub>	

**NOTE:**

1. A<sub>0</sub> is not used in either x8 or x16 modes when obtaining the identifier codes. The lowest order address line is A<sub>1</sub>. Data is always presented on the low byte in x16 mode (upper byte contains 00h).
2. X selects the specific block's lock configuration code. See Figure 6 for the device identifier code memory map.

#### 4.4 Read Status Register Command

The status register may be read to determine when a block erase, program, or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or the first edge of CE<sub>0</sub>, CE<sub>1</sub>, or CE<sub>2</sub> that enables the device (see Table 2, *Chip Enable Truth Table*). OE# must toggle to V<sub>IH</sub> or the device must be disabled (see Table 2, *Chip Enable Truth Table*) before further reads to update the status register latch. The Read Status Register command functions independently of the V<sub>PEN</sub> voltage. RP# can be V<sub>IH</sub> or V<sub>HH</sub>.

During a program, block erase, set lock-bit, or clear lock-bit command sequence, only SR.7 is valid until the Write State Machine completes or suspends the operation. Device I/O pins DQ<sub>0</sub>–DQ<sub>6</sub> and DQ<sub>8</sub>–DQ<sub>15</sub> are placed in a high-impedance state. When the operation completes or suspends (check Status Register bit 7), all contents of the Status Register are valid when read.

#### 4.5 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to “1”s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 16). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V<sub>PEN</sub> voltage. RP# can be V<sub>IH</sub> or V<sub>HH</sub>. The Clear Status Register Command is only valid when the WSM is off or the device is suspended.

#### 4.6 Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires an appropriate address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 9). The CPU can detect block erase completion by analyzing the output of the STS pin or status register bit SR.7. Toggle OE#, CE<sub>0</sub>, CE<sub>1</sub>, or CE<sub>2</sub> to update the status register.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to “1.” Also, reliable block erasure can only occur when V<sub>CC</sub> is valid and V<sub>PEN</sub> = V<sub>PENH</sub>. If block erase is attempted while V<sub>PEN</sub> ≤ V<sub>PENLK</sub>, SR.3 and SR.5 will be set to “1.” Successful block erase requires that the corresponding block lock-bit be cleared or, if set, that RP# = V<sub>HH</sub>. If block erase is attempted when the corresponding block lock-bit is set and RP# = V<sub>IH</sub>, SR.1 and SR.5 will be set to “1.” Block erase operations with V<sub>IH</sub> < RP# < V<sub>HH</sub> produce spurious results and should not be attempted.

#### 4.7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or program data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bit SR.7 then SR.6 can determine when the block erase operation has been suspended (both will be set to “1”). In default mode, STS will also transition to

$V_{OH}$ . Specification  $t_{WHRH}$  defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A program command sequence can also be issued during erase suspend to program data in other blocks. During a program operation with block erase suspended, status register bit SR.7 will return to "0" and the STS output (in default mode) will transition to  $V_{OL}$ .

The only other valid commands while block erase is suspended are Read Query, Read Status Register, Clear Status Register, Configure, and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and STS (in default mode) will return to  $V_{OL}$ . After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 10).  $V_{PEN}$  must remain at  $V_{PENH}$  (the same  $V_{PEN}$  level used for block erase) while block erase is suspended. RP# must also remain at  $V_{IH}$  or  $V_{HH}$  (the same RP# level used for block erase). Block erase cannot resume until program operations initiated during block erase suspend have completed.

#### 4.8 Write to Buffer Command

To program the flash device, a Write to Buffer command sequence is initiated. A variable number of bytes, up to the buffer size, can be loaded into the buffer and written to the flash device. First, the Write to Buffer setup command is issued along with the Block Address (see Figure 7, *Write to Buffer Flowchart*). At this point, the eXtended Status Register (XSR, see Table 17) information is loaded and XSR.7 reverts to "buffer available" status. If XSR.7 = 0, the write buffer is not available. To retry, continue monitoring XSR.7 by issuing the Write to Buffer setup command with the Block Address until XSR.7 = 1. When XSR.7 transitions to a "1," the buffer is ready for loading.

Now a word/byte count is given to the part with the Block Address. On the next write, a device start address is given along with the write buffer data. Subsequent writes provide additional device addresses and data, depending on the count. All subsequent addresses must lie within the start address plus the count.

Internally, this device programs many flash cells in parallel. Because of this parallel programming, maximum programming performance and lower power are obtained by aligning the start address at the beginning of a write buffer boundary (i.e.,  $A_4-A_0$  of the start address = 0).

After the final buffer data is given, a Write Confirm command is issued. This initiates the WSM (Write State Machine) to begin copying the buffer data to the flash array. If a command other than Write Confirm is written to the device, an "Invalid Command/Sequence" error will be generated and Status Register bits SR.5 and SR.4 will be set to a "1." For additional buffer writes, issue another Write to Buffer setup command and check XSR.7.

If an error occurs while writing, the device will stop writing, and Status Register bit SR.4 will be set to a "1" to indicate a program failure. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. If a program error is detected, the status register should be cleared. Any time SR.4 and/or SR.5 is set (e.g., a media failure occurs during a program or an erase), the device will not accept any more Write to Buffer commands. Additionally, if the user attempts to program past an erase block boundary with a Write to Buffer command, the device will abort the Write to Buffer operation. This will generate an "Invalid Command/Sequence" error and Status Register bits SR.5 and SR.4 will be set to a "1."

Reliable buffered writes can only occur when  $V_{PEN} = V_{PENH}$ . If a buffered write is attempted while  $V_{PEN} \leq V_{PENLK}$ , Status Register bits SR.4 and SR.3 will be set to "1." Buffered write attempts with invalid  $V_{CC}$  and  $V_{PEN}$  voltages produce spurious results and should not be attempted. Finally, successful programming requires that the corresponding Block Lock-Bit be reset or, if set, that RP# =  $V_{HH}$ . If a buffered write is attempted when the corresponding Block Lock-Bit is set and RP# =  $V_{IH}$ , SR.1 and SR.4 will be set to "1." Buffered write operations with  $V_{IH} < RP# < V_{HH}$  produce spurious results and should not be attempted.

#### 4.9 Byte/Word Program Commands

Byte/Word program is executed by a two-cycle command sequence. Byte/Word program setup (standard 40H or alternate 10H) is written followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM

then takes over, controlling the program and program verify algorithms internally. After the program sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect the completion of the program event by analyzing the STS pin or status register bit SR.7.

When program is complete, status register bit SR.4 should be checked. If a program error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable byte/word programs can only occur when  $V_{CC}$  and  $V_{PEN}$  are valid. If a byte/word program is attempted while  $V_{PEN} \leq V_{PENLK}$ , status register bits SR.4 and SR.3 will be set to "1." Successful byte/word programs require that the corresponding block lock-bit be cleared or, if set, that  $RP\# = V_{HH}$ . If a byte/word program is attempted when the corresponding block lock-bit is set and  $RP\# = V_{IH}$ , SR.1 and SR.4 will be set to "1." Byte/Word program operations with  $V_{IH} < RP\# < V_{HH}$  produce spurious results and should not be attempted.

#### 4.10 Configuration Command

The Status (STS) pin can be configured to different states using the Configuration command. Once the STS pin has been configured, it remains in that configuration until another configuration command is issued or  $RP\#$  is asserted low. Initially, the STS pin defaults to RY/BY# operation where RY/BY# low indicates that the state machine is busy. RY/BY# high indicates that the state machine is ready for a new operation or suspended. Table 15 displays the possible STS configurations.

To reconfigure the Status (STS) pin to other modes, the Configuration command is given followed by the desired configuration code. The three alternate configurations are all pulse mode for use as a system interrupt as described below. For these configurations, bit 0 controls Erase Complete interrupt pulse, and bit 1 controls Program Complete interrupt pulse. Supplying the 00h configuration code with the Configuration command resets the STS pin to the default RY/BY# level mode. The possible configurations and their usage are described in Table 15. The Configuration command may only be given when the device is not busy or suspended. Check SR.7 for device status.

An invalid configuration code will result in both status register bits SR.4 and SR.5 being set to "1." When configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250 ns.

#### 4.11 Set Block and Master Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits and a master lock-bit. The block lock-bits gate program and erase operations while the master lock-bit gates block-lock bit modification. With the master lock-bit not set, individual block lock-bits can be set using the Set Block Lock-Bit command. The Set Master Lock-Bit command, in conjunction with  $RP\# = V_{HH}$ , sets the master lock-bit. After the master lock-bit is set, subsequent setting of block lock-bits requires both the Set Block Lock-Bit command and  $V_{HH}$  on the  $RP\#$  pin. These commands are invalid while the WSM is running or the device is suspended. See Table 14 for a summary of hardware and software write protection options.

Set block lock-bit and master lock-bit commands are executed by a two-cycle sequence. The set block or master lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set master lock-bit confirm (and any device address). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 11). The CPU can detect the completion of the set lock-bit event by analyzing the STS pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block or Master Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1." Also, reliable operations occur only when  $V_{CC}$  and  $V_{PEN}$  are valid. With  $V_{PEN} \leq V_{PENLK}$ , lock-bit contents are protected against alteration.



A successful set block lock-bit operation requires that the master lock-bit be zero or, if the master lock-bit is set, that  $RP\# = V_{HH}$ . If it is attempted with the master lock-bit set and  $RP\# = V_{IH}$ , SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations while  $V_{IH} < RP\# < V_{HH}$  produce spurious results and should not be attempted. A successful set master lock-bit operation requires that  $RP\# = V_{HH}$ . If it is attempted with  $RP\# = V_{IH}$ , SR.1 and SR.4 will be set to "1" and the operation will fail. Set master lock-bit operations with  $V_{IH} < RP\# < V_{HH}$  produce spurious results and should not be attempted.

**4.12 Clear Block Lock-Bits Command**

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With the master lock-bit not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the master lock-bit is set, clearing block lock-bits requires both the Clear Block Lock-Bits command and  $V_{HH}$  on the  $RP\#$  pin. This command is invalid while the WSM is running or the device is suspended. See Table 14 for a summary of hardware and software write protection options.

Clear block lock-bits command is executed by a two-cycle sequence. A clear block lock-bits setup is first written. The device automatically outputs status register data when read (see Figure 12). The CPU

can detect completion of the clear block lock-bits event by analyzing the STS pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1." Also, a reliable clear block lock-bits operation can only occur when  $V_{CC}$  and  $V_{PEN}$  are valid. If a clear block lock-bits operation is attempted while  $V_{PEN} \leq V_{PENLK}$ , SR.3 and SR.5 will be set to "1." A successful clear block lock-bits operation requires that the master lock-bit is not set or, if the master lock-bit is set, that  $RP\# = V_{HH}$ . If it is attempted with the master lock-bit set and  $RP\# = V_{IH}$ , SR.1 and SR.5 will be set to "1" and the operation will fail. A clear block lock-bits operation with  $V_{IH} < RP\# < V_{HH}$  produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to  $V_{PEN}$  or  $V_{CC}$  transitioning out of valid range or  $RP\#$  active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the master lock-bit is set, it cannot be cleared.

**Table 14. Write Protection Alternatives**

Operation	Master Lock-Bit	Block Lock-Bit	RP#	Effect
Block Erase or Program	X	0	$V_{IH}$ or $V_{HH}$	Block Erase and Program Enabled
		1	$V_{IH}$	Block is Locked. Block Erase and Program Disabled
			$V_{HH}$	Block Lock-Bit Override. Block Erase and Program Enabled
Set or Clear Block Lock-Bit	0	X	$V_{IH}$ or $V_{HH}$	Set or Clear Block Lock-Bit Enabled
	1	X	$V_{IH}$	Master Lock-Bit Is Set. Set or Clear Block Lock-Bit Disabled
			$V_{HH}$	Master Lock-Bit Override. Set or Clear Block Lock-Bit Enabled
Set Master Lock-Bit	X	X	$V_{IH}$	Set Master Lock-Bit Disabled
			$V_{HH}$	Set Master Lock-Bit Enabled

Table 15. Configuration Coding Definitions

Reserved	Pulse On Program Complete <sup>(1)</sup>	Pulse On Erase Complete <sup>(1)</sup>
bits 7–2	bit 1	bit 0
<p>DQ7–DQ2 = Reserved</p> <p>DQ1–DQ0 = STS Pin Configuration Codes</p> <p>00 = default, level mode RY/BY# (device ready) indication</p> <p>01 = pulse on Erase complete</p> <p>10 = pulse on Program complete</p> <p>11 = pulse on Erase or Program Complete</p> <p>Configuration Codes 01b, 10b, and 11b are all pulse mode such that the STS pin pulses low then high when the operation indicated by the given configuration is completed.</p> <p>Configuration Command Sequences for STS pin configuration (masking bits DQ7–DQ2 to 00h) are as follows:</p> <p>Default RY/BY# level mode: B8h, 00h</p> <p>ER INT (Erase Interrupt): B8h, 01h</p> <p style="padding-left: 20px;">Pulse-on-Erase Complete</p> <p>PR INT (Program Interrupt): B8h, 02h</p> <p style="padding-left: 20px;">Pulse-on-Program Complete</p> <p>ER/PR INT (Erase or Program Interrupt): B8h, 03h</p> <p style="padding-left: 20px;">Pulse-on-Erase or Program Complete</p>	<p>DQ7–DQ2 are reserved for future use.</p> <p>default (DQ1–DQ0 = 00) RY/BY#, level mode — used to control HOLD to a memory controller to prevent accessing a flash memory subsystem while any flash device’s WSM is busy.</p> <p>configuration 01 ER INT, pulse mode — used to generate a system interrupt pulse when any flash device in an array has completed a Block Erase or sequence of Queued Block Erases. Helpful for reformatting blocks after file system free space reclamation or “cleanup”</p> <p>configuration 10 PR INT, pulse mode — used to generate a system interrupt pulse when any flash device in an array has complete a Program operation. Provides highest performance for servicing continuous buffer write operations.</p> <p>configuration 11 ER/PR INT, pulse mode — used to generate system interrupts to trigger servicing of flash arrays when either erase or program operations are completed when a common interrupt service routine is desired.</p>	

**NOTE:**

1. When the device is configured in one of the pulse modes, the STS pin pulses low with a typical pulse width of 250 ns.



Table 16. Status Register Definitions

WSMS	ESS	ECLBS	PSLBS	VPENS	R	DPS	R
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
<b>High Z When Busy?</b>	<b>Status Register Bits</b>					<b>NOTES:</b>	
<b>No</b>	SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy					Check STS or SR.7 to determine block erase, program, or lock-bit configuration completion. SR.6–SR.0 are not driven while SR.7 = “0.”	
<b>Yes</b>	SR.6 = ERASE SUSPEND STATUS 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed					If both SR.5 and SR.4 are “1”s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.	
<b>Yes</b>	SR.5 = ERASE AND CLEAR LOCK-BITS STATUS 1 = Error in Block Erasure or Clear Lock-Bits 0 = Successful Block Erase or Clear Lock-Bits					SR.3 does not provide a continuous programming voltage level indication. The WSM interrogates and indicates the programming voltage level only after Block Erase, Program, Set Block/Master Lock-Bit, or Clear Block Lock-Bits command sequences.	
<b>Yes</b>	SR.4 = PROGRAM AND SET LOCK-BIT STATUS 1 = Error in Programming or Set Master/Block Lock-Bit 0 = Successful Programming or Set Master/Block Lock Bit					SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RP# only after Block Erase, Program, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RP# is not V <sub>HH</sub> . Read the block lock and master lock configuration codes using the Read Identifier Codes command to determine master and block lock-bit status.	
<b>Yes</b>	SR.3 = PROGRAMMING VOLTAGE STATUS 1 = Low Programming Voltage Detected, Operation Aborted 0 = Programming Voltage OK						
<b>Yes</b>	SR.2 = RESERVED FOR FUTURE ENHANCEMENTS						
<b>Yes</b>	SR.1 = DEVICE PROTECT STATUS 1 = Master Lock-Bit, Block Lock-Bit and/or RP# Lock Detected, Operation Abort 0 = Unlock						
<b>Yes</b>	SR.0 = RESERVED FOR FUTURE ENHANCEMENTS					SR.2 and SR.0 are reserved for future use and should be masked when polling the status register.	



Table 17. eXtended Status Register Definitions

<b>WBS</b>	<b>Reserved</b>	
<b>bit 7</b>	<b>bits 6–0</b>	
<b>High Z When Busy?</b>	<b>Status Register Bits</b>	<b>NOTES:</b>
<b>No</b>	XSR.7 = WRITE BUFFER STATUS 1 = Write buffer available 0 = Write buffer not available	After a Buffer-Write command, XSR.7 = 1 indicates that a Write Buffer is available.
<b>Yes</b>	XSR.6–XSR.0 = RESERVED FOR FUTURE ENHANCEMENTS	SR.6–SR.0 are reserved for future use and should be masked when polling the status register.

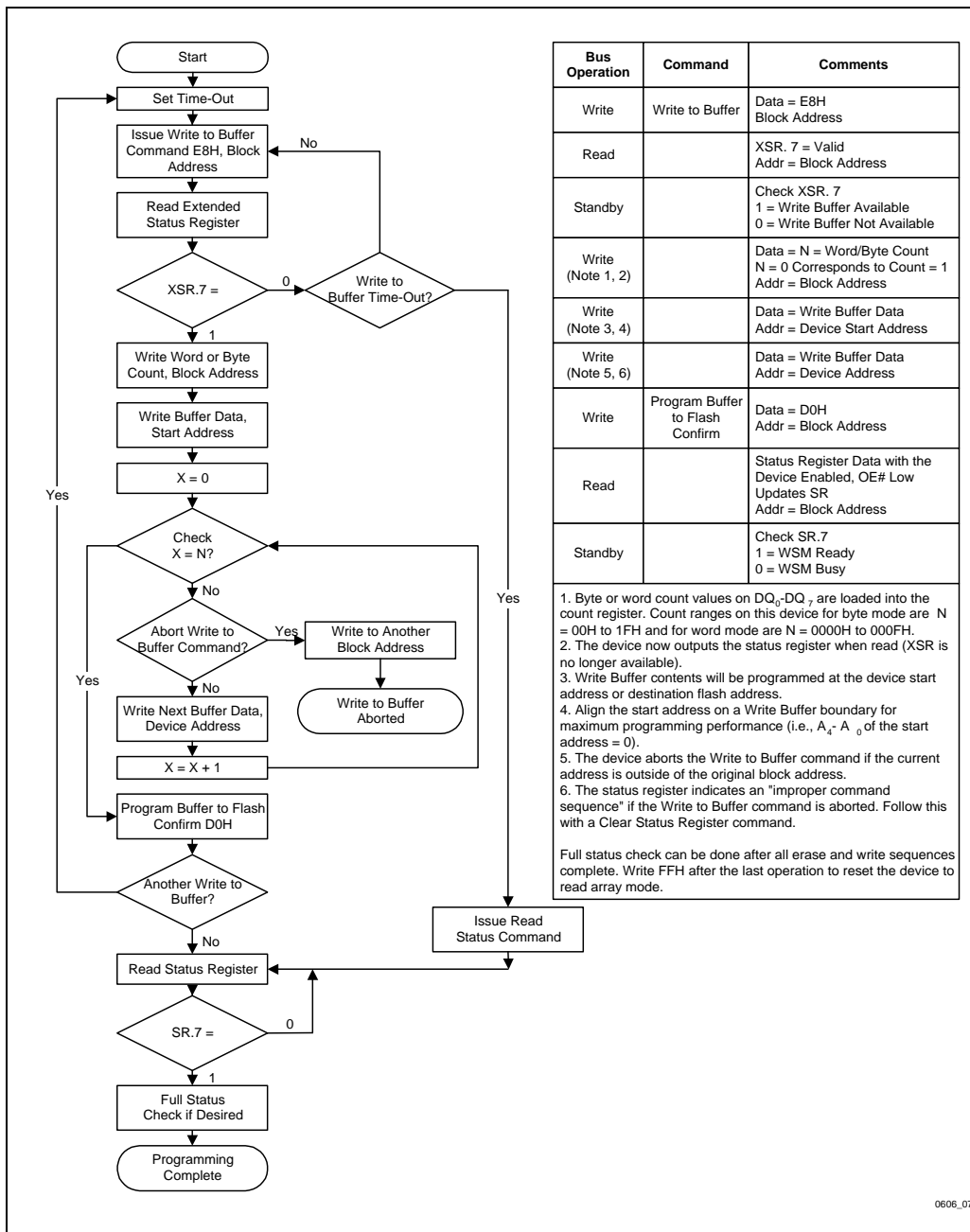


Figure 7. Write to Buffer Flowchart

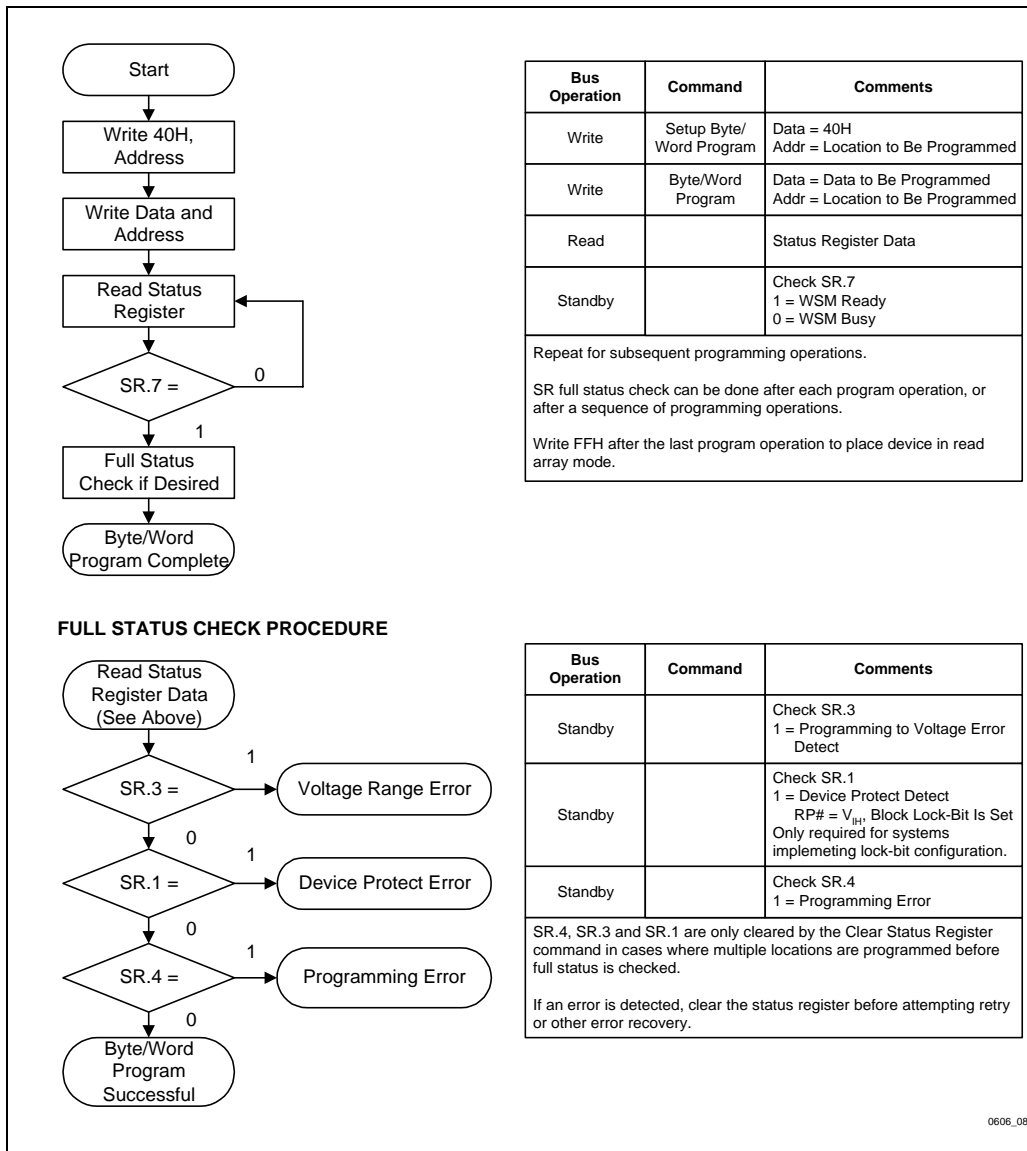


Figure 8. Byte/Word Program Flowchart

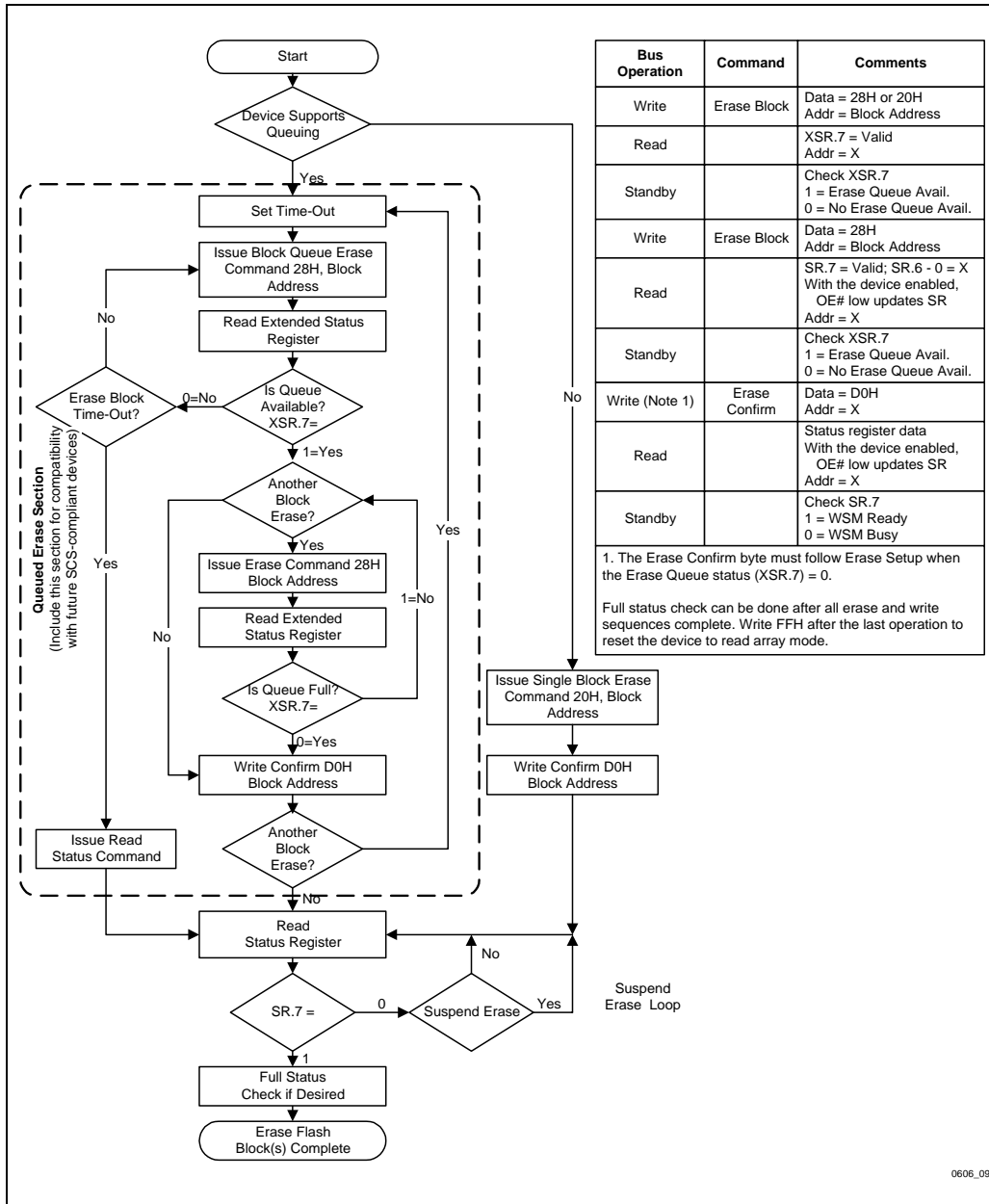


Figure 9. Block Erase Flowchart

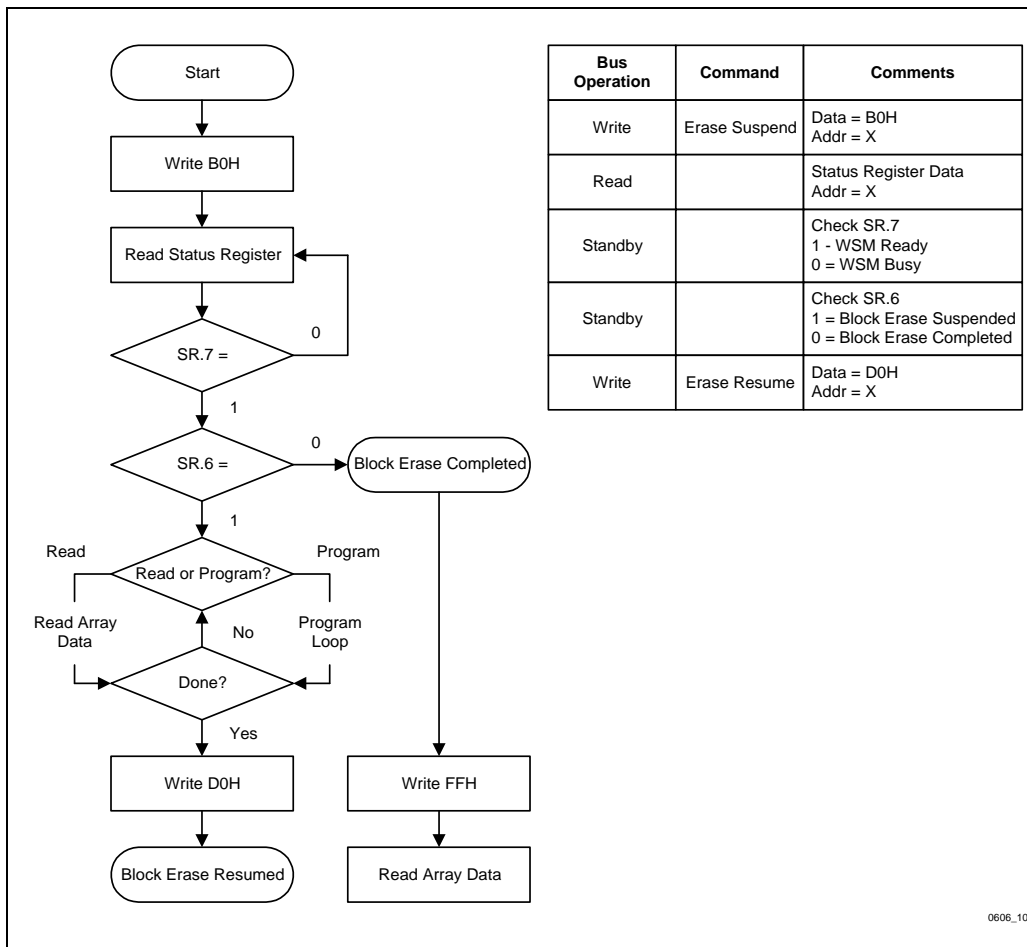


Figure 10. Block Erase Suspend/Resume Flowchart

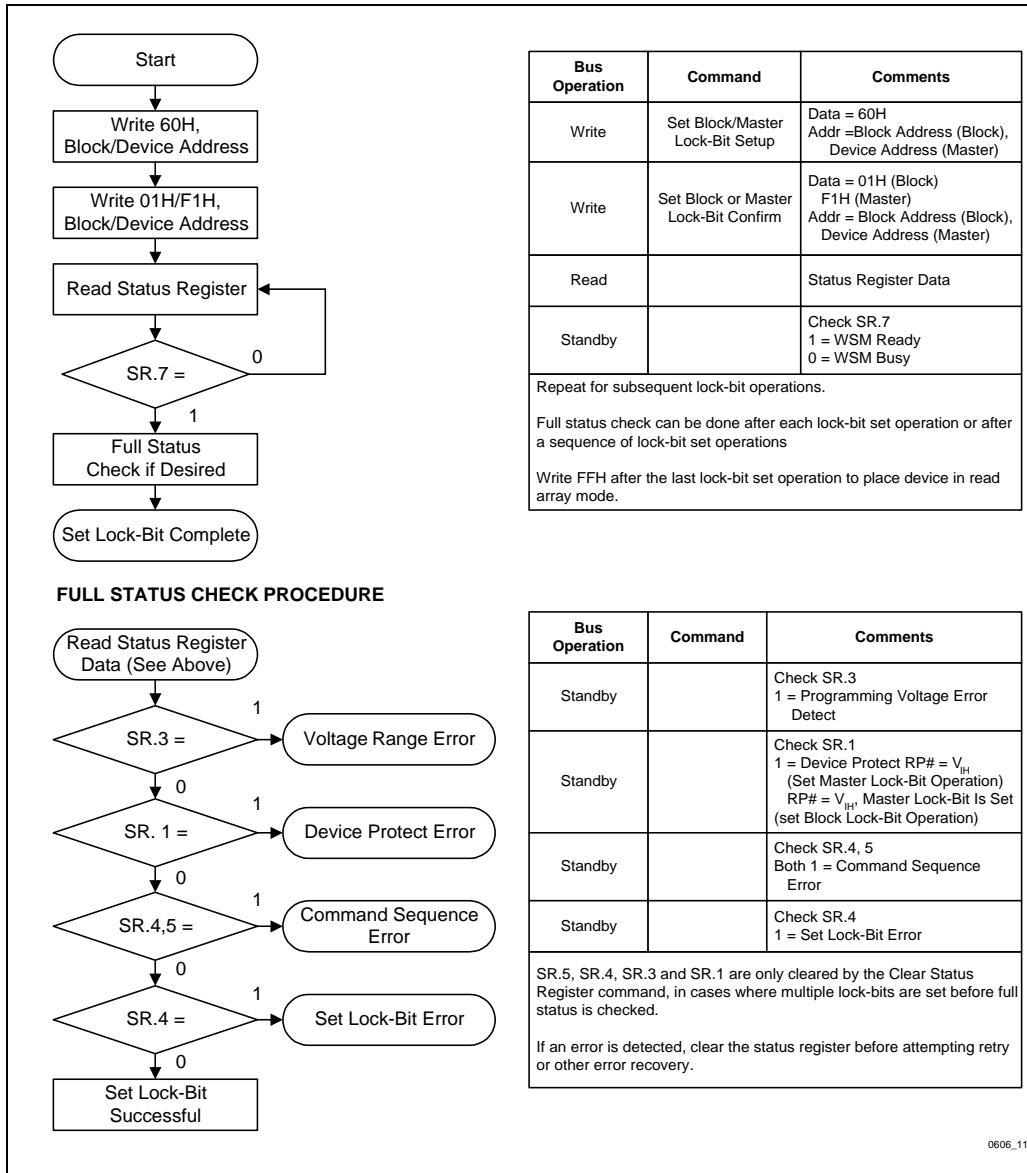


Figure 11. Set Block Lock-Bit Flowchart

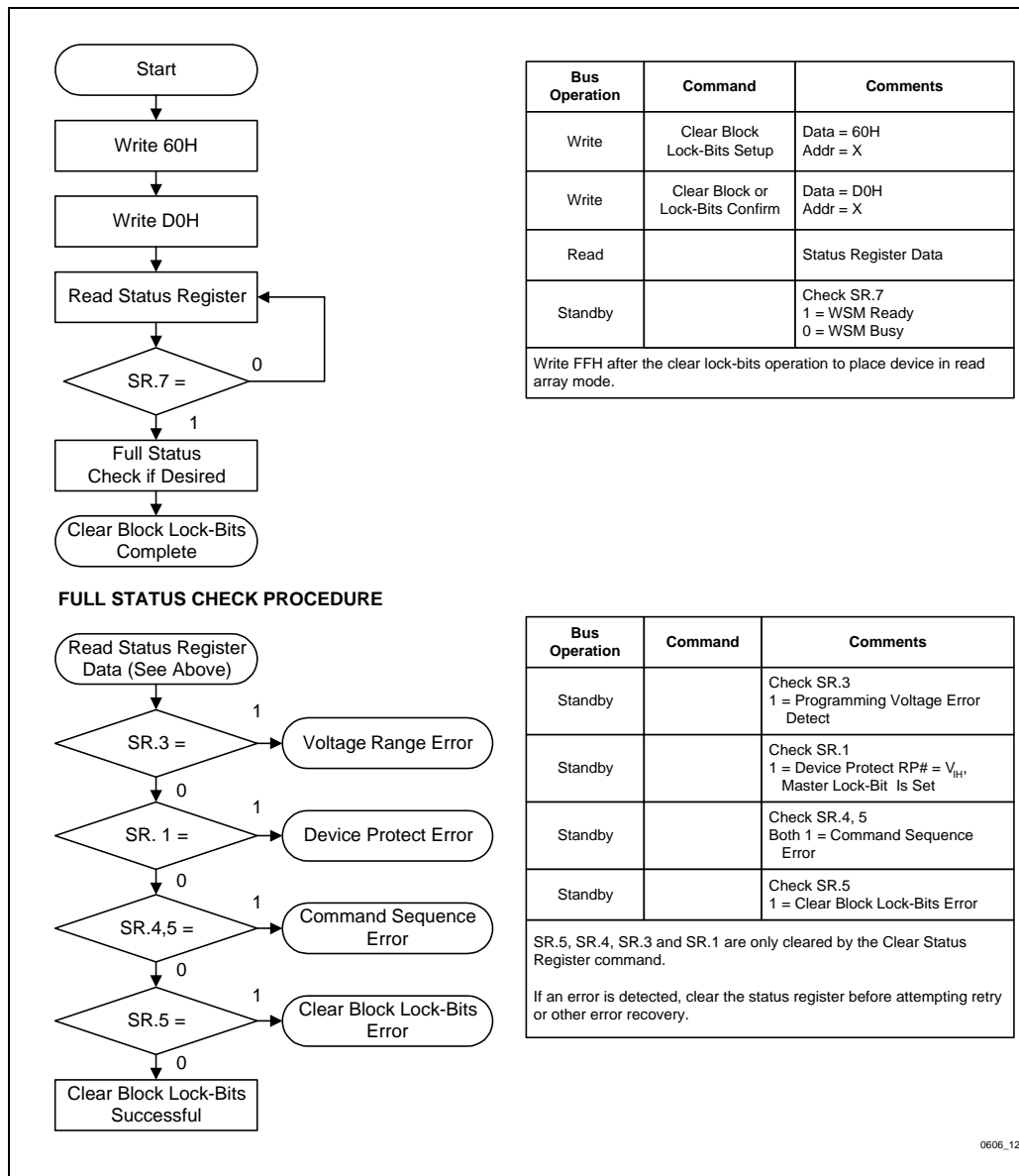


Figure 12. Clear Block Lock-Bit Flowchart

## 5.0 DESIGN CONSIDERATIONS

### 5.1 Three-Line Output Control

The device will often be used in large memory arrays. Intel provides five control inputs (CE<sub>0</sub>, CE<sub>1</sub>, CE<sub>2</sub>, OE#, and RP#) to accommodate multiple memory connections. This control provides for:

- a. Lowest possible memory power dissipation.
- b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable the device (see Table 2, *Chip Enable Truth Table*) while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while de-selected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

### 5.2 STS and Block Erase, Program, and Lock-Bit Configuration Polling

STS is an open drain output that should be connected to V<sub>CCQ</sub> by a pull-up resistor to provide a hardware method of detecting block erase, program, and lock-bit configuration completion. In default mode, it transitions low after block erase, program, or lock-bit configuration commands and returns to High Z when the WSM has finished executing the internal algorithm. For alternate configurations of the STS pin, see the Configuration command.

STS can be connected to an interrupt input of the system CPU or controller. It is active at all times. STS, in default mode, is also High Z when the device is in block erase suspend (with programming inactive) or in reset/power-down mode.

### 5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE<sub>0</sub>, CE<sub>1</sub>, CE<sub>2</sub>, and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Since Intel StrataFlash memory devices draw their power from three V<sub>CC</sub> pins (these devices do not include a V<sub>PP</sub> pin), it is recommended that systems without separate power and ground planes attach a 0.1 μF ceramic capacitor between each of the device's three V<sub>CC</sub> pins (this includes V<sub>CCQ</sub>) and ground. These high-frequency, low-inductance capacitors should be placed as close as possible to package leads on each StrataFlash device. Each device should have a 0.1 μF ceramic capacitor connected between its V<sub>CC</sub> and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed between V<sub>CC</sub> and GND at the array's power supply connection. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

### 5.4 V<sub>CC</sub>, V<sub>PEN</sub>, RP# Transitions

Block erase, program, and lock-bit configuration are not guaranteed if V<sub>PEN</sub> or V<sub>CC</sub> falls outside of the specified operating ranges, or RP# ≠ V<sub>IH</sub> or V<sub>IHL</sub>. If RP# transitions to V<sub>IL</sub> during block erase, program, or lock-bit configuration, STS (in default mode) will remain low for a maximum time of t<sub>PLPH</sub> + t<sub>PHRH</sub> until the reset operation is complete. Then, the operation will abort and the device will enter reset/power-down mode. The aborted operation may leave data partially corrupted after programming, or partially altered after an erase or lock-bit configuration. Therefore, block erase and lock-bit configuration commands must be repeated after normal operation is restored. Device power-off or RP# = V<sub>IL</sub> clears the status register.



The CUI latches commands issued by system software and is not altered by  $V_{PEN}$ ,  $CE_0$ ,  $CE_1$ , or  $CE_2$  transitions, or WSM actions. Its state is read array mode upon power-up, after exit from reset/power-down mode, or after  $V_{CC}$  transitions below  $V_{LKO}$ .  $V_{CC}$  must be kept at or above  $V_{PEN}$  during  $V_{CC}$  transitions.

After block erase, program, or lock-bit configuration, even after  $V_{PEN}$  transitions down to  $V_{PENLK}$ , the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.  $V_{PEN}$  must be kept at or below  $V_{CC}$  during  $V_{PEN}$  transitions.

### 5.5 Power-Up/Down Protection

The device is designed to offer protection against accidental block erasure, programming, or lock-bit configuration during power transitions. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for  $V_{CC}$  voltages above  $V_{LKO}$  when  $V_{PEN}$  is active. Since  $WE\#$  must be low and the device enabled (see Table 2, *Chip Enable Truth Table*) for a command write, driving  $WE\#$  to  $V_{IH}$  or disabling the device will inhibit writes. The CUI's two-step command sequence architecture provides added protection against data alteration.

Keeping  $V_{PEN}$  below  $V_{PENLK}$  prevents inadvertent data alteration. In-system block lock and unlock capability protects the device against inadvertent programming. The device is disabled while  $RP\# = V_{IL}$  regardless of its control inputs.

### 5.6 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.



**6.0 ELECTRICAL SPECIFICATIONS**

**6.1 Absolute Maximum Ratings\***

Temperature under Bias  
 Expanded ..... -20 °C to +70 °C  
 Storage Temperature..... -65 °C to +125 °C  
 Voltage On Any Pin (except RP#)  
 ..... -2.0 V to +7.0 V<sup>(1)</sup>  
 RP# Voltage with Respect to  
 GND during Lock-Bit  
 Configuration Operations-2.0 V to +14.0 V<sup>(1,2,3)</sup>  
 Output Short Circuit Current..... 100 mA<sup>(4)</sup>

NOTICE: This datasheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

*\*WARNING: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.*

**NOTES:**

1. All specified voltages are with respect to GND. Minimum DC voltage is -0.5 V on input/output pins and -0.2 V on V<sub>CC</sub> and V<sub>PEN</sub> pins. During transitions, this level may undershoot to -2.0 V for periods <20 ns. Maximum DC voltage on input/output pins, V<sub>CC</sub>, and V<sub>PEN</sub> is V<sub>CC</sub> +0.5 V which, during transitions, may overshoot to V<sub>CC</sub> +2.0 V for periods <20 ns.
2. Maximum DC voltage on RP# may overshoot to +14.0 V for periods <20 ns.
3. RP# voltage is normally at V<sub>IL</sub> or V<sub>IH</sub>. Connection to supply of V<sub>IH</sub> is allowed for a maximum cumulative period of 80 hours.
4. Output shorted for no more than one second. No more than one output shorted at a time.

**6.2 Operating Conditions**

**Temperature and V<sub>CC</sub> Operating Conditions**

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T <sub>A</sub>	Operating Temperature		-20	+70	°C	Ambient Temperature
V <sub>CC</sub>	V <sub>CC1</sub> Supply Voltage (5 V ± 10%)		4.50	5.50	V	
V <sub>CCQ1</sub>	V <sub>CCQ1</sub> Supply Voltage (5 V ± 10%)		4.50	5.50	V	
V <sub>CCQ2</sub>	V <sub>CCQ2</sub> Supply Voltage (2.7V-3.6 V)		2.70	3.60	V	

**6.3 Capacitance<sup>(1)</sup>**

T<sub>A</sub> = +25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C <sub>IN</sub>	Input Capacitance	6	8	pF	V <sub>IN</sub> = 0.0 V
C <sub>OUT</sub>	Output Capacitance	8	12	pF	V <sub>OUT</sub> = 0.0 V

**NOTE:**

1. Sampled, not 100% tested.

**6.4 DC Characteristics**

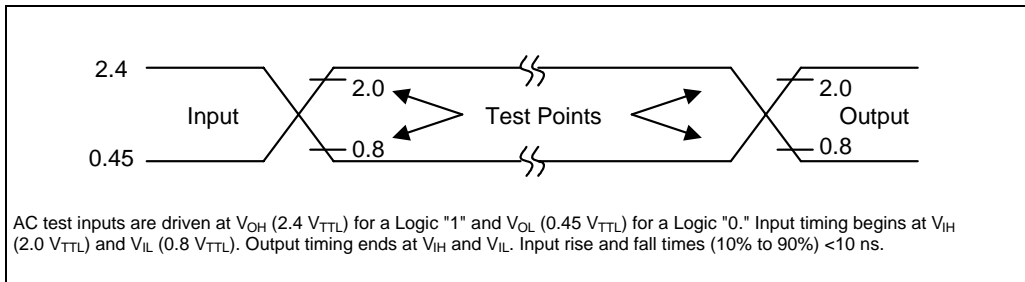
Sym	Parameter	Notes	Typ	Max	Unit	Test Conditions
I <sub>LI</sub>	Input and V <sub>PEN</sub> Load Current	1		±1	μA	V <sub>CC</sub> = V <sub>CC</sub> Max V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>LO</sub>	Output Leakage Current	1		±10	μA	V <sub>CC</sub> = V <sub>CC</sub> Max V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current	1,3,5	80	150	μA	CMOS Inputs, V <sub>CC</sub> = V <sub>CC</sub> Max, CE <sub>0</sub> = CE <sub>1</sub> = CE <sub>2</sub> = RP# = V <sub>CCQ1</sub> ± 0.2 V
			450	900	μA	CMOS Inputs, RP# = V <sub>CC</sub> = V <sub>CC</sub> Max, CE <sub>0</sub> = CE <sub>1</sub> = CE <sub>2</sub> = V <sub>CCQ2</sub> Min
			325	650	μA	CMOS Inputs, RP# = V <sub>CC</sub> = V <sub>CC</sub> Max, CE <sub>2</sub> = GND, CE <sub>0</sub> = CE <sub>1</sub> = V <sub>CCQ2</sub> Min
			210	400	μA	CMOS Inputs, RP# = V <sub>CC</sub> = V <sub>CC</sub> Max, CE <sub>1</sub> = CE <sub>2</sub> = GND, CE <sub>0</sub> = V <sub>CCQ2</sub> Min or CE <sub>0</sub> = CE <sub>2</sub> = GND, CE <sub>1</sub> = V <sub>CCQ2</sub> Min
			0.71	2	mA	TTL Inputs, V <sub>CC</sub> = V <sub>CC</sub> Max, CE <sub>0</sub> = CE <sub>1</sub> = CE <sub>2</sub> = RP# = V <sub>IH</sub>
I <sub>CCD</sub>	V <sub>CC</sub> Power-Down Current		80	125	μA	RP# = GND ± 0.2V I <sub>OUT</sub> (STS) = 0 mA
I <sub>CCR</sub>	V <sub>CC</sub> Read Current	1,5,6	35	55	mA	CMOS Inputs, V <sub>CC</sub> = V <sub>CCQ</sub> = V <sub>CC</sub> Max Device is enabled (see Table 2, <i>Chip Enable Truth Table</i> ) f = 5 MHz I <sub>OUT</sub> = 0 mA
			45	65	mA	TTL Inputs, V <sub>CC</sub> = V <sub>CC</sub> Max Device is enabled (see Table 2, <i>Chip Enable Truth Table</i> ) f = 5 MHz I <sub>OUT</sub> = 0 mA
I <sub>CCW</sub>	V <sub>CC</sub> Program or Set Lock-Bit Current	1,6,7	35	60	mA	CMOS Inputs, V <sub>PEN</sub> = V <sub>CC</sub>
			40	70	mA	TTL Inputs, V <sub>PEN</sub> = V <sub>CC</sub>
I <sub>CCE</sub>	V <sub>CC</sub> Block Erase or Clear Block Lock-Bits Current	1,6,7	35	70	mA	CMOS Inputs, V <sub>PEN</sub> = V <sub>CC</sub>
			40	80	mA	TTL Inputs, V <sub>PEN</sub> = V <sub>CC</sub>
I <sub>CCES</sub>	V <sub>CC</sub> Block Erase Suspend Current	1,2		10	mA	Device is disabled (see Table 2, <i>Chip Enable Truth Table</i> )

## 6.4 DC Characteristics (Continued)

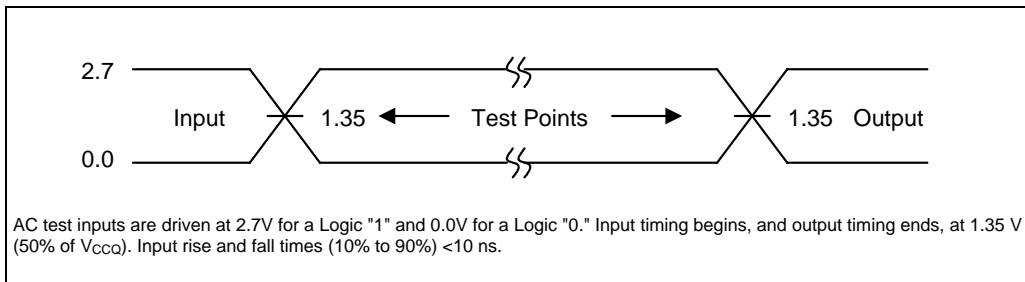
Sym	Parameter	Notes	Min	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	7	-0.5	0.8	V	
V <sub>IH</sub>	Input High Voltage	7	2.0	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage	3,7		0.45	V	V <sub>CCQ</sub> = V <sub>CCQ1</sub> Min I <sub>OL</sub> = 5.8 mA
				0.4	V	V <sub>CCQ</sub> = V <sub>CCQ2</sub> Min I <sub>OL</sub> = 2 mA
V <sub>OH1</sub>	Output High Voltage (TTL)	3,7	2.4		V	V <sub>CCQ</sub> = V <sub>CCQ1</sub> Min or V <sub>CCQ</sub> = V <sub>CCQ2</sub> Min I <sub>OH</sub> = -2.5 mA (V <sub>CCQ1</sub> ) -2 mA (V <sub>CCQ2</sub> )
V <sub>OH2</sub>	Output High Voltage (CMOS)	3,7	0.85 V <sub>CCQ</sub>		V	V <sub>CCQ</sub> = V <sub>CCQ1</sub> Min or V <sub>CCQ</sub> = V <sub>CCQ2</sub> Min I <sub>OH</sub> = -2.5 mA
			V <sub>CCQ</sub> -0.4		V	V <sub>CCQ</sub> = V <sub>CCQ1</sub> Min or V <sub>CCQ</sub> = V <sub>CCQ2</sub> Min I <sub>OH</sub> = -100 μA
V <sub>PENLK</sub>	V <sub>PEN</sub> Lockout during Normal Operations	4,7,11	3.6		V	
V <sub>PENH</sub>	V <sub>PEN</sub> during Block Erase, Program, or Lock-Bit Operations	4,11	4.5	5.5	V	
V <sub>LKO</sub>	V <sub>CC</sub> Lockout Voltage	8	3.25		V	
V <sub>HH</sub>	RP# Unlock Voltage	9,10	11.4	12.6	V	Set master lock-bit Override lock-bit

## NOTES:

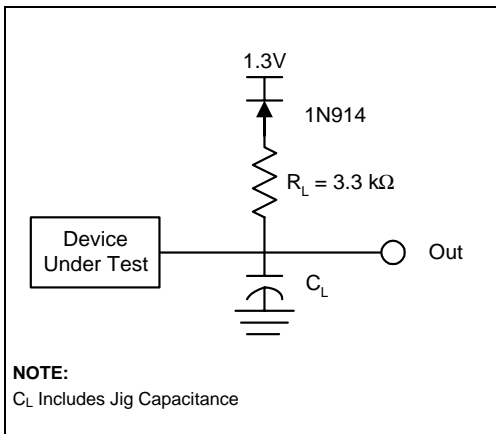
- All currents are in RMS unless otherwise noted. These currents are valid for all product versions (packages and speeds). Contact Intel's Application Support Hotline or your local sales office for information about typical specifications.
- I<sub>CCES</sub> is specified with the device de-selected. If the device is read or written while in erase suspend mode, the device's current draw is I<sub>CCR</sub> or I<sub>CCW</sub>.
- Includes STS.
- Block erases, programming, and lock-bit configurations are inhibited when V<sub>PEN</sub> ≤ V<sub>PENLK</sub>, and not guaranteed in the range between V<sub>PENLK</sub> (max) and V<sub>PENH</sub> (min), and above V<sub>PENH</sub> (max).
- CMOS inputs are either V<sub>CC</sub> ± 0.2 V or GND ± 0.2 V. TTL inputs are either V<sub>IL</sub> or V<sub>IH</sub>.
- Add 5 mA for V<sub>CCQ</sub> = V<sub>CCQ2</sub> min.
- Sampled, not 100% tested.
- Block erases, programming, and lock-bit configurations are inhibited when V<sub>CC</sub> < V<sub>LKO</sub>, and not guaranteed in the range between V<sub>LKO</sub> (min) and V<sub>CC</sub> (min), and above V<sub>CC</sub> (max).
- Master lock-bit set operations are inhibited when RP# = V<sub>IH</sub>. Block lock-bit configuration operations are inhibited when the master lock-bit is set and RP# = V<sub>IH</sub>. Block erases and programming are inhibited when the corresponding block-lock bit is set and RP# = V<sub>IH</sub>. Block erase, program, and lock-bit configuration operations are not guaranteed and should not be attempted with V<sub>IH</sub> < RP# < V<sub>HH</sub>.
- RP# connection to a V<sub>HH</sub> supply is allowed for a maximum cumulative period of 80 hours.
- Tie V<sub>PEN</sub> to V<sub>CC</sub> (4.5 V–5.5 V).



**Figure 13. Transient Input/Output Reference Waveform for  $V_{CCQ} = 5.0\text{ V} \pm 10\%$  (Standard Testing Configuration)**



**Figure 14. Transient Input/Output Reference Waveform for  $V_{CCQ} = 2.7\text{ V} - 3.6\text{ V}$**



**Figure 15. Transient Equivalent Testing Load Circuit**

**Test Configuration Capacitance Loading Value**

Test Configuration	$C_L$ (pF)
$V_{CCQ} = 5.0\text{ V} \pm 10\%$	100
$V_{CCQ} = 2.7\text{ V} - 3.6\text{ V}$	50

## 6.5 AC Characteristics—Read-Only Operations<sup>(1)</sup>

Versions (All units in ns unless otherwise noted)		5 V ± 10% V <sub>CCQ</sub>		-100/-150 <sup>(4)</sup>		-120 <sup>(4)</sup>		
		2.7 V—3.6V V <sub>CCQ</sub>		-100/-150 <sup>(4)</sup>		-120 <sup>(4)</sup>		
#	Sym	Parameter		Notes	Min	Max	Min	Max
R1	t <sub>AVAV</sub>	Read/Write Cycle Time		32 Mbit	100		120	
				64 Mbit	150			
R2	t <sub>AVQV</sub>	Address to Output Delay		32 Mbit		100		120
				64 Mbit		150		
R3	t <sub>ELQV</sub>	CE <sub>x</sub> to Output Delay		32 Mbit	2	100		120
				64 Mbit	2	150		
R4	t <sub>GLQV</sub>	OE# to Output Delay		2		50		50
R5	t <sub>PHQV</sub>	RP# High to Output Delay		32 Mbit		180		180
				64 Mbit		210		
R6	t <sub>ELQX</sub>	CE <sub>x</sub> to Output in Low Z		3	0		0	
R7	t <sub>GLQX</sub>	OE# to Output in Low Z		3	0		0	
R8	t <sub>EHQZ</sub>	CE <sub>x</sub> High to Output in High Z		3		55		55
R9	t <sub>GHQZ</sub>	OE# High to Output in High Z		3		15		15
R10	t <sub>OH</sub>	Output Hold from Address, CE <sub>x</sub> , or OE# Change, Whichever Occurs First		3	0		0	
R11	t <sub>ELFL</sub>	CE <sub>x</sub> Low to BYTE# High or Low		3		10		10
	t <sub>ELFH</sub>							
R12	t <sub>FLQV</sub>	BYTE# to Output Delay				1000		1000
	t <sub>FHQV</sub>							
R13	t <sub>FLQZ</sub>	BYTE# to Output in High Z		3		1000		1000
R14	t <sub>EHQL</sub>	CE <sub>x</sub> Pulse width		3	10		10	

### NOTES:

CE<sub>x</sub> low is defined as the first edge of CE<sub>0</sub>, CE<sub>1</sub>, or CE<sub>2</sub> that enables the device. CE<sub>x</sub> high is defined at the first edge of CE<sub>0</sub>, CE<sub>1</sub>, or CE<sub>2</sub> that disables the device (see Table 2, *Chip Enable Truth Table*).

- See Figure 16, *AC Waveform for Read Operations* for the maximum allowable input slew rate.
- OE# may be delayed up to t<sub>ELQV</sub>-t<sub>GLQV</sub> after the first edge of CE<sub>0</sub>, CE<sub>1</sub>, or CE<sub>2</sub> that enables the device (see Table 2, *Chip Enable Truth Table*) without impact on t<sub>ELQV</sub>.
- Sampled, not 100% tested.
- See Figures 13–15, *Transient Input/Output Reference Waveform for V<sub>CCQ</sub> = 5.0 V ± 10%*, *Transient Input/Output Reference Waveform for V<sub>CCQ</sub> = 2.7 V – 3.6 V*, and *Transient Equivalent Testing Load Circuit* for testing characteristics.

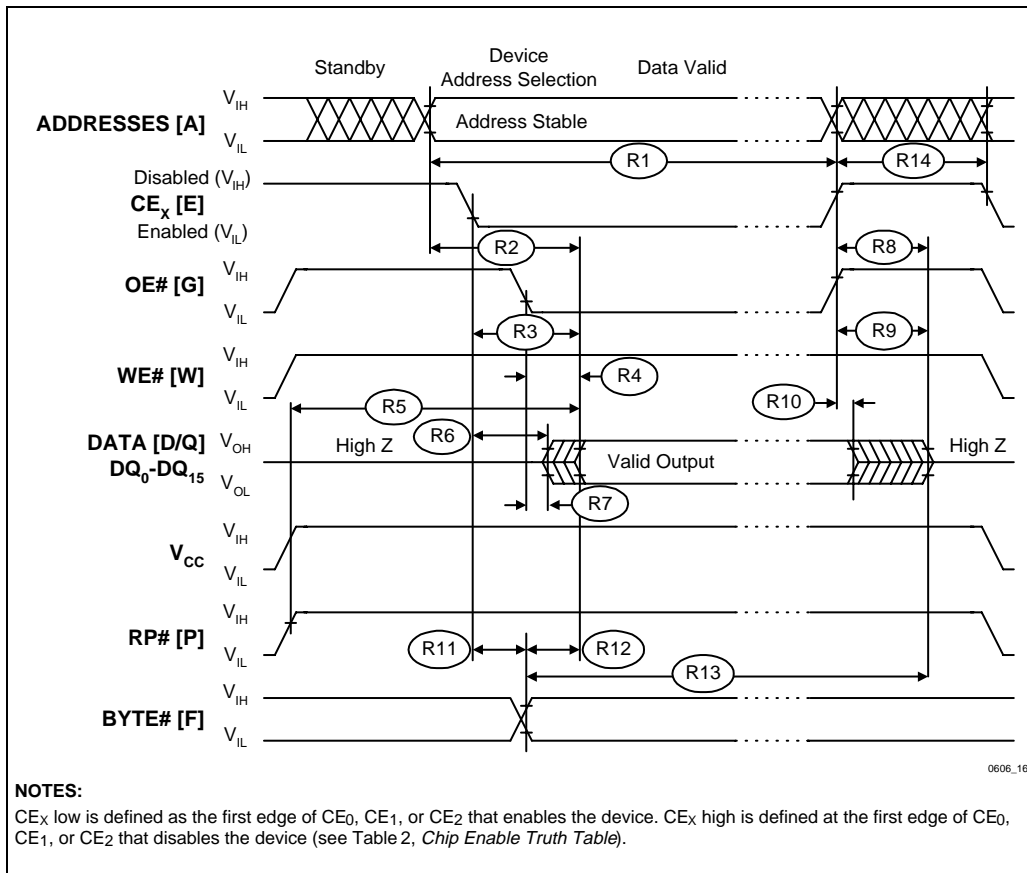


Figure 16. AC Waveform for Read Operations

## 6.6 AC Characteristics— Write Operations<sup>(1,2)</sup>

Versions				Valid for All Speeds		Unit
#	Sym	Parameter	Notes	Min	Max	
W1	t <sub>PHWL</sub> (t <sub>PHL</sub> )	RP# High Recovery to WE# (CE <sub>x</sub> ) Going Low	3	1		μs
W2	t <sub>ELWL</sub> (t <sub>WLEL</sub> )	CE <sub>x</sub> (WE#) Low to WE# (CE <sub>x</sub> ) Going Low	8	0		ns
W3	t <sub>WP</sub>	Write Pulse Width	8	70		ns
W4	t <sub>DVWH</sub> (t <sub>DVEH</sub> )	Data Setup to WE# (CE <sub>x</sub> ) Going High	4	50		ns
W5	t <sub>AVWH</sub> (t <sub>AVEH</sub> )	Address Setup to WE# (CE <sub>x</sub> ) Going High	4	50		ns
W6	t <sub>WHEH</sub> (t <sub>EHWH</sub> )	CE <sub>x</sub> (WE#) Hold from WE# (CE <sub>x</sub> ) High		10		ns
W7	t <sub>WHDX</sub> (t <sub>EHDX</sub> )	Data Hold from WE# (CE <sub>x</sub> ) High		0		ns
W8	t <sub>WHAX</sub> (t <sub>EHAX</sub> )	Address Hold from WE# (CE <sub>x</sub> ) High		0		ns
W9	t <sub>WPH</sub>	Write Pulse Width High	9	30		ns
W10	t <sub>PHHWH</sub> (t <sub>PHHEH</sub> )	RP# V <sub>HH</sub> Setup to WE# (CE <sub>x</sub> ) Going High	3	0		ns
W11	t <sub>VPWH</sub> (t <sub>VPEH</sub> )	V <sub>PEN</sub> Setup to WE# (CE <sub>x</sub> ) Going High	3	0		ns
W12	t <sub>WHGL</sub> (t <sub>EHGL</sub> )	Write Recovery before Read	6	35		ns
W13	t <sub>WHRL</sub> (t <sub>EHRL</sub> )	WE# (CE <sub>x</sub> ) High to STS Going Low	5		90	ns
W14	t <sub>QVPH</sub>	RP# V <sub>HH</sub> Hold from Valid SRD, STS Going High	3,5,7	0		ns
W15	t <sub>QVVL</sub>	V <sub>PEN</sub> Hold from Valid SRD, STS Going High	3,5,7	0		ns

### NOTES:

CE<sub>x</sub> low is defined as the first edge of CE<sub>0</sub>, CE<sub>1</sub>, or CE<sub>2</sub> that enables the device. CE<sub>x</sub> high is defined at the first edge of CE<sub>0</sub>, CE<sub>1</sub>, or CE<sub>2</sub> that disables the device (see Table 2, *Chip Enable Truth Table*).

- Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to *AC Characteristics—Read-Only Operations*.
- A write operation can be initiated and terminated with either CE<sub>x</sub> or WE#.
- Sampled, not 100% tested.
- Refer to Table 4 for valid A<sub>IN</sub> and D<sub>IN</sub> for block erase, program, or lock-bit configuration.
- STS timings are based on STS configured in its RY/BY# default mode.
- For array access, t<sub>AVQV</sub> is required in addition to t<sub>WHGL</sub> for any accesses after a write.
- V<sub>PEN</sub> should be held at V<sub>PENH</sub> (and if necessary RP# should be held at V<sub>HH</sub>) until determination of block erase, program, or lock-bit configuration success (SR.1/3/4/5 = 0).
- Write pulse width (t<sub>WP</sub>) is defined from CE<sub>x</sub> or WE# going low (whichever goes low first) to CE<sub>x</sub> or WE# going high (whichever goes high first). Hence, t<sub>WP</sub> = t<sub>WLWH</sub> = t<sub>LEH</sub> = t<sub>WLEH</sub> = t<sub>ELWH</sub>. If CE<sub>x</sub> is driven low 10 ns before WE# going low, WE# pulse width requirement decreases to t<sub>WP</sub> - 10 ns.
- Write pulse width high (t<sub>WPH</sub>) is defined from CE<sub>x</sub> or WE# going high (whichever goes high first) to CE<sub>x</sub> or WE# going low (whichever goes low first). Hence, t<sub>WPH</sub> = t<sub>WHWL</sub> = t<sub>EHL</sub> = t<sub>WHEL</sub> = t<sub>EHWL</sub>.



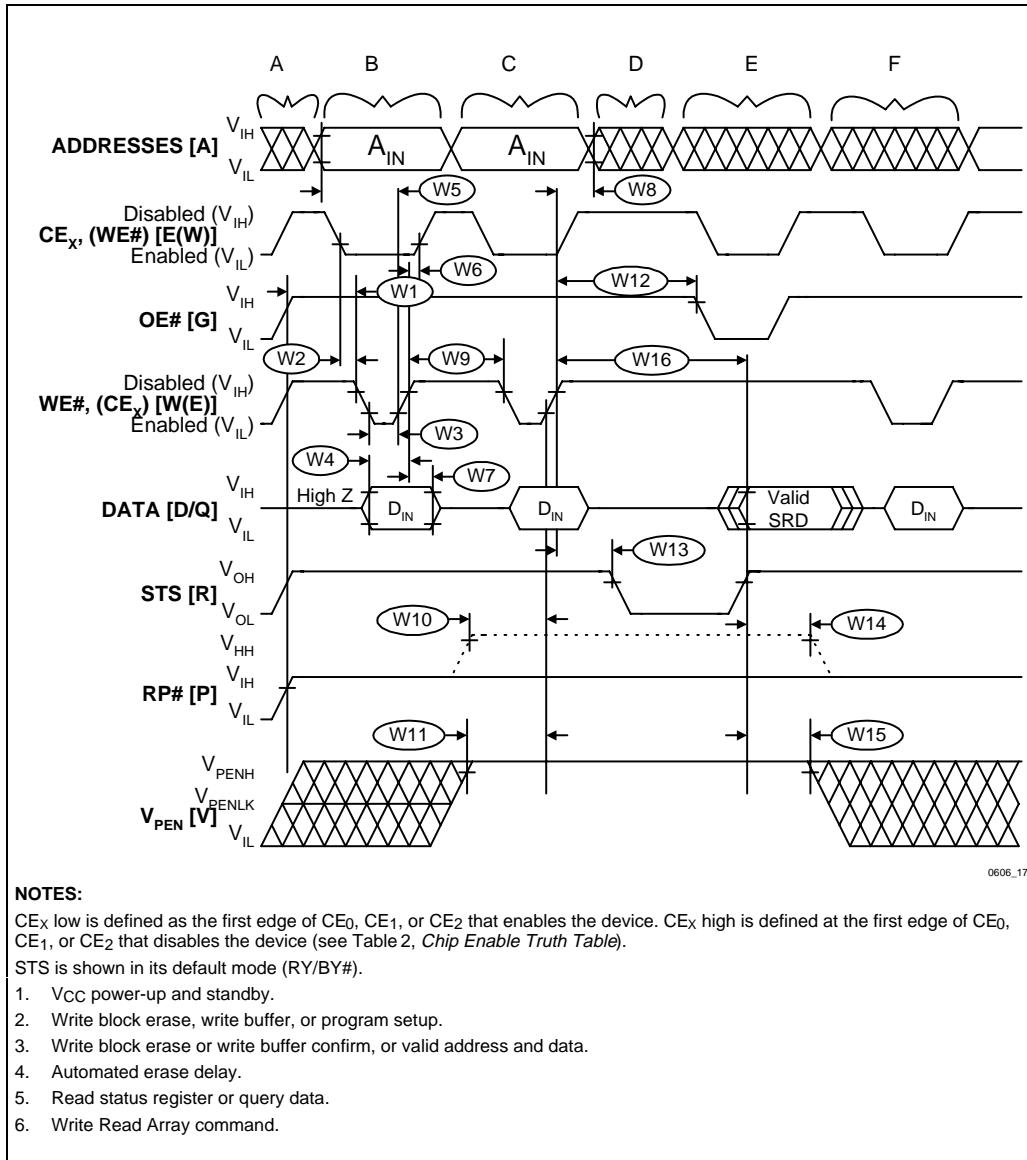


Figure 17. AC Waveform for Write Operations

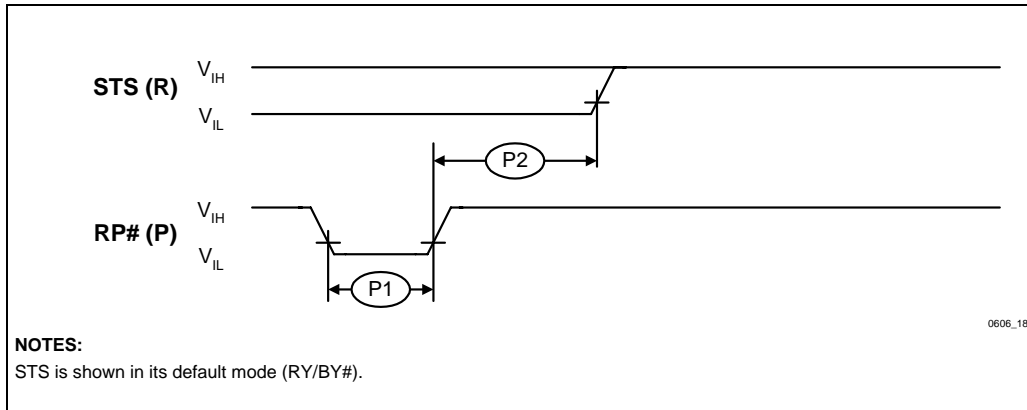


Figure 18. AC Waveform for Reset Operation

Reset Specifications<sup>(1)</sup>

#	Sym.	Parameter	Notes	Min	Max	Unit
P1	t <sub>PLPH</sub>	RP# Pulse Low Time (If RP# is tied to V <sub>CC</sub> , this specification is not applicable)	2	35		µs
P2	t <sub>PHRH</sub>	RP# High to Reset during Block Erase, Program, or Lock-Bit Configuration	3		100	ns

**NOTES:**

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, program, or lock-bit configuration operation is not executing then the minimum required RP# Pulse Low Time is 100 ns.
3. A reset time, t<sub>PHQV</sub>, is required from the latter of STS (in RY/BY# mode) or RP# going high until outputs are valid.

**6.7 Block Erase, Program, and Lock-Bit Configuration Performance<sup>(3,4)</sup>**

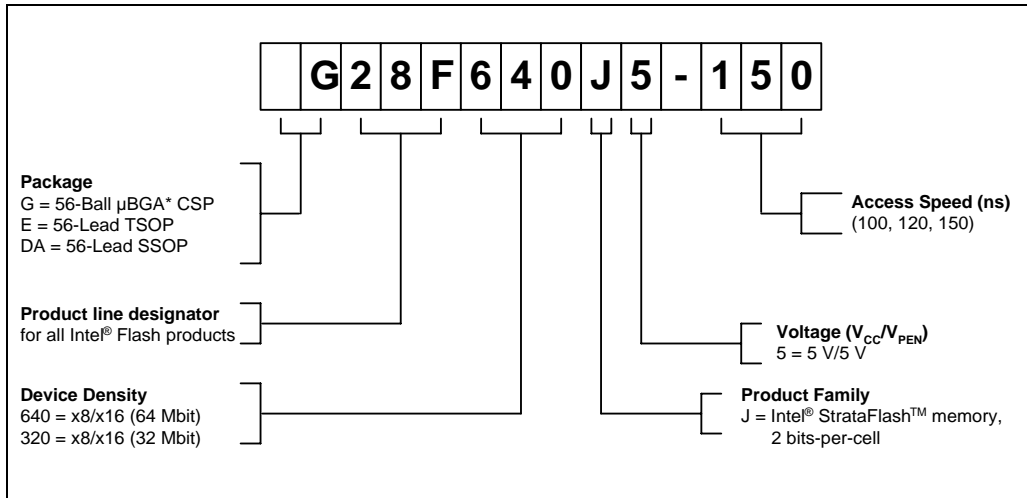
#	Sym	Parameter	Notes	Min	Typ <sup>(1)</sup>	Max	Unit
W16	t <sub>WHQV1</sub> t <sub>EHQV1</sub>	Write Buffer Byte Program Time	2,5	TBD	6.3	TBD	µs
W16	t <sub>WHQV2</sub> t <sub>EHQV2</sub>	Write Buffer Word Program Time	2,5	TBD	12.6	TBD	µs
W16	t <sub>WHQV3</sub> t <sub>EHQV3</sub>	Byte Program Time (Using Word/Byte Program Command)	2	TBD	180	TBD	µs
		Block Program Time (Using Write to Buffer Command)	2	TBD	0.8	TBD	sec
W16	t <sub>WHQV4</sub> t <sub>EHQV4</sub>	Block Erase Time	2	TBD	0.7	TBD	sec
W16	t <sub>WHQV5</sub> t <sub>EHQV5</sub>	Set Lock-Bit Time	2	TBD	32	TBD	µs
W16	t <sub>WHQV6</sub> t <sub>EHQV6</sub>	Clear Block Lock-Bits Time	2	TBD	0.3	TBD	sec
W16	t <sub>WHRH</sub> t <sub>EHRH</sub>	Erase Suspend Latency Time to Read			26	TBD	µs

**NOTES:**

1. Typical values measured at T<sub>A</sub> = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.



7.0 ORDERING INFORMATION



Order Code by Density			Valid Operational Conditions	
			5 V V <sub>CC</sub>	
32 Mbit		64 Mbit	2.7 V – 3.6 V V <sub>CCQ</sub>	5 V ± 10% V <sub>CCQ</sub>
DA28F320J5-100	DA28F320J5-120	DA28F640J5-150	Yes	Yes
E28F320J5-100	E28F320J5-120		Yes	Yes
		G28F640J5-150	Yes	Yes



**8.0 ADDITIONAL INFORMATION(1,2)**

Order Number	Document
210830	<i>Flash Memory Databook</i>
292123	<i>AP-374 Flash Memory Write Protection Techniques</i>
292203	<i>AP-644 Intel® StrataFlash™ Memory Migration Guide</i>
292204	<i>AP-646 Common Flash Interface (CFI) and Command Sets</i>
292205	<i>AP-647 Intel® StrataFlash™ Memory Design Guide</i>
297848	<i>Intel® StrataFlash™ Memory 32 and 64 Mbit Specification Update</i>

**NOTE:**

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at <http://www.intel.com> for technical documentation and tools.