82562ET 10/100 Mbps Platform LAN Connect (PLC)

Networking Silicon

Datasheet

Product Features

- IEEE 802.3 10BASE-T/100BASE-TX compliant physical layer interface
- IEEE 802.3u Auto-Negotiation support
- Digital Adaptive Equalization control
- Link status interrupt capability
- XOR tree mode support
- 3-port LED support (speed, link and activity)
- 10BASE-T auto-polarity correction
- LAN Connect Interface
- Diagnostic loopback mode
- 1:1 transmit transformer ratio support
- Low power (less than 300 mW in active transmit mode)
- Reduced power in “unplugged mode” (less than 50 mW)
- Automatic detection of “unplugged mode”
- 3.3 V device
- 48-pin Shrink Small Outline Package

Revision 1.3
March 2003

Revision History

Revision	Revision Date	Description
1.3	March 2003	Added product ordering code in Section 1.0.
1.2	October 2001	Removed confidential status. • Removed sections: “Physical Layer Interface Functionality” and “Platform LAN Connect”. • Changed “Electrical and Timing Specifications” section to “Voltage and Temperature Specifications” and removed timing specifications.
1.1	June 2000	Advance Information Datasheet release (Intel Confidential). • On cover page, replaced Boundary Scan Support with XOR tree mode support. Added bullet for LAN Connect I/F. • Pg. 3, added a Solution Block Diagram as included in OR-2338 Pg. 4 but replaced EM with ET in diagram. • Pg. 11, removed Figure 4, “NRZ to MLT-3 Encoding Diagram”. • Pg. 35, changed the Rev. number on the 82562 Pinout symbol to 1.0.
1.0	May 2000	Advance Information Datasheet release (Intel Secret). • Modified Table 1 “82562ET Hardware Configuration” to add one row for XOR Tree and include column for comments. • Updated the descrition of the Activity LED signal in Section 3.6, “LED Pins”. • Revised Section 3.7, “Miscellaneous Control Pins” to reflect references to Table 1 “82562ET Hardware Configuration”. • Updated Section 4.0, “Voltage and Temperature Specifications”. • Replaced diagrams in Section 5.1, “Package Information”.
0.6	Nov. 1999	• Corrected Figure 4 “NRZ to MLT-3 Encoding Diagram on Pg. 11 to reflect correct signal transitions. • Removed “10BASE-T Error Detection and Reporting” section since the 82562 does not do 10BASE-T error reporting.
0.55	Sept. 1999	Initial release.

Contents

1.0 Introduction

1.1 Overview

The Intel® 82562ET is a highly-integrated Platform LAN Connect device designed for 10 or 100 Mbps Ethernet systems. It is based on the IEEE 10BASE-T and 100BASE-TX standards. The IEEE 802.3u standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable.

The 82562ET complies with the IEEE 802.3u Auto-Negotiation standard and the IEEE 802.3x Full Duplex Flow Control standard. The 82563ET also includes a PHY interface compliant to the current platform LAN connect interface.

1.2 Features

- IEEE 802.3 10BASE-T/100BASE-TX compliant physical layer interface
- IEEE 802.3u Auto-Negotiation support
- Digital Adaptive Equalization control
- Link status interrupt capability
- XOR Tree mode support for board testing
- 3-port LED support (speed, link and activity)
- 10BASE-T auto-polarity correction
- Diagnostic loopback mode
- 1:1 transmit transformer ratio support
- Low power (less than 300 mW in active transmit mode)
- Reduced power in “unplugged mode” (less than 50 mW)
- Automatic detection of “unplugged mode”
- 3.3 V device
- 48-pin Shrink Small Outline Package
- Platform LAN connect interface support

1.3 References

- IEEE 802.3 Standard for Local and Metropolitan Area Networks, Institute of Electrical and Electronics Engineers
- 82555 10/100 Mbps LAN Physical Layer Interface Datasheet, Intel Corporation
- LAN Connect Interface Specification, Intel Corporation

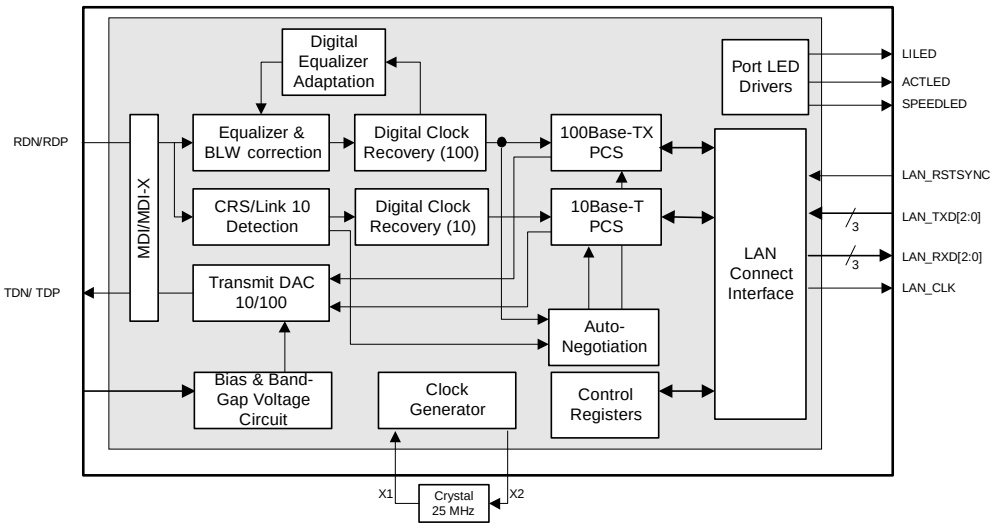
1.4 Product Code

The product ordering code for the 82562ET is: DA82562ET.

2.0 82562ET Architectural Overview

The 82562ET is a highly integrated Platform LAN Connect device that combines a 10BASE-T and 100BASE-TX physical layer interfaces. The 82562ET supports a single interface fully compliant with the IEEE 802.3 standard. Figure 1 provides a block diagram of the 82562ET architecture.

Figure 1. 82562ET Block Diagram



The 8252ET is a 3.3 V device in a 48-pin Shrink Small Outline Package (SSOP). This document describes the architecture of the device in all modes of operation.

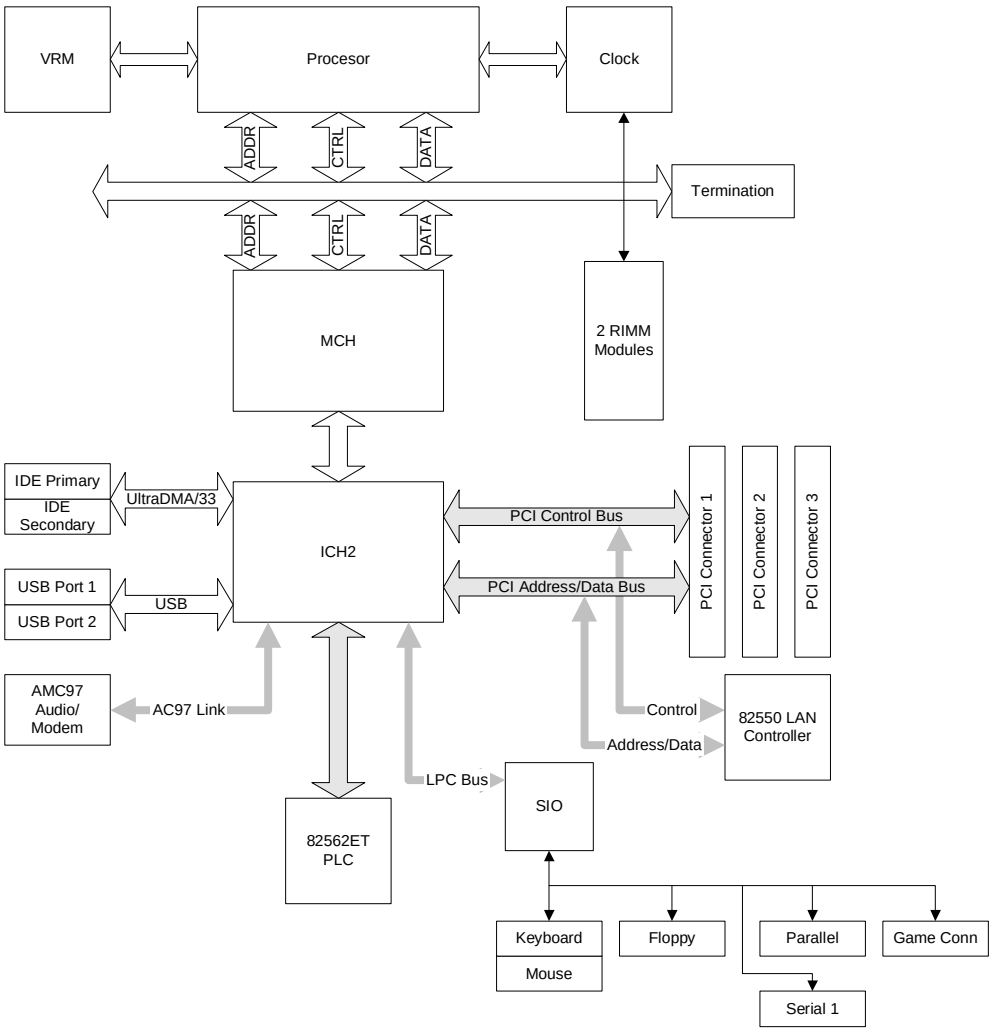
Four pins, test Enable (TESTEN), Test Clock (ISOL_TCK), Test Input (ISOL_TI), and Test Execute (ISOL_EX), define the general operation of the device. Table 1 shows the pin settings for the different modes of operation.

Table 1. 82562ET Hardware Configuration

Mode of Operation	TESTEN	ISOL_TCK	ISOL_TI	ISOL_EX	Comments
Normal operating mode	0	0	0	0	The ISOL_TCK, ISOL_TI, and ISOL_EX pins can remain floating.
Isolate mode (Tri-state and full power-down mode)	0	1	1	1	The device is in tri-state and power-down mode.
	1	1	1	1	The device is in tri-state and the fully powered down.
XOR Tree	1	0	0	0	The XOR Tree is used for board testing and tri-state mode.

NOTE: Combinations not shown in Table 1 are reserved and should not be used.

Figure 2. 82562ET Solution Overview



3.0 82562ET Signal Descriptions

3.1 Signal Type Definitions

Type	Name	Description
I	Input	Input pin to the 82562ET.
O	Output	Output pin from the 82562ET.
I/O	Input/Output	Multiplexed input and output pin to and from the 82562ET.
MLT	Multi-level analog I/O	Multi-level analog pin used for input and output.
B	Bias	Bias pin used for ground connection through a resistor or an external voltage reference.
DPS	Digital Power Supply	Digital power or ground pin for the 82562ET.
APS	Analog Power Supply	Analog power or ground pin for the 82562ET.

3.2 Twisted Pair Ethernet (TPE) Pins

Pin Name	Pin Number	Type	Description
TDP TDN	10 11	MLT	**Transmit Differential Pair.** The transmit differential pair sends serial bit streams to the unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T (Manchester) mode and a three-level signal in 100BASE-TX mode (MLT-3). These signals directly interface with the isolation transformer.
RDP RDN	15 16	MLT	**Receive Differential Pair.** The receive differential pair receive the serial bit stream from an unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T mode (Manchester) or a three-level signal in 100BASE-TX mode (MLT-3). These signals directly interface with an isolation transformer.

3.3 External Bias Pins

Pin Name	Pin Number	Type	Description
RBIAS10	4	B	**Bias Reference Resistor 10.** This pin should be connected to a 549 Ω pull-down resistor.[a]
RBIAS100	5	B	**Bias reference Resistor 100.** This pin should be connected to a 619 Ω pull-down resistor.[b]

a. 549 Ω for RBIAS10 is only a recommended value and should be fine tuned for various designs.
b. 619 Ω for RBIAS100 is only a recommended value and should be fine tuned for various designs.

3.4 Clock Pins

Pin Name	Pin Number	Type	Description
X1	46	I	**Crystal Input Clock.** X1 and X2 can be driven by an external 25 MHz crystal of 50 PPM or better. Otherwise, X1 is driven by an external metal-oxide semiconductor (MOS) level 25 MHz oscillator when X2 is left floating.
X2	47	O	**Crystal Output Clock.** X1 and X2 can be driven by an external 25 MHz crystal of 50 PPM or better.

3.5 Platform LAN Connect Interface Pins

Pin Name	Pin Number	Type	Description
LAN_CLK	39	O	**LAN Connect Clock.** The LAN Connect Clock is driven by the 82562ET on two frequencies depending on operation speed. When the 82562ET is in 100BASE-TX mode, LAN_CLK drives a 50 MHz clock. Otherwise, LAN_CLK drives a 5 MHz clock for 10BASE-T. The LAN_CLK does not stop during normal operation.
LAN_ RSTSYNC	42	I	**Reset/Synchronize.** This is a multiplexed pin and is driven by the Media Access Control (MAC) layer device. Its functions are: • Reset. When this pin is asserted beyond one LAN Connect clock period, the 82562ET uses this signal Reset. To ensure reset of the 82562ET, the Reset signal should remain active for at least 500 µseconds. • Synchronize. When this pin is activated synchronously, for only one LAN Connect clock period, it is used to synchronize the MAC and PHY on LAN Connect word boundaries.
LAN_ TXD[2:0]	45, 44, 43	I	**LAN Connect Transmit Data.** The LAN Connect transmit pins are used to transfer data from the MAC device to the 82562ET. These pins are used to move transmitted data and real time control and management data. They also transmit out of band control data from the MAC to the PHY. The pins should be fully synchronous to LAN_CLK.
LAN_ RXD[2:0]	37, 35, 34	O	**LAN Connect Receive Data.** The LAN Connect receive pins are used to transfer data from the 82562ET to the MAC device. These pins are used to move received data and real time control and management data. They also move out of band control data from the PHY to the MAC. These pins are synchronous to LAN_CLK.

3.6 LED Pins

Pin Name	Pin Number	Type	Description
LILED#	27	O	**Link Integrity LED.** The LED is active low and the Link Integrity LED pin indicates link status in either 10BASE-T or 100BASE-TX mode. If a link is present in either mode, the LILED is asserted.
ACTLED#	32	O	**Activity LED.** The LED is active low and the Activity LED signal indicates either receive or transmit activity. When no activity is present, the LED is off. The Activity LED will flicker when activity is present. The flicker rate depends on the activity load. The individual address LED control bit (Word A hexadecimal, bit 4) in the ICH2 EEPROM can select the ACTLED# behavior. It controls the Activity LED (ACTLED) functionality in Wake on LAN (WOL) mode. 0 = In WOL mode, the ACTLED is activated by the transmission and reception of broadcast and individual address match packets. 1 = In WOL mode, the ACTLED is activated by the transmission and reception of individual address match packets only. This bit is configured by the OEM and is activated by a transmission and reception of individual address match packets.
SPDLED#	31	O	**Speed LED.** The LED is active low and the Speed LED signal indicates the speed of operation, either 10 Mbps or 100 Mbps. The Speed LED is on during 100BASE-TX operation and off in 10BASE-T mode.

3.7 Miscellaneous Control Pins

Pin Name	Pin Number	Type	Description
ADV10	41	I	**Advertise 10 Mbps Only.** The Advertise 10 Mbps Only signal is asserted high, and the 82562ET advertises only 10BASE-T technology during Auto-Negotiation processes in this state. Otherwise, the 82562ET advertises all of its technologies. Note: ADV10 has an internal pull-down resistor.
ISOL_TCK	30	I	**Test Clock.** The Test Clock signal sets the device into asynchronous test mode in conjunction with the Test Input, Test Execute and Test Enable pins (refer to Table 1). In the manufacturing test mode, it acts as the test clock. Note: ISOL_TCK has an internal pull-down resistor.
ISOL_TI	28	I	**Test Input.** The Test Input signal sets the device into asynchronous test mode in conjunction with the Test Clock, Test Execute and Test Enable pins (refer to Table 1). In the manufacturing test mode, it acts as the test data input pin. Note: ISOL_TI has an internal pull-down resistor.

Pin Name	Pin Number	Type	Description
ISOL_TEX	29	I	**Test Execute.** The Test Execute signal sets the device into asynchronous test mode in conjunction with the Test Clock, Test Input, and Test Enable pins (refer to Table 1). In the manufacturing test mode, it places the command that was entered through the TI pin in the instruction register. Note: ISOL_TEX has an internal pull-down resistor.
TOUT	26	O	**Test Output.** The Test Output pin is used for Boundary XOR scan output. In the manufacturing test mode, it acts as the test output port.
TESTEN	21	I	**Test Enable.** The Test Enable pin is used to enable test mode and should be pulled down to V_{SS} to allow XOR Tree test mode.

3.8 Power and Ground Connections

Pin Name	Pin Number	Type	Description
VCC VCCP VCCA VCCA2 VCCT	1, 25 36, 40 2, 7, 9, 12, 14, 17	DPS	**Digital 3.3 V Power.** These pins should be connected to the main digital power supply.
VSS VSSP VSSA VSSA2	8, 13, 18 24, 48 33, 38 3 6	DPS	**Digital Ground.** These pins should be connected to the main digital ground.
VCCR	19, 23	APS	**Analog Power.**
VSSR	20, 22	APS	**Analog Ground.** These pins should not be isolated from the main digital.

4.0 Voltage and Temperature Specifications

4.1 Absolute Maximum Ratings

Maximum ratings are listed below:

Case Temperature under Bias . . . . . 0 C to 135 C
Storage Temperature . . . . . -65 C to 150 C
Supply Voltage with respect to V_{SS} . . . . . -0.5 V to 3.45 V
Output Voltages . . . . . -0.50 V to 3.45 V
Input Voltages . . . . . V_{CC} to 3.45 V

Stresses above the listed absolute maximum ratings may cause permanent damage to the 82562ET device. This is a stress rating only and functional operations of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC Characteristics

Table 2. General DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CC}	Supply Voltage		3.0	3.3	3.45	V	
T	Temperature	Minimum/Maximum Case Temperature	0		85	C	
P	Power Consumption	10/100Mbps (transmitter on)		300		mW	
		Reduced Power		50		mW	
		Auto-Negotiation		200		mW	

4.2.1 X1 Clock DC Specifications

Table 3. X1 Clock DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{IL}	Input Low Voltage				0.8	V	
V_{IH}	Input High Voltage		2.0			V	
I_{ILIH}	Input Leakage Currents	$0 < V_{IN} < V_{CC}$			±10	µA	
C_I	Input Capacitance				8	pF	1

NOTES:
1. This characteristic is only characterized, not tested. It is valid for digital pins only.

4.2.2 LAN Connect Interface DC Specifications

Table 4. LAN Connect Interface DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{CCJ}	Input/Output Supply Voltage		3.0		3.45	V	
V_{IL}	Input Low Voltage		-0.5		$0.3V_{CCJ}$	V	
V_{IH}	Input High Voltage		$0.6V_{CCJ}$		V_{CCJ} + 0.5	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{CCJ}$			±10	µA	
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA			$0.1V_{CCJ}$	V	
V_{OH}	Output High Voltage	I_{OUT} = -500 µA	$0.9V_{CCJ}$			V	
C_{IN}	Input Pin Capacitance				8	pF	1

NOTES:
1. This characteristic is only characterized, not tested. It is valid for digital pins only.

4.2.3 LED DC Specifications

Table 5. LED DC Specifications

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OLLED}	Output Low Voltage	I_{OUT} = 10 mA			0.7	V	
V_{OHLED}	Output High Voltage	I_{OUT} = -10 mA	2.4			V	

4.2.4 10BASE-T Voltage and Current DC Specifications

Table 6. 10BASE-T Transmitter

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OD10}	Output Differential Peak Voltage	R_L = 100 Ω	2.2		2.8	V	1

NOTES: Current is measured between the transmit differential pins (TDP and TDN) at 3.3 V.
1. R_L is the resistive load measured across the transmit differential pins, TDP and TDN.

Table 7. 10BASE-T Receiver

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
R_{ID10}	Input Differential Resistance	DC	10			KΩ	1
V_{IDA10}	Input Differential Accept Peak Voltage	5 MHz ≤ f ≤ 10 MHz	585		3100	mV	
V_{IDR10}	Input Differential Reject Peak Voltage	5 MHz ≤ f ≤ 10 MHz			300	mV	
V_{ICM10}	Input Common Mode Voltage			$V_{CC/2}$		V	

NOTES:
1. The input differential resistance is measured across the receive differential pins, RDP and RDN.

4.2.5 100BASE-TX Voltage and Current DC Specifications

Table 8. 100BASE-TX Transmitter

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
V_{OD100}	Output Differential Peak Voltage	R_L = 100 Ω	0.95	1.0	1.05	V	1

NOTES: Current is measured between the transmit differential pins (TDP and TDN) at 3.3 V.
1. R_L is the resistive load measured across the transmit differential pins, TDP and TDN.

Table 9. 100BASE-TX Receiver

Symbol	Parameter	Condition	Min	Typical	Max	Units	Notes
R_{ID100}	Input Differential Resistance	DC	10			KΩ	1
V_{IDA100}	Input Differential Accept Peak Voltage		500		1200	mV	
V_{IDR100}	Input Differential Reject Peak Voltage				100	mV	
V_{ICM100}	Input Common Mode Voltage			$V_{CC/2}$		V	

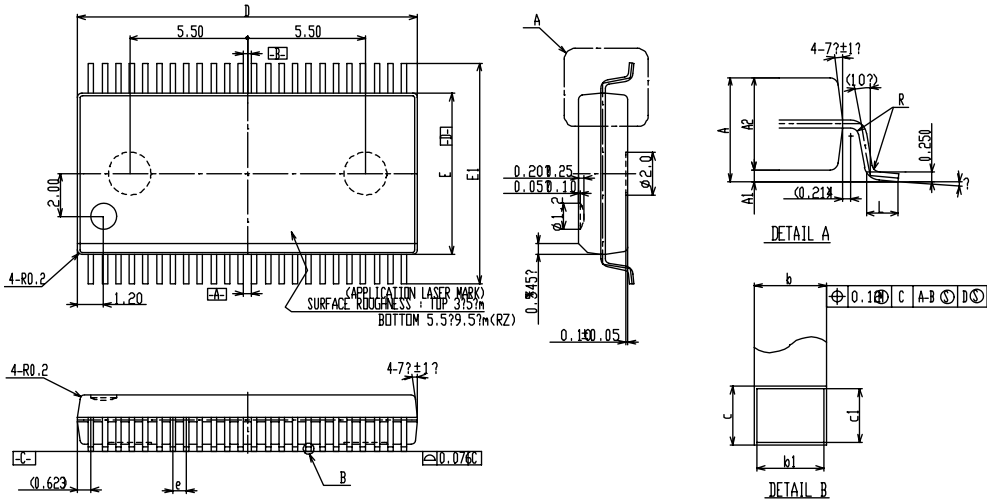
NOTES:
1. The input differential resistance is measured across the receive differential pins, RDP and RDN.

5.0 Package and Pinout Information

5.1 Package Information

The 82562ET is a 48-pin Shrink Small Outlying Package (SSOP). The Package dimensions are shown in Figure 3. More information on Intel device packaging is available in the Intel Packaging Handbook, which is available from the Intel Literature Center or your local sales office.

Figure 3. Dimension Diagram for the 82562ET 48-pin SSOP



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	2.44	2.59	2.74
A1	0.20	0.30	0.40
A2	2.24	2.29	2.34
b	0.22	—	0.30
b1	0.22	0.25	0.28
c	0.18	—	0.25
c1	0.18	0.20	0.22
D	15.75	15.85	15.95
E	7.45	7.50	7.55
E1	10.16	10.285	10.41
L	0.70	0.80	0.90
e	0.635 BSC		
R	0.10	0.20	0.30
?	0?	5?	8?

NOTES)
1. ALL DIMENSIONS ARE IN MILLIMETERS. (ANGLES IN DEGREES)
2. DIMENSIONS ?D? DOES NOT INCLUDE BURRS.
   HOWEVER, DIMENSION INCLUDING PROTRUSIONS OR GATE BURRS
   SHALL BE MAX. 0.20mm.
3. DIMENSION ?E? DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
   INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5.2 Pinout Information

5.2.1 82562ET Pin Assignments

Table 10. 82562ET Pin Assignments

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	VCC	13	VSS	25	VCC	37	LAN_RXD2
2	VCCA	14	VCCT	26	TOUT	38	VSSP
3	VSSA	15	RDP	27	LILED	39	LAN_CLK
4	RBIAS10	16	RDN	28	ISOL_TI	40	VCCP
5	RBIAS100	17	VCCT	29	ISOL_TEX	41	ADV10
6	VSSA2	18	VSS	30	ISOL_TCK	42	LAN_RSTSYNC
7	VCCA2	19	VCCR	31	SPDLED	43	LAN_TXD0
8	VSS	20	VSSR	32	ACTLED	44	LAN_TXD1
9	VCCT	21	TESTEN	33	VSSP	45	LAN_TXD2
10	TDP	22	VSSR	34	LAN_RXD0	46	X1
11	TDN	23	VCCR	35	LAN_RXD1	47	X2
12	VCCT	24	VSS	36	VCCP	48	VSS

5.2.2 82562ET Shrink Small Outlying Package Diagram

Figure 4. 82562ET Pin Out Diagram