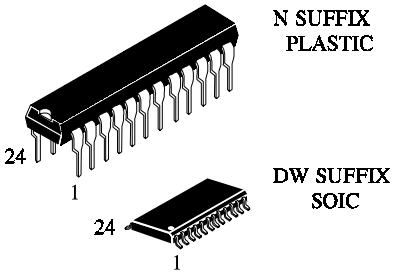
IN74AC652

Octal 3-State Bus Transceivers and D Flip-Flops

High-Speed Silicon-Gate CMOS



ORDERING INFORMATION
IN74AC652N Plastic
IN74AC652DW SOIC
T_A = -40° to 85° C for all packages

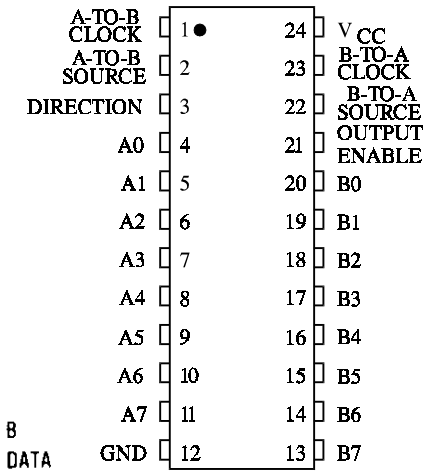
The IN74AC652 is identical in pinout to the LS/ALS652, HC/HCT652. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALS outputs.

These devices consists of bus transceiver circuits, D-type flip-flop, and control circuitry arranged for multiplex transmission of data directly from the data bus or from the internal storage registers. Direction and Output Enable are provided to select the read-time or stored data function. Data on the A or B Data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (A-to-B Clock or B-to-A Clock) regardless of the select or enable or enable control pins. When A-to-B Source and B-to-A Source are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling Direction and Output Enable. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

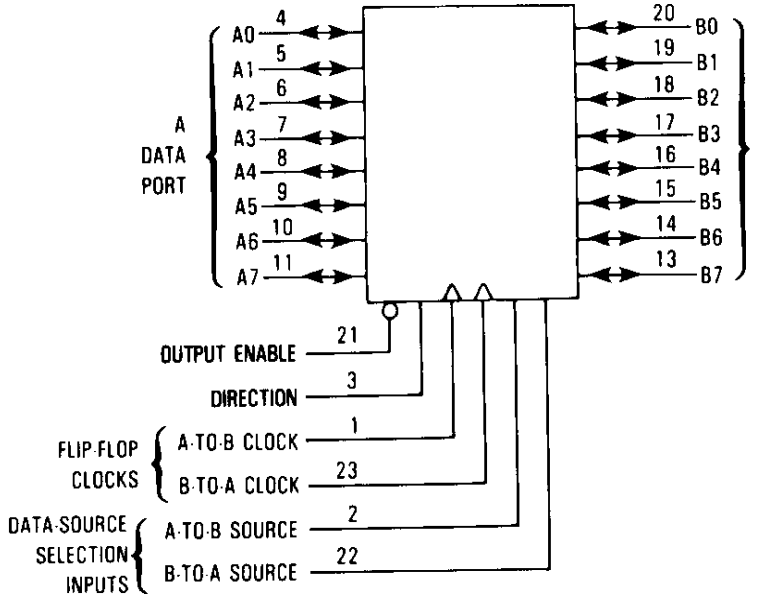
The IN74AC652 has noninverted outputs.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA, 0.1 μA @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 24=V_{CC}
PIN 12 = GND

INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_J	Junction Temperature (PDIP)			140	°C
T_A	Operating Temperature, All Package Types		-40	+85	°C
I_{OH}	Output Current - High			-24	mA
I_{OL}	Output Current - Low			24	mA
t_r, t_f	Input Rise and Fall Time *	V_{CC} =3.0 V	0	150	ns/V
	(except Schmitt Inputs)	V_{CC} =4.5 V	0	40	
		V_{CC} =5.5 V	0	25	

* V_{IN} from 30% to 70% V_{CC}

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limits		Unit
				25 °C	-40°C to 85°C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V	3.0 4.5 5.5	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High-Level Output Voltage	$I_{OUT} \leq$ -50 μA	3.0 4.5 5.5	2.9 4.4 5.4	2.9 4.4 5.4	V
		*V_{IN}=V_{IH} or V_{IL} I_{OH}=-12 mA I_{OH}=-24 mA I_{OH}=-24 mA	 3.0 4.5 5.5	 2.56 3.86 4.86	 2.46 3.76 4.76	
V_{OL}	Maximum Low-Level Output Voltage	$I_{OUT} \leq$ 50 μA	3.0 4.5 5.5	0.1 0.1 0.1	0.1 0.1 0.1	V
		*V_{IN}=V_{IH} or V_{IL} I_{OL}=12 mA I_{OL}=24 mA I_{OL}=24 mA	 3.0 4.5 5.5	 0.36 0.36 0.36	 0.44 0.44 0.44	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	5.5	±0.1	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	V_{IN}(OE)=V_{IH} or V_{IL} V_{IN}=V_{CC} or GND V_{OUT}=V_{CC} or GND	5.5	±0.6	±6.0	μA
I_{OLD}	+Minimum Dynamic Output Current	V_{OLD}=1.65 V Max	5.5		75	mA
I_{OHD}	+Minimum Dynamic Output Current	V_{OHD}=3.85 V Min	5.5		-75	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND	5.5	8.0	80	μA

* All outputs loaded; thresholds on input associated with output under test.
+Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limits				Unit
			25 °C		-40°C to 85°C		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay, A-to-B Clock or B-to-A Clock to A or B Data Port (Figure 1)	3.3 5.0	4.0 2.5	17.0 12.0	3.0 2.0	19.0 14.0	ns
t_{PHL}	Propagation Delay, A-to-B Clock or B-to-A Clock to A or B Data Port (Figure 1)	3.3 5.0	3.0 2.0	14.5 10.5	2.5 1.5	16.5 12.0	ns
t_{PLH}	Propagation Delay, Input A to Output B or Input B to Output A (Figures 2,3)	3.3 5.0	3.0 2.0	14.0 9.5	2.5 1.5	16.0 11.0	ns
t_{PHL}	Propagation Delay, Input A to Output B or Input B to Output A (Figures 2,3)	3.3 5.0	2.5 1.5	13.0 9.0	2.0 1.0	15.0 10.5	ns
t_{PLH}	Propagation Delay, A-to-B Source or B-to-A Source to A or B Data Port (Figure 4)	3.3 5.0	3.0 2.5	14.0 10.0	2.5 2.0	16.0 11.5	ns
t_{PHL}	Propagation Delay, A-to-B Source or B-to-A Source to A or B Data Port (Figure 4)	3.3 5.0	2.5 2.0	13.5 10.0	2.0 1.5	15.5 11.5	ns
t_{PZH}	Propagation Delay, Output Enable to A Data Port (Figure 5)	3.3 5.0	2.5 1.5	12.0 9.0	2.0 1.0	13.5 10.0	ns
t_{PZL}	Propagation Delay, Output Enable to A Data Port (Figure 5)	3.3 5.0	2.5 1.5	12.0 9.0	2.0 1.0	14.0 10.5	ns
t_{PHZ}	Propagation Delay, Output Enable to A Data Port (Figure 5)	3.3 5.0	3.0 2.0	13.0 11.0	2.5 1.5	14.0 12.0	ns
t_{PLZ}	Propagation Delay, Output Enable to A Data Port (Figure 5)	3.3 5.0	2.5 2.0	12.5 10.5	2.0 1.5	14.0 12.0	ns
t_{PZH}	Propagation Delay, Direction to B Data Port (Figure 6)	3.3 5.0	3.0 2.0	12.5 9.5	2.5 1.5	14.0 10.5	ns
t_{PZL}	Propagation Delay, Direction to B Data Port (Figure 6)	3.3 5.0	2.5 1.5	12.5 9.5	2.0 1.0	14.5 11.0	ns
t_{PHZ}	Propagation Delay, Direction to B Data Port (Figure 6)	3.3 5.0	3.5 2.5	13.5 11.5	3.0 2.0	14.5 12.5	ns
t_{PLZ}	Propagation Delay, Direction to B Data Port (Figure 6)	3.3 5.0	3.0 2.5	13.5 11.5	2.5 2.0	15.0 13.0	ns
C_{IN}	Maximum Input Capacitance	5.0	4.5		4.5		pF
C_{OUT}	Input/Output Capacitance	5.0	15		15		pF

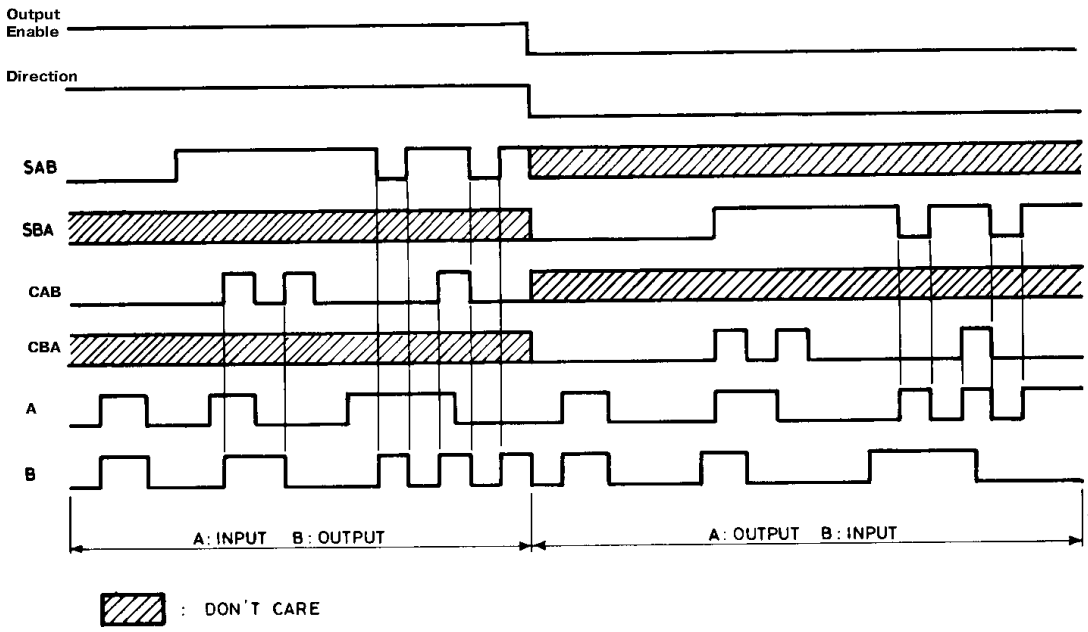
		Typical @25°C,V_{CC}=5.0 V	
C_{PD}	Power Dissipation Capacitance	60	pF

*Voltage Range 3.3 V is 3.3 V ±0.3 V
Voltage Range 5.0 V is 5.0 V ±0.5 V

TIMING REQUIREMENTS(C_L=50pF, Input t_r=t_f=3.0 ns)

Symbol	Parameter	V_{CC}* V	Guaranteed Limits		Unit
			25 °C	-40°C to 85°C	
t_{su}	Minimum Setup Time, A or B Data Port to A-to-B Clock or B-to-A Clock (Figure 7)	5.0	7.0	8.0	ns
t_h	Minimum Hold Time, A-to-B Clock or B-to-A Clock to A or B Data Port (Figure 7)	5.0	2.5	2.5	ns
t_w	Minimum Pulse Width, A-to-B Clock or B-to-A Clock (Figure 7)	5.0	6.0	7.0	ns

TIMING DIAGRAM



FUNCTION TABLE

Dir.	OE	CAB	CBA	SAB	SBA	A	B	FUNCTION
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↓	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops, are displayed at the A bus.
		X*	↓	X	H	H L	H L	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↓	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↓	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↓	↓	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respec.

X : DON'T CARE
Z : HIGH IMPEDANCE
Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO TRANSITION OF THE CLOCK INPUTS

SWITCHING DIAGRAMS

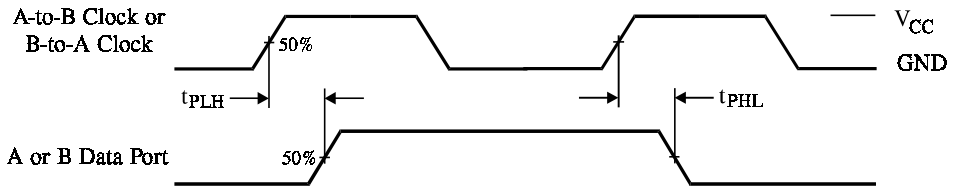


Figure 1. Switching Waveforms

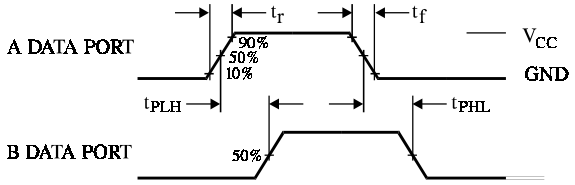


Figure 2. A Data Port = Input, B Data Port = Output

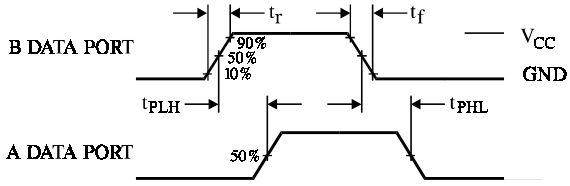


Figure 3. A Data Port = Output, B Data Port = Input

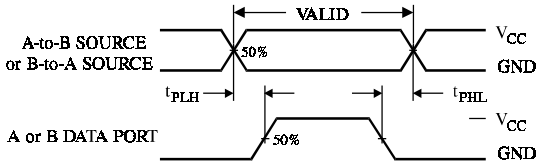


Figure 4. Switching Waveforms

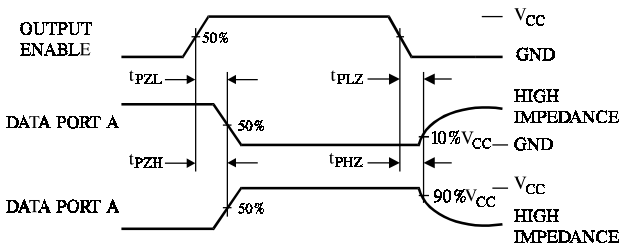


Figure 5. Switching Waveforms

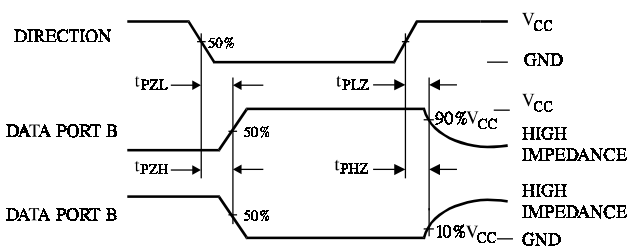


Figure 6. Switching Waveforms

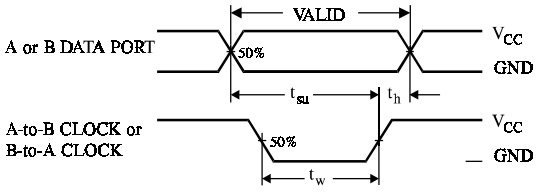


Figure 7. Switching Waveforms

EXPANDED LOGIC DIAGRAM