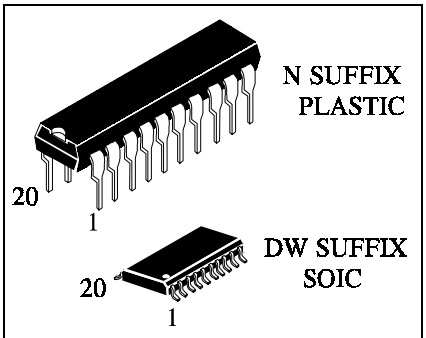
IN74ALS574

Octal 3-State Noninverting D Flip-Flop

The device is comprised of eight edge-triggered D-Type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

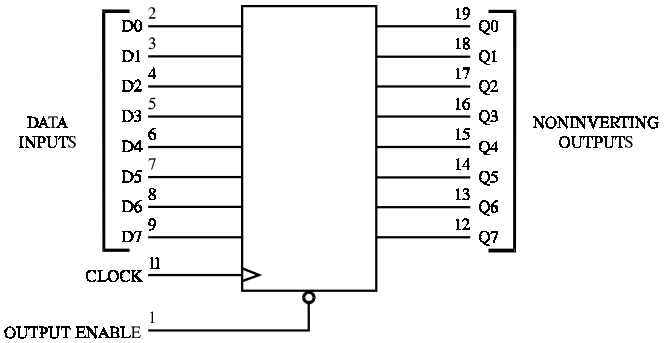
A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- TRI-STATE buffer-type outputs drive bus lines directly



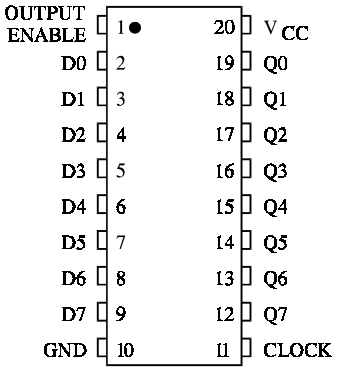
ORDERING INFORMATION
IN74ALS574N Plastic
IN74ALS574DW SOIC
T_A = -10° to 70° C
for all packages

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Output
Output Enable	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L,H, ↓	X	no change
H	X	X	Z

X = don't care
Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7.0	V
V_{IN}	Input Voltage	7.0	V
V_{OUT}	Output Voltage (Referenced to GND)	5.5	V
Tstg	Storage Temperature Range	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	High Level Input Voltage	2.0		V
V_{IL}	Low Level Input Voltage		0.8	V
I_{OH}	High Level Output Current		-2.6	mA
I_{OL}	Low Level Output Current		24	mA
T_A	Ambient Temperature Range	-10	+70	°C

DC ELECTRICAL CHARACTERISTICS over full operating conditions

Symbol	Parameter	Test Conditions		Guaranteed Limit		Unit
				Min	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = min, I_{IN} = -18 mA			-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = min, I_{OH} = -0.4 mA		2.5		V
		V_{CC} = min, I_{OH} = -2.6 mA		2.4		
V_{OL}	Low Level Output Voltage	V_{CC} = min, I_{OL} = 12 mA			0.4	V
		V_{CC} = min, I_{OL} = 24 mA			0.5	
I_{OZH}	Output Off Current HIGH	V_{CC} = max, V_{OUT} = 2.7 V			20	µA
I_{OZL}	Output Off Current LOW	V_{CC} = max, V_{OUT} = 0.4 V			-20	µA
I_{IH}	High Level Input Current	V_{CC} = max, V_{IN} = 2.7 V			20	µA
		V_{CC} = max, V_{IN} = 7.0 V			0.1	mA
I_{IL}	Low Level Input Current	V_{CC} = max, V_{IN} = 0.4 V			-0.1	mA
I_O	Output Short Circuit Current	V_{CC} = max, V_O = 2.25 V		-30	-112	mA
I_{CC}	Supply Current	V_{CC} = max	Outputs Low		17	mA
			Outputs High		24	
			3-State (High Z)		27	

AC ELECTRICAL CHARACTERISTICS over full operating conditions
(V_{CC} = 5.0 V±10%, C_L = 50 pF, R_{L1} = R_{L2} = 500 Ω, Input t_r = t_f = 2.0 ns)

Symbol	Parameter	Guaranteed Limit		Unit
		Min	Max	
f_{max}	Maximum Clock Frequency	35		MHz
t_{PLH}, t_{PHL}	Propagation Delay Time, from Clock to Output		14	ns
t_{PZH}, t_{PZL}	Propagation Delay Time, from Enable to Any Q		18	ns
t_{PHZ}	Propagation Delay Time, from Enable to Any Q		32	ns
t_{PLZ}	Propagation Delay Time, from Enable to Any Q		18	ns
t_w	Pulse Duratio, Enable, 25°C at 5.0 V	16.5		ns
t_{su}	Data Setup Time before Clock	15		ns
t_h	Data Hold Time after Clock	4		ns

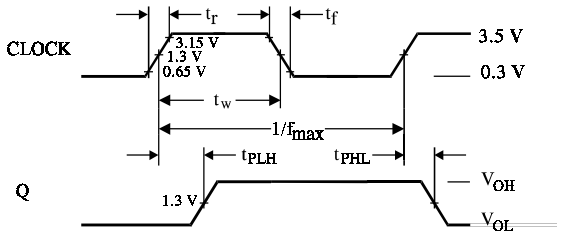
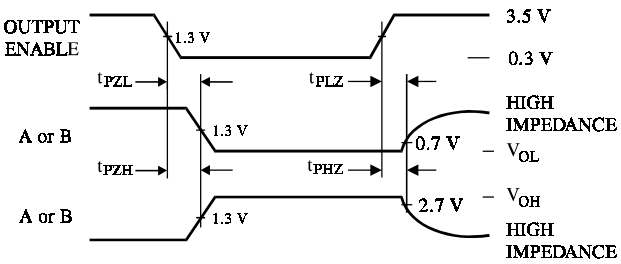


Figure 1. Switching Waveforms



t_{PZL}, t_{PLZ} - S1 closed
t_{PZH}, t_{PHZ} - S1 opened

Figure 2. Switching Waveforms

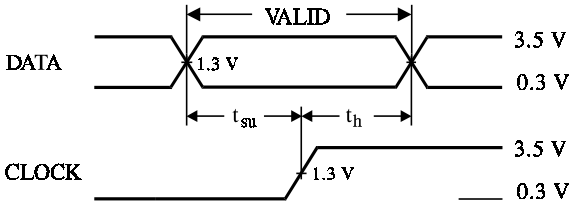
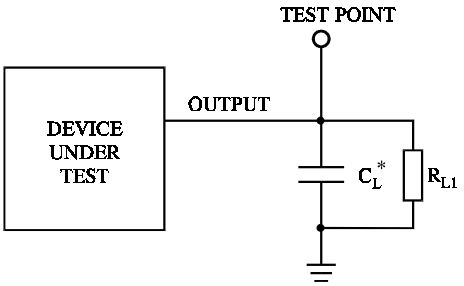
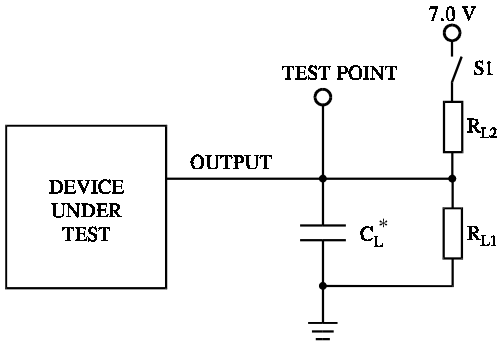


Figure 3. Switching Waveforms



* Includes all probe and jig capacitance.

Figure 3. Test Circuit



* Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM