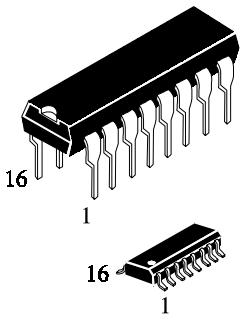
IN74HC123

Dual Retriggerable Monostable Multivibrator



ORDERING INFORMATION
IN74HC123N Plastic
IN74HC123D SOIC
T_A = -55° to 125° C for all packages

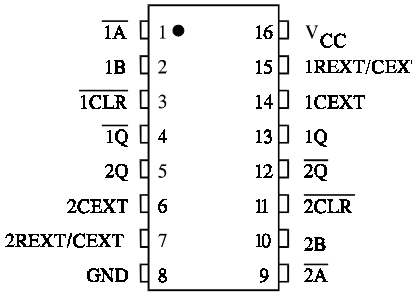
The IN74HC123 is identical in pinout to the LS/ALS123. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

There are two trigger inputs, $\overline{A}$ INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for rising/falling signals.

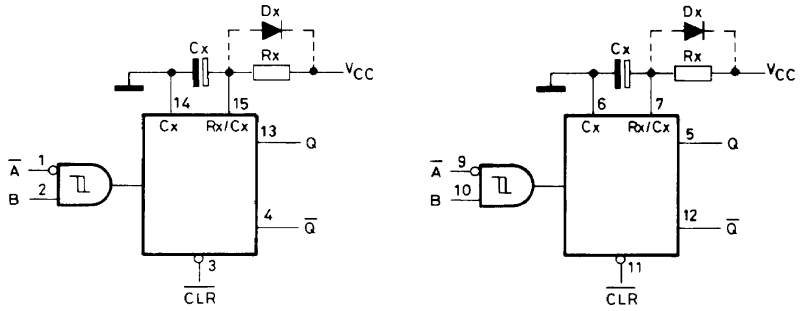
The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor R_X and capacitor C_X. Taking CLR low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

Note
(1) C_X, R_X, D_X are external components.
(2) D_X is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off C_X is discharged mainly through an internal parasitic diode. If C_X is sufficiently large and V_{CC} decreases rapidly, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA.

FUNCTION TABLE

Inputs			Outputs		Note
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
⊓	H	H	⊓	⊔	Output Enable
X	L	H	L *	H *	Inhibit
H	X	H	L *	H *	Inhibit
L	⊓	H	⊓	⊔	Output Enable
L	H	⊓	⊓	⊔	Output Enable
X	X	L	L	H	Inhibit

X = don't care
* - except for monostable period

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin A, B, $\overline{CLR}$ C_X, R_X	±20 ±30	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		3.0 **	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time - $\overline{CLR}$ (Figure 2)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns
	A or B		-	No Limit	
R_X	External Timing Resistor	V_{CC} <4.5 V V_{CC} ≥ 4.5 V	10 2.0	1000 1000	kΩ
C_X	External Timing Capacitor		0	No Limit	μF

** The In74HC123 will function at 2.0 V but for optimum pulse width stability, V_{CC} should be above 3.0 V.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20$ μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20$ μA	2.0 4.5 6.0	0.5 1.35 1.8	0.5 1.35 1.8	0.5 1.35 1.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current (A, B, CLR)	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{IN}	Maximum Input Leakage Current (R_X, C_X)	V_{IN}=V_{CC} or GND	6.0	±50	±500	±500	nA
I_{CC}	Maximum Quiescent Supply Current (per Package) Standby State	V_{IN}=V_{CC} or GND Q1 and Q2 = Low I_{OUT}=0μA	6.0	130	220	350	μA
				25°C	-45°C to 85°C	-55°C to 125°C	
I_{CC}	Maximum Supply Current (per Package) Active State	V_{IN}=V_{CC} or GND Q1 and Q2 = High I_{OUT}=0μA Pins 15 and 7 = 0.5 V_{CC}	6.0	400	600	800	μA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85 °C	≤125 °C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input $\overline{A}$ or B to Q or $\overline{Q}$ (Figures 1 and 3)	2.0 4.5 6.0	255 50 45	320 65 55	385 75 65	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , $\overline{CLR}$ to Q or $\overline{Q}$ (Figures 2 and 3)	2.0 4.5 6.0	215 45 35	270 55 45	325 65 55	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output(Figures 2 and 3)	2.0 4.5 6.0	75 16 14	95 20 17	110 22 20	ns
C_{IN}	Maximum Input Capacitance $\overline{A}$, B, $\overline{CLR}$ C_X, R_X	-	10 25	10 25	10 25	pF

C_{PD}	Power Dissipation Capacitance (Per Multivibrator) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 150	pF

TIMING REQUIREMENTS(C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Inactive to $\overline{A}$ or B (Figure 2)	2.0 4.5 6.0	0 0 0	0 0 0	0 0 0	ns
t_w	Minimum Pulse Width, Input $\overline{A}$ or B (Figure 1)	2.0 4.5 6.0	100 20 17	125 25 20	150 30 25	ns
t_w	Minimum Pulse Width, $\overline{CLR}$ (Figure 2)	2.0 4.5 6.0	100 20 17	125 25 20	150 30 25	ns
t_r, t_r	Maximum Input Rise and Fall Times, $\overline{CLR}$ (Figure 2)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns
	A or B (Figure 2)	2.0 4.5 6.0	No Limit			

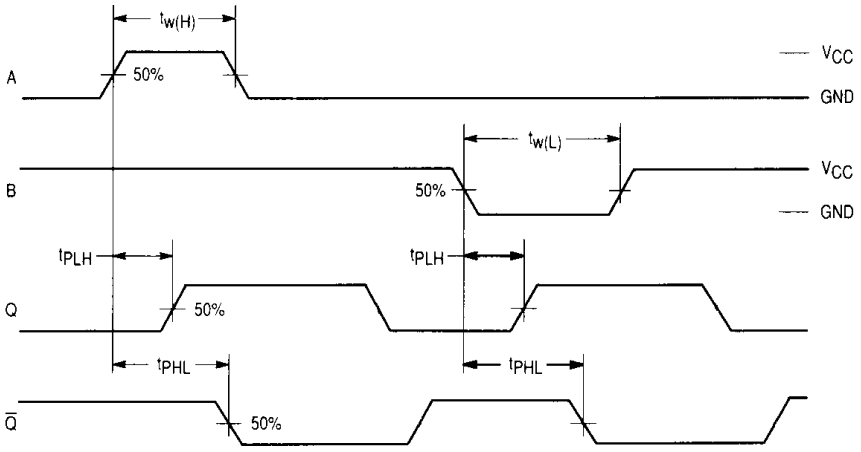


Figure 1. Switching Waveforms

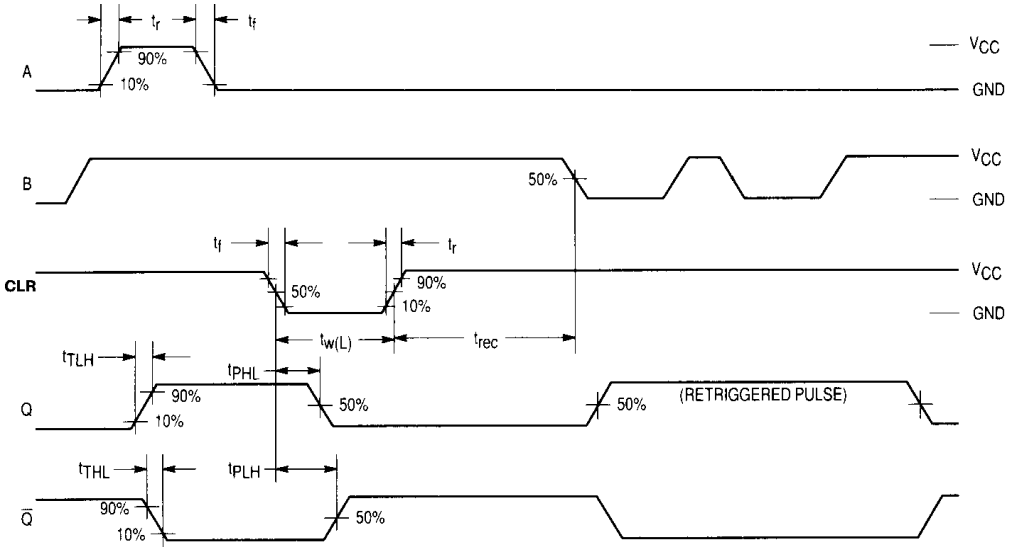
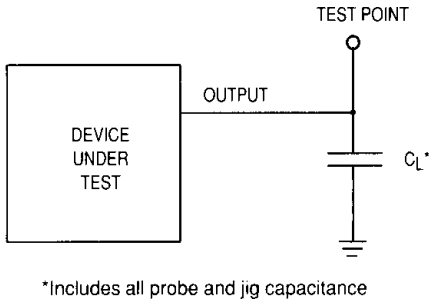


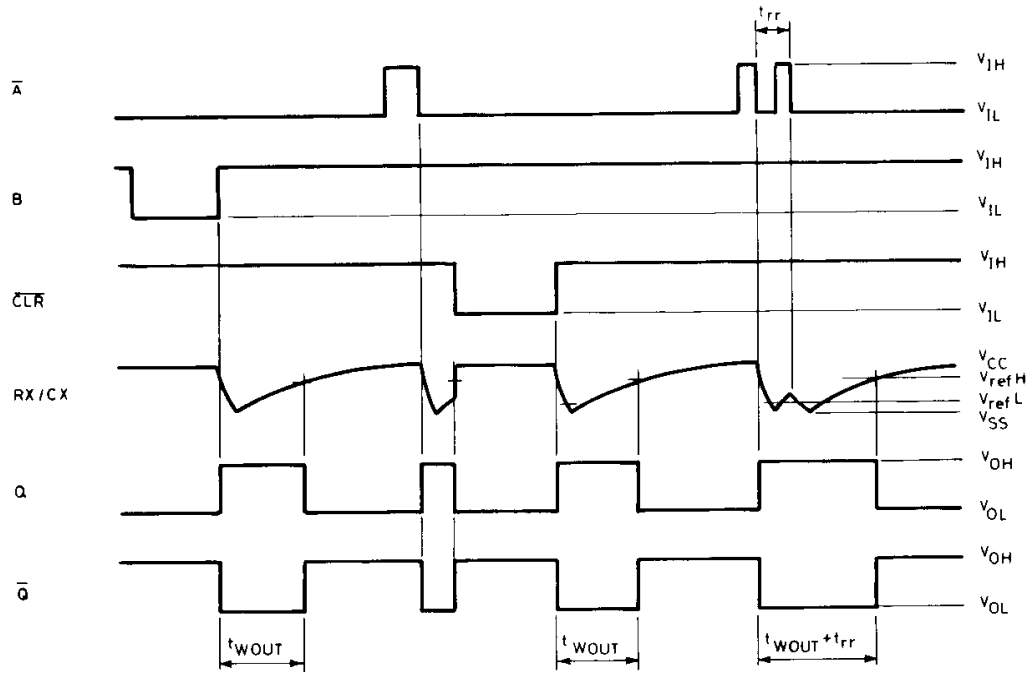
Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM