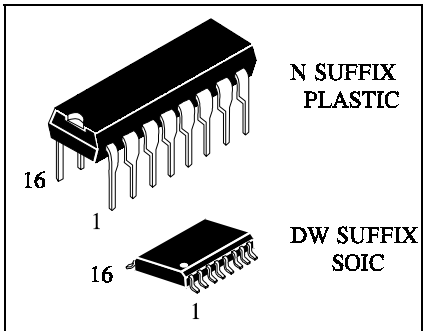
IN74HC4051

Analog Multiplexer Demultiplexer
High-Performance Silicon-Gate CMOS



ORDERING INFORMATION
IN74HC4051N Plastic
IN74HC4051DW SOIC
T_A = -55° to 125° C for all packages

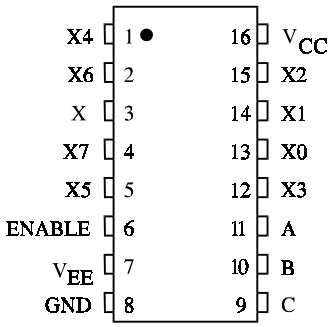
The IN74HC4051 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input.When the Enable pin is high, all analog switches are turned off.

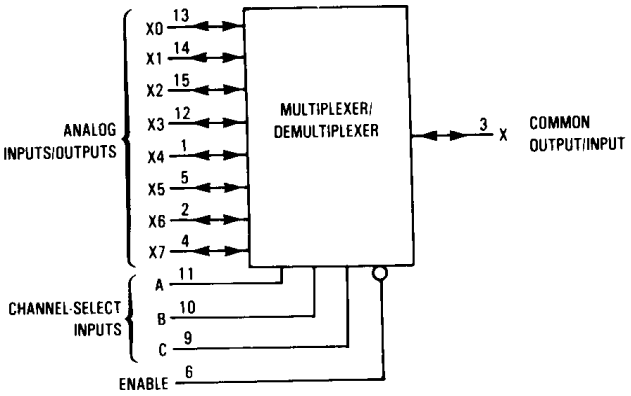
The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range (V_{CC}-V_{EE})=2.0 to 12.0 V
- Digital (Control) Power Supply Range (V_{CC}-GND)=2.0 to 6.0 V
- Low Noise

PIN ASSIGNMENT



LOGIC DIAGRAM
Single-Pole, 8-Position Plus Common Off



PIN 16 =V_{CC}
PIN 7 = V_{EE}
PIN 8 = GND

FUNCTION TABLE

Control Inputs				ON Channels
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	None

X = don’t care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V_{EE})	-0.5 to +7.0 -0.5 to +14.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)	-7.0 to +0.5	V
V_{IS}	Analog Input Voltage	V_{EE} - 0.5 to V_{CC}+0.5	V
V_{IN}	Digital Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
I	DC Input Current Into or Out of Any Pin	±25	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive Supply Voltage (Referenced to GND) (Referenced to V_{EE})		2.0 2.0	6.0 12.0	V
V_{EE}	Negative DC Supply Voltage (Referenced to GND)		- 6.0	GND	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{IN}	Digital Input Voltage (Referenced to GND)		GND	V_{CC}	V
V_{IO}*	Static or Dynamic Voltage Across Switch		-	1.2	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Channel Select or Enable Inputs)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

* For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i. e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range indicated in the Recommended Operating Conditions..

Unused digital input pins must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused Analog I/O pins may be left open or terminated.

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND)
V_{EE}=GND, Except Where Noted

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	R_{ON} = Per Spec	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage, Channel-Select or Enable Inputs	R_{ON} = Per Spec	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
I_{IN}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	V_{IN}=V_{CC} or GND, V_{EE}=-6.0 V	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select = V_{CC} or GND Enable = V_{CC} or GND V_{IS} = V_{CC} or GND V_{IO}= 0 V V_{EE} = GND V_{EE} = - 6.0	 6.0 6.0	 2 8	 20 80	 40 160	μA

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					25 °C to -55°C	≤85 °C	≤125 °C	
R_{ON}	Maximum "ON" Resistance	V_{IN}=V_{IL} or V_{IH} V_{IS} = V_{CC} or V_{EE} I_S ≤ 2.0 mA(Figure 1)	4.5 4.5 6.0	0.0 -4.5 -6.0	190 120 100	240 150 125	280 170 140	Ω
		V_{IN}=V_{IL} or V_{IH} V_{IS} = V_{CC} or V_{EE} (Endpoints) I_S ≤ 2.0 mA(Figure 1)	4.5 4.5 6.0	0.0 -4.5 -6.0	150 100 80	190 125 100	230 140 115	
ΔR_{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V_{IN}=V_{IL} or V_{IH} V_{IS} = 1/2 (V_{CC}- V_{EE}) I_S ≤ 2.0 mA	4.5 4.5 6.0	0.0 -4.5 -6.0	30 12 10	35 15 12	40 18 14	Ω
I_{OFF}	Maximum Off- Channel Leakage Current, Any One Channel	V_{IN}=V_{IL} or V_{IH} V_{IO}= V_{CC}- V_{EE} Switch Off (Figure 2)	6.0	-6.0	0.1	0.5	1.0	μA
	Maximum Off- Channel Leakage Current, Common Channel	V_{IN}=V_{IL} or V_{IH} V_{IO} = V_{CC}- V_{EE} Switch Off (Figure 3)	6.0	-6.0	0.2	2.0	4.0	
I_{ON}	Maximum On- Channel Leakage Current, Channel to Channel	V_{IN}=V_{IL} or V_{IH} Switch to Switch = V_{CC}- V_{EE} (Figure 4)	6.0	-6.0	0.2	2.0	4.0	μA

AC ELECTRICAL CHARACTERISTICS(C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter		V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel-Select to Analog Output (Figures 8 and 9)		2.0 4.5 6.0	370 74 63	465 93 79	550 110 94	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay , Analog Input to Analog Output (Figures 10 and 11)		2.0 4.5 6.0	60 12 10	75 15 13	90 18 15	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay , Enable to Analog Output (Figures 12 and 13)		2.0 4.5 6.0	290 58 49	364 73 62	430 86 73	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay , Enable to Analog Output (Figures 12 and 13)		2.0 4.5 6.0	345 69 59	435 87 74	515 103 87	ns
C_{IN}	Maximum Input Capacitance, Channel-Select or Enable Inputs		-	10	10	10	pF
$C_{I/O}$	Maximum Capacitance Analog I/O	All Switches Off	-	35	35	35	pF
	Common O/I		-	130	130	130	
	Feedthrough		-	1.0	1.0	1.0	

C_{PD}	Power Dissipation Capacitance (Per Package) (Figure 14) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V, V_{EE}=0 V 45	pF

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0.0 V)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Limit* 25 °C	Unit
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 5)	f_{in}=1 MHz Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{OS} Increase f_{in} Frequence Until dB Meter Reads -3 dB R_L =50 Ω, C_L=10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	80 80 80	MHz
-	Off-Channel Feedthrough Isolation (Figure 6)	f_{in}= Sine Wave Adjust f_{in} Voltage to Obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L =600 Ω, C_L=50 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-50 -50 -50	dB
		f_{in} = 1.0 MHz, R_L =50 Ω, C_L=10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	-40 -40 -40	
-	Feedthrough Noise, Channel Select Input to Common O/I (Figure 7)	V_{IN}≤ 1 Mhz Square Wave ($t_r = t_f$ = 6 ns) Adjust R_L at Setup so that I_S= 0 A Enable = GND R_L =600 Ω, C_L=50 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	25 105 135	mV_{PP}
		R_L =10 Ω, C_L=10 pF	2.25 4.50 6.00	-2.25 -4.50 -6.00	35 145 190	
THD	Total Harmonic Distortion (Figure 15)	f_{in}= 1 kHz, R_L =10 kΩ, C_L=50 pF THD = $THD_{Measured}$ - THD_{Source} V_{IS} =4.0 V_{PP} sine wave V_{IS} =8.0 V_{PP} sine wave V_{IS} =11.0 V_{PP} sine wave	2.25 4.50 6.00	-2.25 -4.50 -6.00	0.10 0.08 0.05	%

* Limits not tested. Determined by design and verified by qualification.

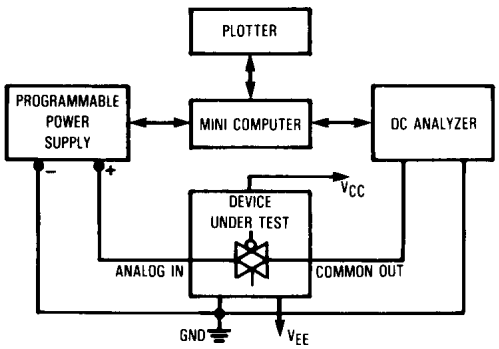


Figure 1. On Resistance Test Set-Up

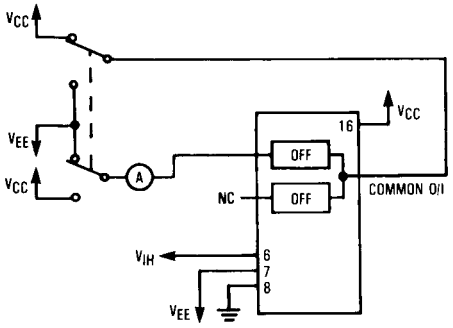


Figure 2. Maximum Off Channel Leakage Current, Any One Channel, Test Set-U$_P$

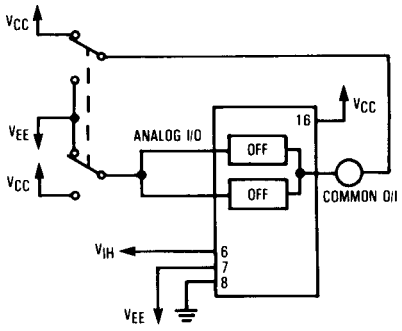


Figure 3. Maximum Off Channel Leakage Current, Common Channel, Test Set-U$_P$

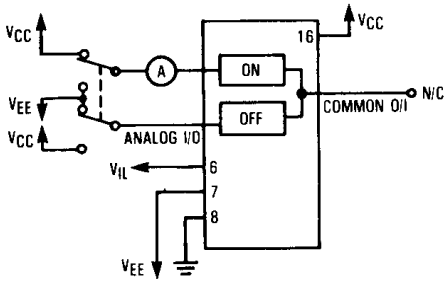
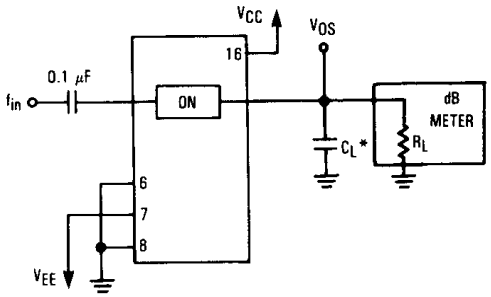
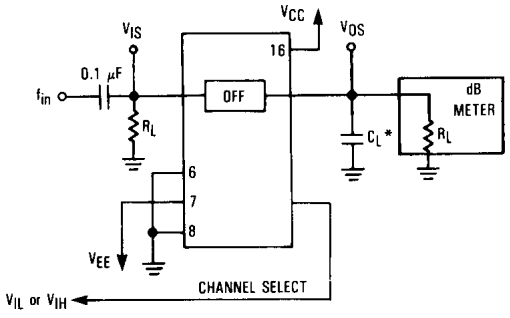


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-U$_P$



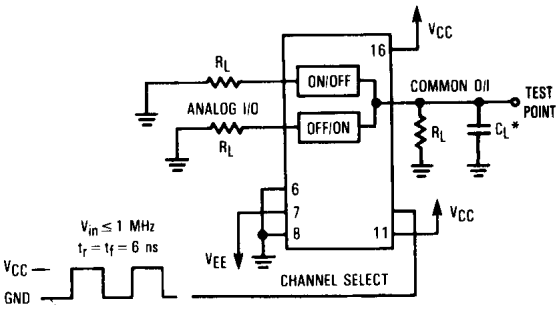
* Includes all probe and jig capacitance.

Figure 5. Maximum On Channel Bandwidth, Test Set-U$_P$



* Includes all probe and jig capacitance.

Figure 6. Off Channel Feedthrough Isolation, Test Set-U$_P$



* Includes all probe and jig capacitance.

Figure 7.Feedthrough Noise, Channel Select to Common Out, Test Set-U$_P$

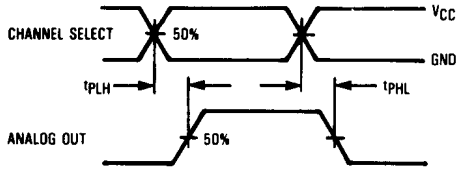
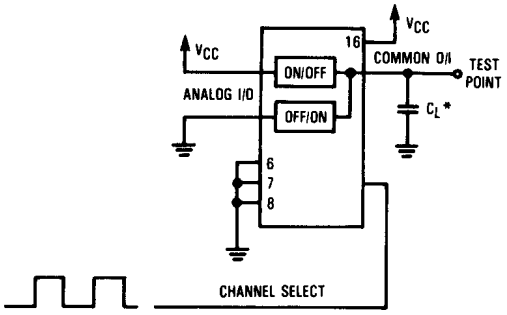


Figure 8. Switching Weveforms



* Includes all probe and jig capacitance.

Figure 9. Test Set-U_P, Channel Select to Analog Out

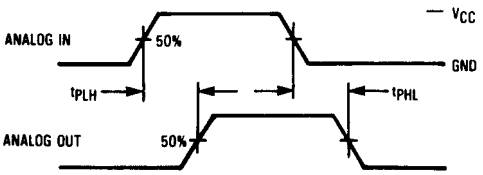
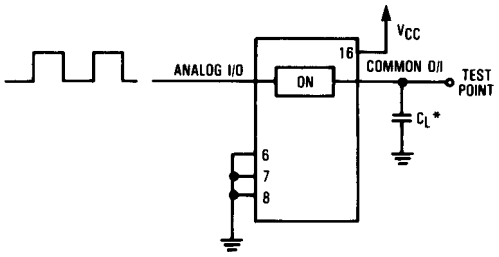


Figure 10. Switching Weveforms



* Includes all probe and jig capacitance.

Figure 11. Test Set-U_P, Analog In to Analog Out

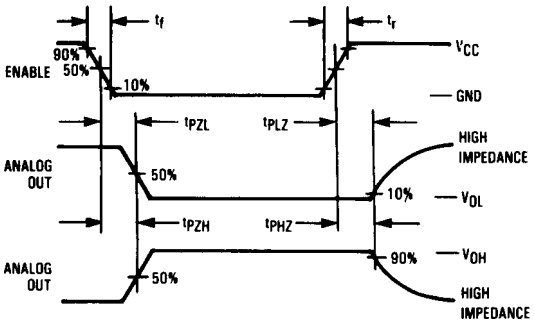


Figure 12. Switching Weveforms

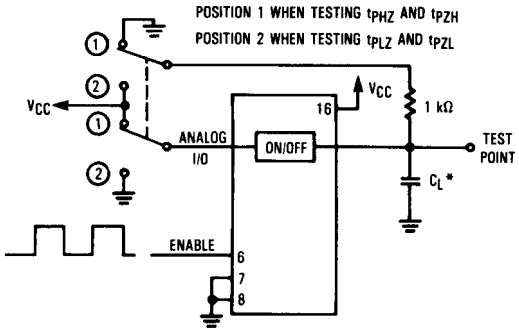


Figure 13. Test Set-U_P, Enable to Analog Out

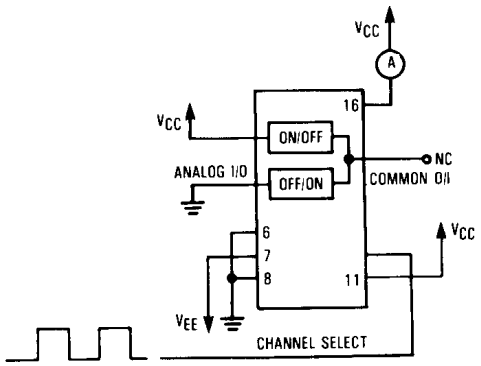
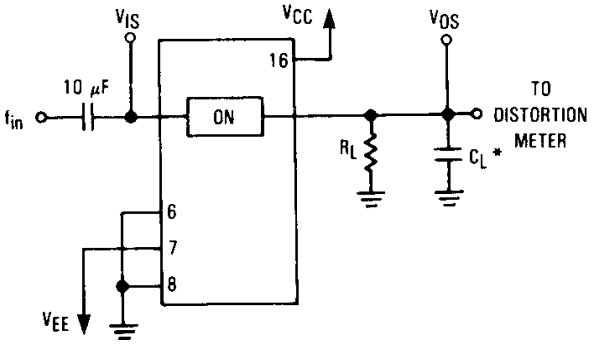


Figure 14. Power Dissipation Capacitance, Test Set-Up



* Includes all probe and jig capacitance

Figure 15. Total Harmonic Distortion, Test Set-U_P

EXPANDED LOGIC DIAGRAM