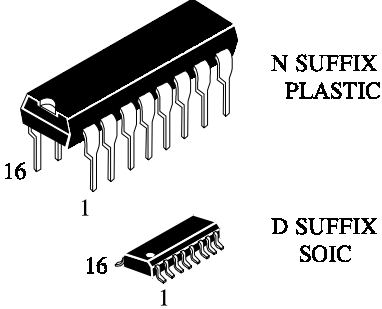


**IW4043B**

**Quad 3-State R/S Latches**  
**High-Voltage Silicon-Gate CMOS**

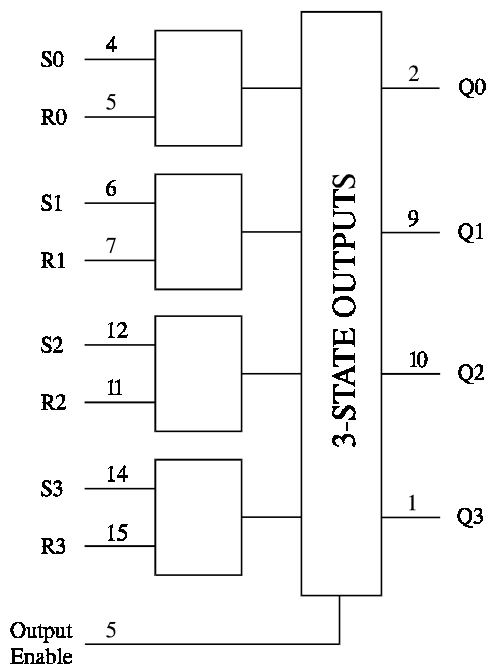
The IW4043B types are quad cross-coupled 3-state CMOS NOR latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
  - 2.5 V min @ 15.0 V supply



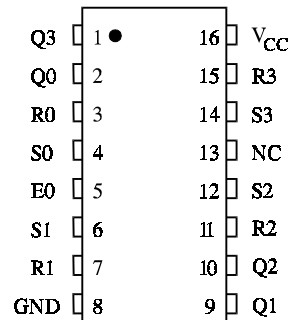
**ORDERING INFORMATION**  
 IW4043BN Plastic  
 IW4043BD SOIC  
 $T_A = -55^\circ$  to  $125^\circ$  C for all packages

**LOGIC DIAGRAM**



PIN 13 = NO CONNECTION  
 PIN 16 = V<sub>CC</sub>  
 PIN 8 = GND

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs			Outputs
S	R	OE	Q
X	X	L	High Impedance
L	L	H	No change
L	H	H	L
H	L	H	H
H	H	H	H

X = don't care

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P <sub>D</sub>	Power Dissipation per Output Transistor	100	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur.  
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: : - 7 mW/°C from 65° to 125°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	3.0	18	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>).  
Unused outputs must be left open.

**DC ELECTRICAL CHARACTERISTICS**(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.5 V or V <sub>CC</sub> - 0.5V	5.0	3.5	3.5	3.5	V
		V <sub>OUT</sub> = 1.0 V or V <sub>CC</sub> - 1.0 V	10	7	7	7	
		V <sub>OUT</sub> = 1.5 V or V <sub>CC</sub> - 1.5V	15	11	11	11	
V <sub>IL</sub>	Maximum Low -Level Input Voltage	V <sub>OUT</sub> = 0.5 V or V <sub>CC</sub> - 0.5V	5.0	1.5	1.5	1.5	V
		V <sub>OUT</sub> = 1.0 V or V <sub>CC</sub> - 1.0 V	10	3	3	3	
		V <sub>OUT</sub> = 1.5 V or V <sub>CC</sub> - 1.5V	15	4	4	4	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> =GND or V <sub>CC</sub>	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = GND or V <sub>CC</sub>	18	±0.1	±0.1	±1.0	μA
I <sub>OZ</sub>	Maximum Three State Leakage Current	Output in High-Impedance State V <sub>IN</sub> = GND or V <sub>CC</sub> V <sub>OUT</sub> = GND or V <sub>CC</sub>	18	±0.4	±0.4	±12.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = GND or V <sub>CC</sub>	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I <sub>OL</sub>	Minimum Output Low (Sink) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> U <sub>OL</sub> =0.4 V U <sub>OL</sub> =0.5 V U <sub>OL</sub> =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I <sub>OH</sub>	Minimum Output High (Source) Current	V <sub>IN</sub> = GND or V <sub>CC</sub> U <sub>OH</sub> =2.5 V U <sub>OH</sub> =4.6 V U <sub>OH</sub> =9.5 V U <sub>OH</sub> =13.5 V	5.0	-2	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

**AC ELECTRICAL CHARACTERISTICS**( $C_L=50\text{pF}$ ,  $R_L=200\text{k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, SET or RESET to Q (Figure 1)	5.0 10 15	300 140 100	300 140 100	600 280 200	ns
$t_{PHZ}$ , $t_{PZH}$	Maximum Propagation Delay, Output Enable to Q (Figures 2,4)	5.0 10 15	230 110 80	230 110 80	460 220 160	ns
$t_{PLZ}$ , $t_{PZL}$	Maximum Propagation Delay, Output Enable to Q (Figures 2,4)	5.0 10 15	180 100 70	180 100 70	360 200 140	ns
$t_{THL}$ , $t_{TLH}$	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
$C_{IN}$	Maximum Input Capacitance	-		7.5		pF

**TIMING REQUIREMENTS**( $C_L=50\text{pF}$ ,  $R_L=200\text{ k}\Omega$ , Input  $t_r=t_f=20\text{ ns}$ )

Symbol	Parameter	$V_{CC}$ V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	$25^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$t_w$	Minimum Pulse Width, SET or RESET (Figure 3)	5.0 10 15	160 80 40	160 80 40	320 160 80	ns

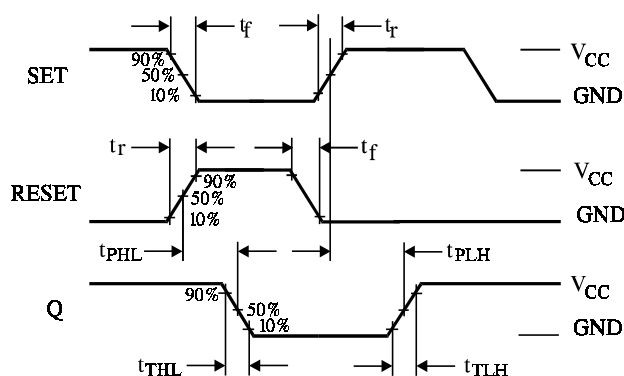


Figure 1. Switching Waveforms

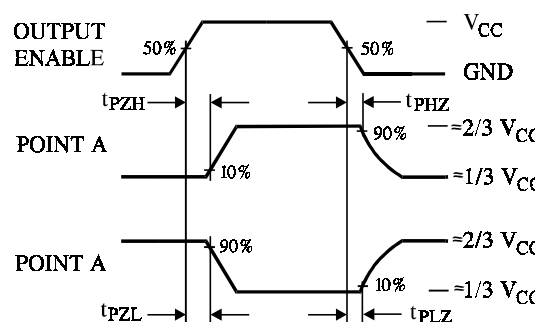


Figure 2. Switching Waveforms

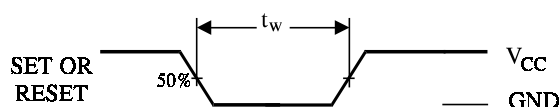
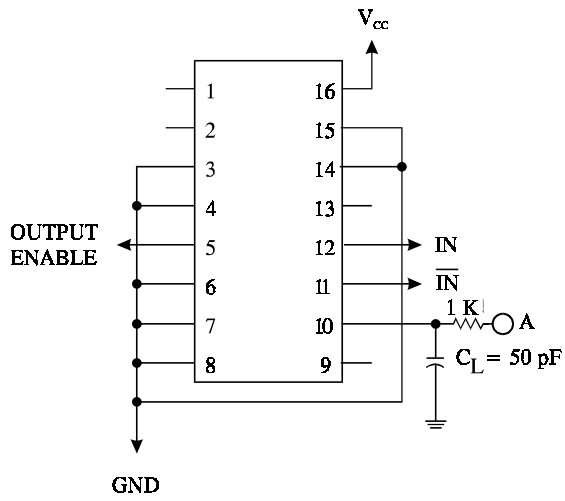


Figure 3. Switching Waveforms



TEST	IN	$\overline{\text{IN}}$	A
$t_{\text{PHZ}}$	$V_{\text{CC}}$	GND	GND
$t_{\text{PLZ}}$	GND	$V_{\text{CC}}$	$V_{\text{CC}}$
$t_{\text{PZH}}$	$V_{\text{CC}}$	GND	GND
$t_{\text{PZL}}$	GND	$V_{\text{CC}}$	$V_{\text{CC}}$

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM  
( 1/4 of the Device)

