

Quality System for producing discrete semiconductor devices and integrated circuits conforms to the requirements of STB ISO 9002-96

78L06AC

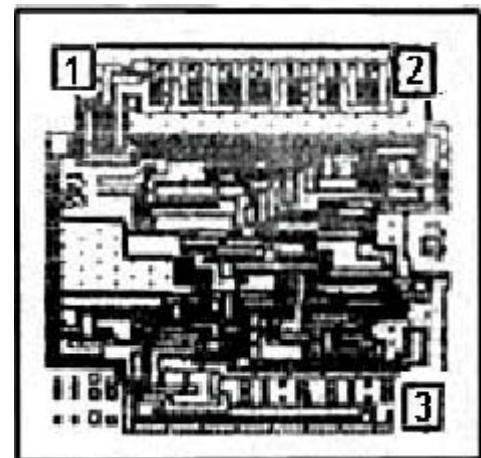
**CHIP FOR THREE-TERMINAL
POSITIVE VOLTAGE REGULATOR IC**

Features:

- ◆ Output current in excess of 100 mA
- ◆ No external components required
- ◆ Internal short circuit current limiting
- ◆ Internal thermal overload protection
- ◆ Available in either $\pm 5\%$ selections

Physical Characteristics:

Wafer Diameter 100 ± 0.5 mm
 Wafer thickness 420 ± 20 μm ;
 Die size $1.3 \times 1.2 \text{ mm}^2$;
 Scribe width $80 \mu\text{m}$
 Passivation PSG



Pad #	Pad name	Description	Bond Pad (μm)
1	OUT	Output	101 x 101
2	IN	Input	101 x 101
3	GND	Ground	101 x 101

- ◆ Maximum Ratings ($T_a = 25^\circ\text{C}$)
- ◆ Input Voltage – 30V
- ◆ Operating Junction Temperature ($T_j = 125^\circ\text{C}$)

Substrate is Common and should be connected to Pad 2

ELECTRICAL CHARACTERISTICS CHIPS ON WAFER ($T_a=25^\circ\text{C}$)

($V_{in} = 11$ V, $I_o = 40$ mA, $C_i = 0.33 \mu\text{F}$, $C_o = 0.1 \mu\text{F}$, $T_j = + 25^\circ\text{C}$, unless otherwise noted.)

Characteristic	Symbol	Test Condition	Min	Max	Unit
Output Voltage	V_o	$8V \leq V_{in} \leq 21V$, $1mA \leq I_o \leq 40mA$ $1mA \leq I_o \leq 70mA$	5.77 5.77	6.23 6.23	V
Line Regulation	ΔV_v	$8 V \leq V_{in} \leq 21 V$ $9 V \leq V_{in} \leq 21 V$		144 99	mV
Load Regulation	ΔV_i	$1mA \leq I_o \leq 100mA$ $1mA \leq I_o \leq 40mA$		63 32	mV
Quiescent Current	I_b			5.8	mA
Quiescent Current Change	ΔI_b	$9 V \leq V_{in} \leq 21 V$ $1mA \leq I_o \leq 40mA$		1.4 0.09	mA

* The parameters are guaranteed after scribing and chip encasement.