Data Sheet February 1999 File Number 1342.5

850MHz, Low Distortion, Output Limiting, Programmable Gain, Buffer Amplifier

The HFA1113 is a high speed Buffer featuring user programmable gain and output limiting coupled with ultra high speed performance. This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. The output limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation following an overdrive condition.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components, as described in the “Application Information” section. Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

Component and composite video systems will also benefit from this buffer’s performance, as indicated by the excellent gain flatness, and 0.02%/0.04 Degree Differential Gain/Phase specifications (R_L = 150Ω).

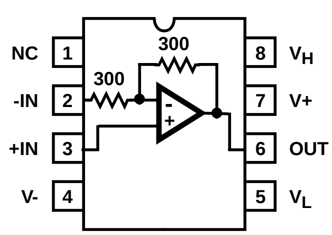
For Military product, refer to the HFA1113/883 data sheet.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA1113IB (H1113I)	-40 to 85	8 Ld SOIC	M8.15
HFA11XXEVAL	DIP Evaluation Board For High Speed Op Amps		

Pinout

HFA1113
(SOIC)
TOP VIEW



Features

- User Programmable Output Voltage Limiting
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Wide -3dB Bandwidth. 850MHz
- Excellent Gain Flatness (to 100MHz). . . . . ±0.07dB
- Low Differential Gain and Phase . . . 0.02%/0.04 Degrees
- Low Distortion (HD3, 30MHz). . . . . -73dBc
- Very Fast Slew Rate 2400V/µs
- Fast Settling Time (0.1%) 13ns
- High Output Current 60mA
- Excellent Gain Accuracy 0.99V/V
- Overdrive Recovery . . . . <1ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems

Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
V_L	5	Lower Output Limit
OUT	6	Output
V+	7	Positive Supply
V_H	8	Upper Output Limit

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage . . . . V_{SUPPLY}
Voltage at V_H or V_L Terminal . . . . (V+) + 2V to (V-) - 2V
Output Current (50% Duty Cycle) 60mA

Operating Conditions

Temperature Range . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
SOIC Package 158
Maximum Junction Temperature (Plastic Package) . . . . .150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Output Offset Voltage		25	-	8	25	mV
		Full	-	-	35	mV
Output Offset Voltage Drift		Full	-	10	-	µV/°C
PSRR		25	39	45	-	dB
		Full	35	-	-	dB
Input Noise Voltage (Note 3)	100kHz	25	-	9	-	nV/√Hz
+Input Noise Current (Note 3)	100kHz	25	-	37	-	pA/√Hz
Non-Inverting Input Bias Current		25	-	25	40	µA
		Full	-	-	65	µA
Non-Inverting Input Resistance		25	25	50	-	kΩ
Inverting Input Resistance (Note 2)		25	240	300	360	Ω
Input Capacitance		25	-	2	-	pF
Input Common Mode Range		Full	±2.5	±2.8	-	V
TRANSFER CHARACTERISTICS						
Gain	A_V = +1, V_{IN} = +2V	25	0.980	0.990	1.020	V/V
		Full	0.975	-	1.025	V/V
	A_V = +2, V_{IN} = +1V	25	1.96	1.98	2.04	V/V
		Full	1.95	-	2.05	V/V
DC Non-Linearity (Note 3)	A_V = +2, ±2V Full Scale	25	-	0.02	-	%
OUTPUT CHARACTERISTICS						
Output Voltage (Note 3)	A_V = -1	25	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current (Note 3)	R_L = 50Ω	25, 85	50	60	-	mA
		-40	35	50	-	mA
Closed Loop Output Impedance	DC, A_V = +2	25	-	0.3	-	Ω
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current (Note 3)		25	-	21	26	mA
		Full	-	-	33	mA

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Notes 2, 3)	A_V = -1	25	450	800	-	MHz
	A_V = +1	25	500	850	-	MHz
	A_V = +2	25	350	550	-	MHz
Slew Rate (V_{OUT} = 5V_{P-P}, Note 2)	A_V = -1	25	1500	2400	-	V/µs
	A_V = +1	25	800	1500	-	V/µs
	A_V = +2	25	1100	1900	-	V/µs
Full Power Bandwidth (V_{OUT} = 5V_{P-P}, Note 3)	A_V = -1	25	-	300	-	MHz
	A_V = +1	25	-	150	-	MHz
	A_V = +2	25	-	220	-	MHz
Gain Flatness (to 30MHz, Notes 2, 3)	A_V = -1	25	-	±0.02	-	dB
	A_V = +1	25	-	±0.1	-	dB
	A_V = +2	25	-	±0.015	±0.04	dB
Gain Flatness (to 50MHz, Notes 2, 3)	A_V = -1	25	-	±0.05	-	dB
	A_V = +1	25	-	±0.2	-	dB
	A_V = +2	25	-	±0.036	±0.08	dB
Gain Flatness (to 100MHz, Notes 2, 3)	A_V = -1	25	-	±0.10	-	dB
	A_V = +2	25	-	±0.07	±0.22	dB
Linear Phase Deviation (to 100MHz, Note 3)	A_V = -1	25	-	±0.13	-	Degrees
	A_V = +1	25	-	±0.83	-	Degrees
	A_V = +2	25	-	±0.05	-	Degrees
2nd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-52	-	dBc
	A_V = +1	25	-	-57	-	dBc
	A_V = +2	25	-	-52	-45	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-71	-	dBc
	A_V = +1	25	-	-73	-	dBc
	A_V = +2	25	-	-72	-65	dBc
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-47	-	dBc
	A_V = +1	25	-	-53	-	dBc
	A_V = +2	25	-	-47	-40	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-63	-	dBc
	A_V = +1	25	-	-68	-	dBc
	A_V = +2	25	-	-65	-55	dBc
2nd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 2, 3)	A_V = -1	25	-	-41	-	dBc
	A_V = +1	25	-	-50	-	dBc
	A_V = +2	25	-	-42	-35	dBc
3rd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P} , Notes 2, 3)	A_V = -1	25	-	-55	-	dBc
	A_V = +1	25	-	-49	-	dBc
	A_V = +2	25	-	-62	-45	dBc

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
3rd Order Intercept (A_V = +2, Note 3)	100MHz	25	-	28	-	dBm
	300MHz	25	-	13	-	dBm
1dB Compression (A_V = +2, Note 3)	100MHz	25	-	19	-	dBm
	300MHz	25	-	12	-	dBm
Reverse Isolation (S_{12}, Note 3)	40MHz	25	-	-70	-	dB
	100MHz	25	-	-60	-	dB
	600MHz	25	-	-32	-	dB
TRANSIENT CHARACTERISTICS						
Rise Time (V_{OUT} = 0.5V Step, Note 2)	A_V = -1	25	-	500	800	ps
	A_V = +1	25	-	480	750	ps
	A_V = +2	25	-	700	1000	ps
Rise Time (V_{OUT} = 2V Step)	A_V = -1	25	-	0.82	-	ns
	A_V = +1	25	-	1.06	-	ns
	A_V = +2	25	-	1.00	-	ns
Overshoot (V_{OUT} = 0.5V Step, Input t_R/t_F = 200ps, Notes 2, 3, 4)	A_V = -1	25	-	12	30	%
	A_V = +1	25	-	45	65	%
	A_V = +2	25	-	6	20	%
0.1% Settling Time (Note 3)	V_{OUT} = 2V to 0V	25	-	13	20	ns
0.05% Settling Time	V_{OUT} = 2V to 0V	25	-	20	33	ns
Differential Gain	A_V = +1, 3.58MHz, R_L = 150Ω	25	-	0.03	-	%
	A_V = +2, 3.58MHz, R_L = 150Ω	25	-	0.02	-	%
Differential Phase	A_V = +1, 3.58MHz, R_L = 150Ω	25	-	0.05	-	Degrees
	A_V = +2, 3.58MHz, R_L = 150Ω	25	-	0.04	-	Degrees
OUTPUT LIMITING CHARACTERISTICS A_V = +2, V_H = +1V, V_L = -1V, Unless Otherwise Specified						
Clamp Accuracy (Note 3)	V_{IN} = ±1.6V, A_V = -1	25	-	±100	±150	mV
		Full	-	-	±200	mV
Clamp Overshoot	V_{IN} = ±1V, Input t_R/t_F = 500ps	25	-	7	-	%
Overdrive Recovery Time (Note 3)	V_{IN} = ±1V	25	-	0.75	1.5	ns
Negative Clamp Range		25	-	-5.0 to +2.0	-	V
Positive Clamp Range		25	-	-2.0 to +5.0	-	V
Clamp Input Bias Current (Note 3)		25	-	50	200	µA
		Full	-	-	300	µA
Clamp Input Bandwidth (Note 3)	V_H or V_L = 100mV_{P-P}	25	-	500	-	MHz

NOTES:

2. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
3. See Typical Performance Curves for more information.
4. Overshoot decreases as input transition times increase, especially for A_V = +1. Please refer to Typical Performance Curves.

Application Information

Closed Loop Gain Selection

The HFA1113 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±Inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 50Ω, C_L = 30pF, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at A_V = +1, R_S = 5Ω, C_L = 340pF.

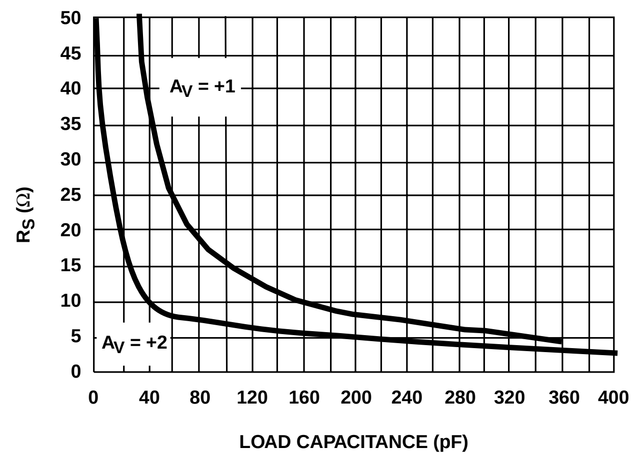


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1113 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R_2), and leave the connection open.
2. a. For A_V = +1 evaluation, remove the 500Ω gain setting resistor (R_1), and leave pin 2 floating.
   b. For A_V = +2, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The modified schematic and layout of the board are shown in Figures 2 and 3.

To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

NOTE: The SOIC version may be evaluated in the DIP board by using a SOIC-to-DIP adapter such as Aries Electronics Part Number 08-350000-10.

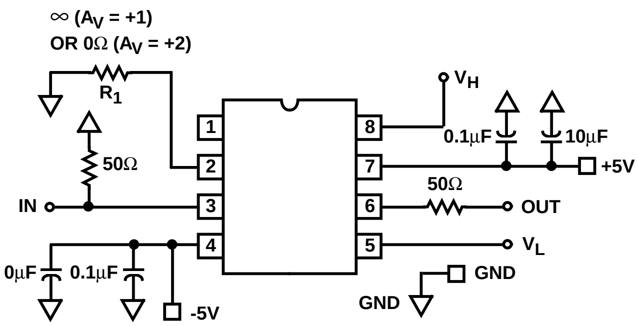


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

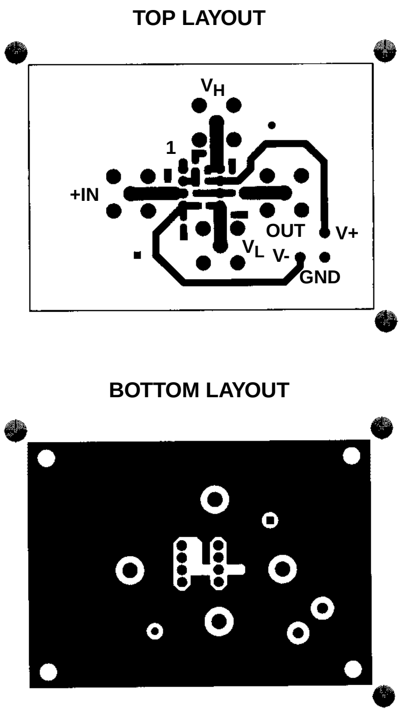


FIGURE 3. EVALUATION BOARD LAYOUT

Limiting Operation

General

The HFA1113 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 4 shows a simplified schematic of the HFA1113 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2}) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of:

$(V_{-IN} - V_{OUT})/R_F + V_{-IN}/R_G$

This current is mirrored onto the high impedance node (Z) by Q_{X3}-Q_{X4}, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4}. Note that when the output reaches its quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (Q_{N6} and Q_{P6}) to set up the base voltage on Q_{P5}.

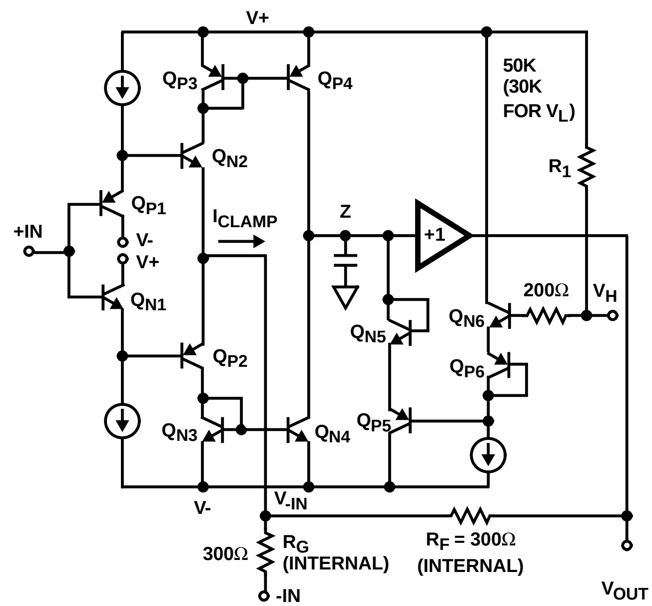


FIGURE 4. HFA1113 SIMPLIFIED V_H CLAMP CIRCUITRY

Q_{P5} begins to conduct whenever the high impedance node reaches a voltage equal to Q_{P5}'s base voltage + $2V_{BE}$ (Q_{P5} and Q_{N5}). Thus, Q_{P5} clamps node Z whenever Z reaches V_H. R_1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as:

$I_{CLAMP} = (V_{-IN} - V_{OUT\ CLAMPED})/300\Omega + V_{-IN}/R_G$.

As an example, a unity gain circuit with V_{IN} = 2V, and V_H = 1V, would have I_{CLAMP} = (2V - 1V)/300Ω + 2V/∞ = 3.33mA (R_G = ∞ because -IN is floated for unity gain applications). Note that I_{CC} will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 4, it can be seen that one component of clamp accuracy is the VBE mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level (A_{VCL} x V_{IN} - $V_{OUT\ CLAMPED}$), so clamp accuracy degrades as the overdrive increases. As an example, the specified accuracy of ±100mV (A_V = -1, V_H = 1V) for a 1.6X overdrive degrades to ±240mV for a 3X (200%) overdrive, as shown in Figure 43.

Consideration must also be given to the fact that the clamp voltages have an affect on amplifier linearity. The “Nonlinearity Near Clamp Voltage” curve, Figure 48, illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1113 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won’t be in a DC output voltage from an AC input signal. A 150mV - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP}/A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of “Unclamped Performance” and “Clamped Performance” (Figures 41 and 42) highlight the HFA1113’s subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 8.0ns for the unclamped pulse, and 8.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1113 propagation delay is 500ps.

Overdrive recovery time is also a function of the overdrive level. Figure 47 details the overdrive recovery time for various clamp and overdrive levels.

Typical Performance Curves

V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified

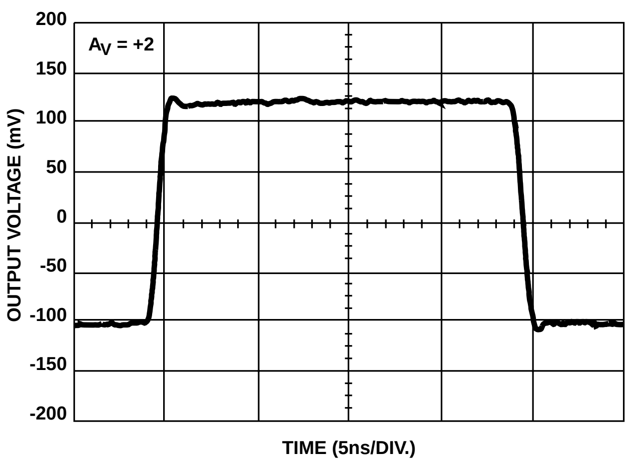


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

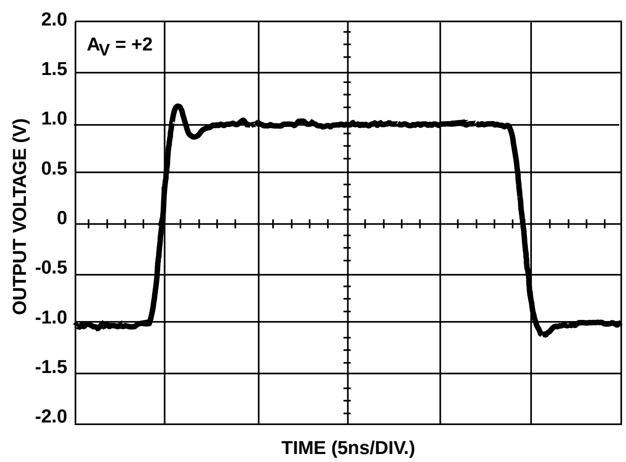


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

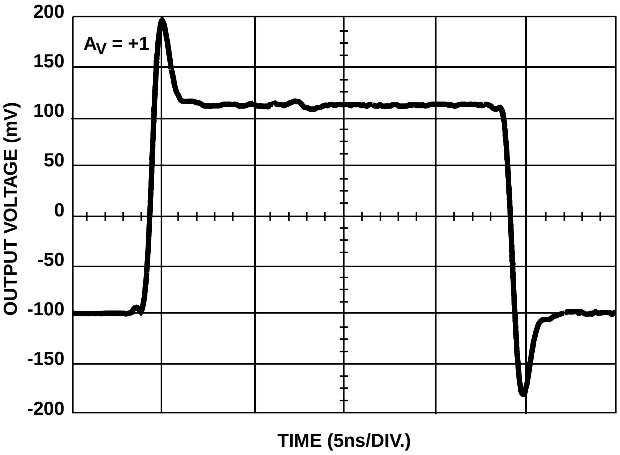


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

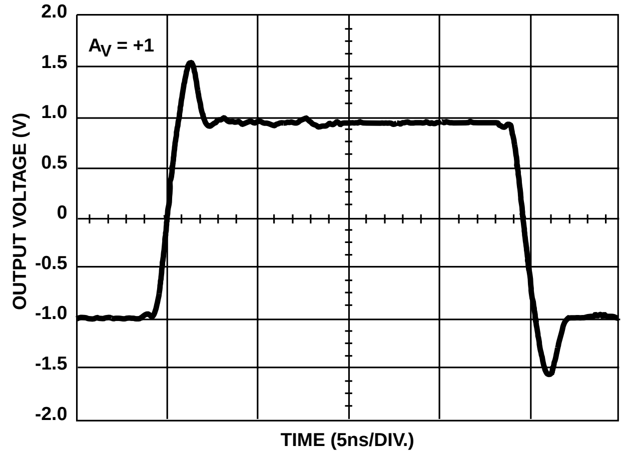


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

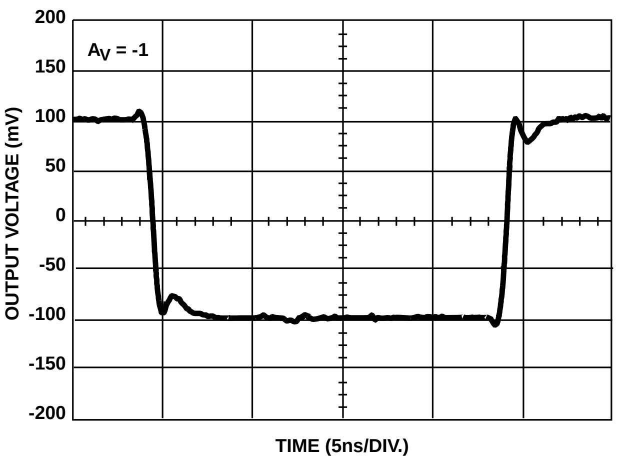


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

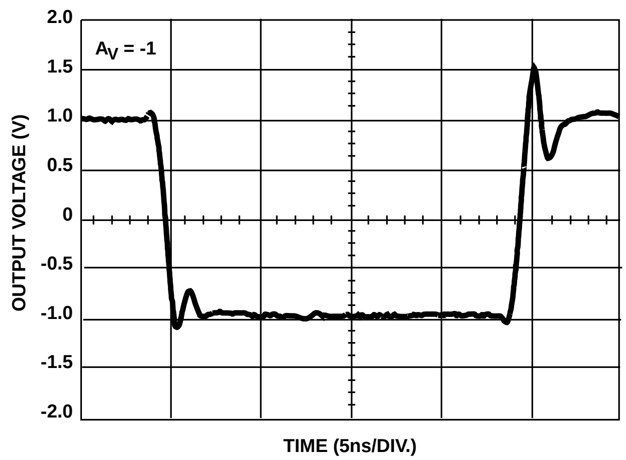


FIGURE 10. LARGE SIGNAL PULSE RESPONSE

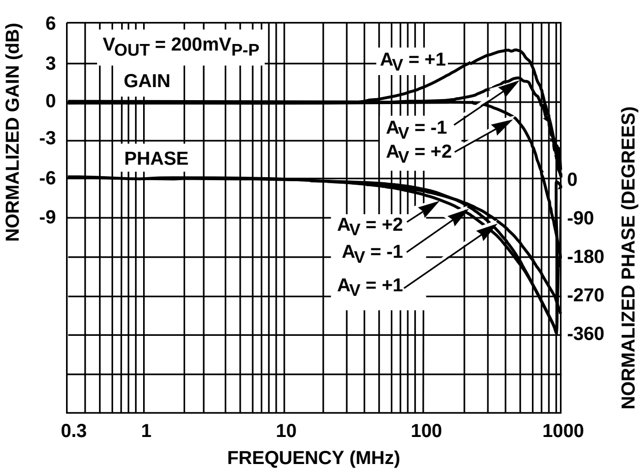


FIGURE 11. FREQUENCY RESPONSE

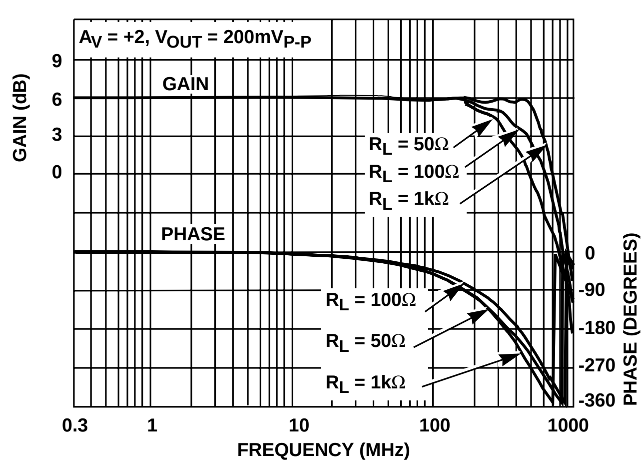


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

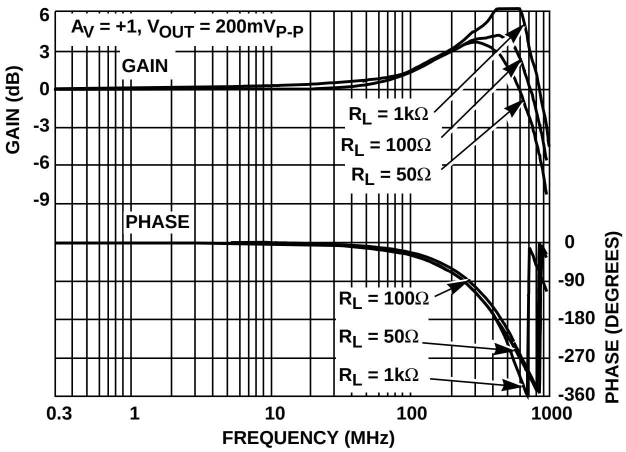


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

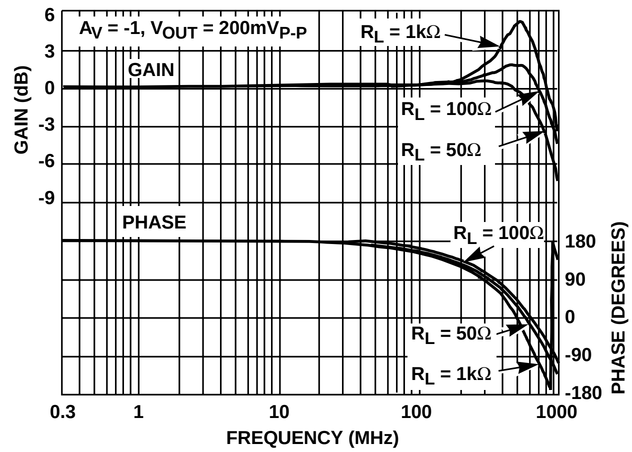


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

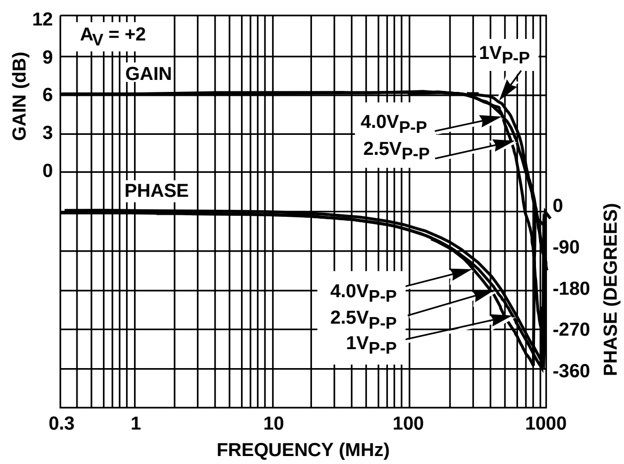


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

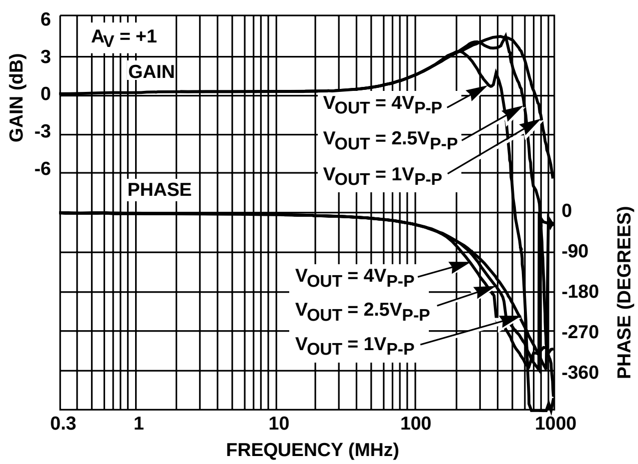


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

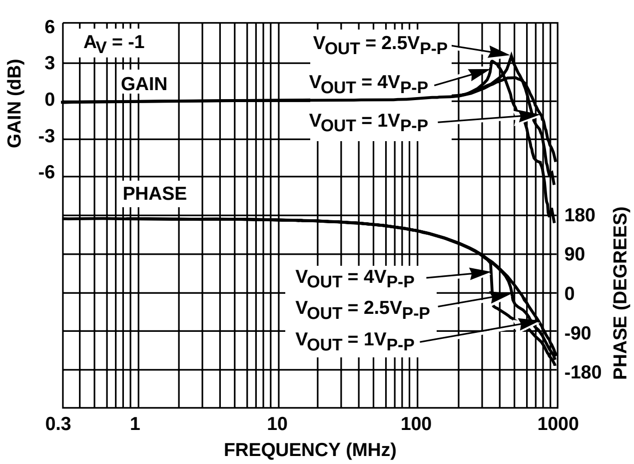


FIGURE 17. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

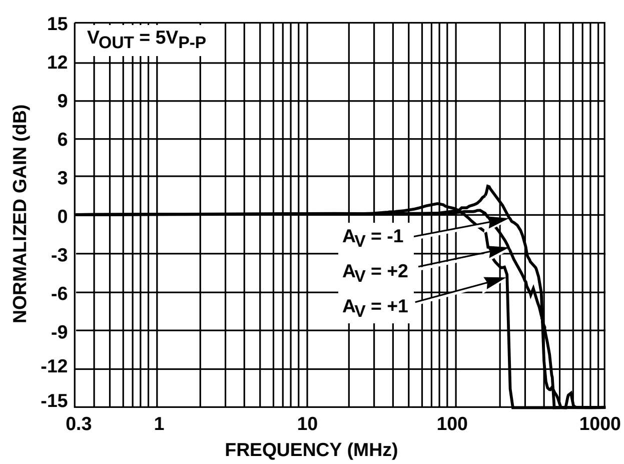


FIGURE 18. FULL POWER BANDWIDTH

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

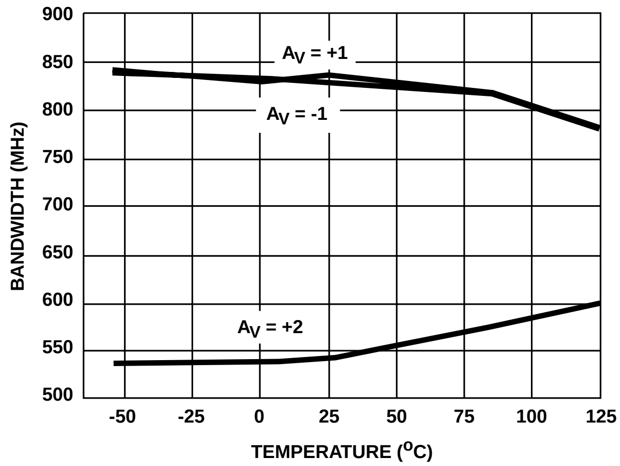


FIGURE 19. -3dB BANDWIDTH vs TEMPERATURE

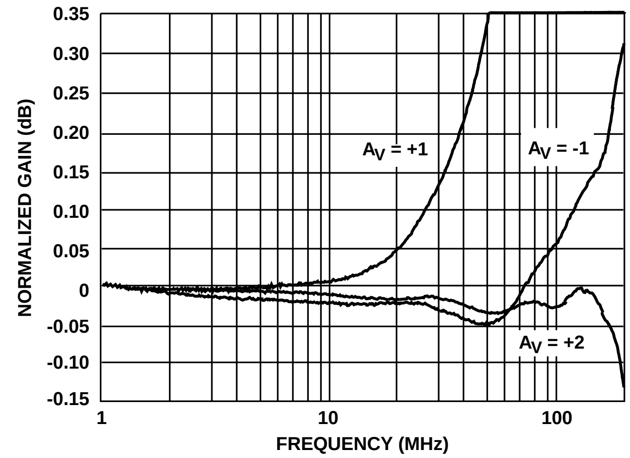


FIGURE 20. GAIN FLATNESS

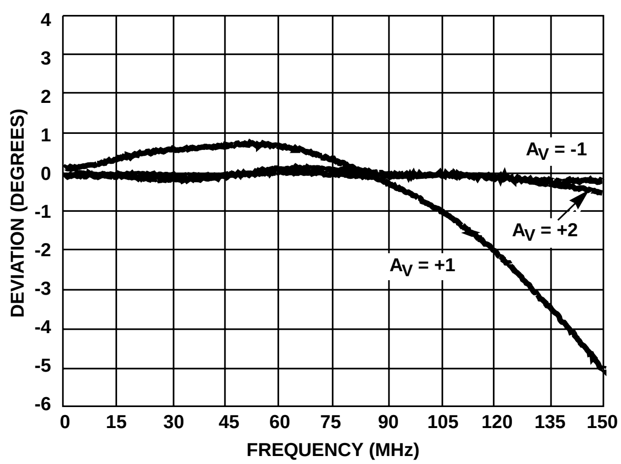


FIGURE 21. DEVIATION FROM LINEAR PHASE

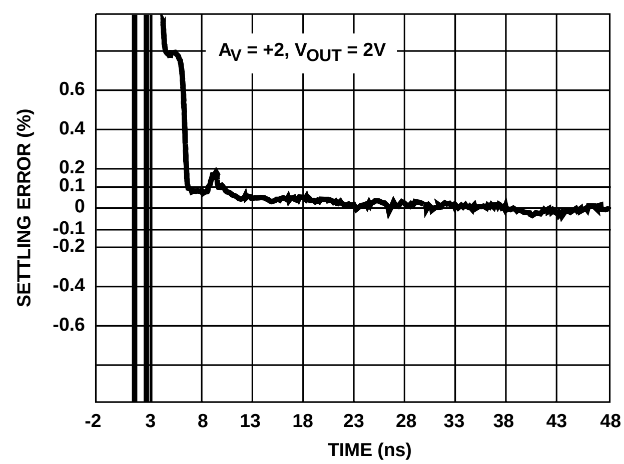


FIGURE 22. SETTLING RESPONSE

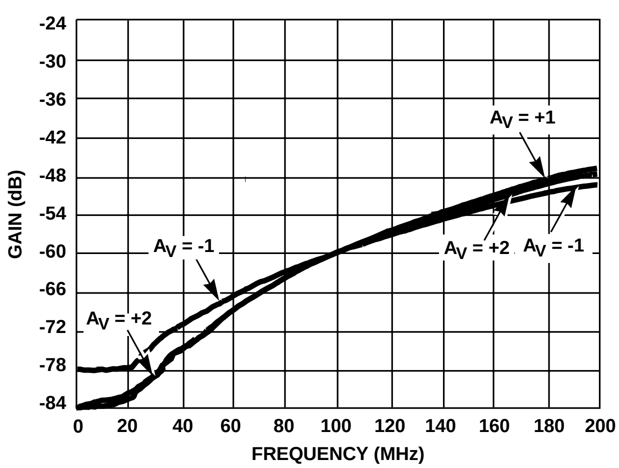


FIGURE 23. LOW FREQUENCY REVERSE ISOLATION (S_{12})

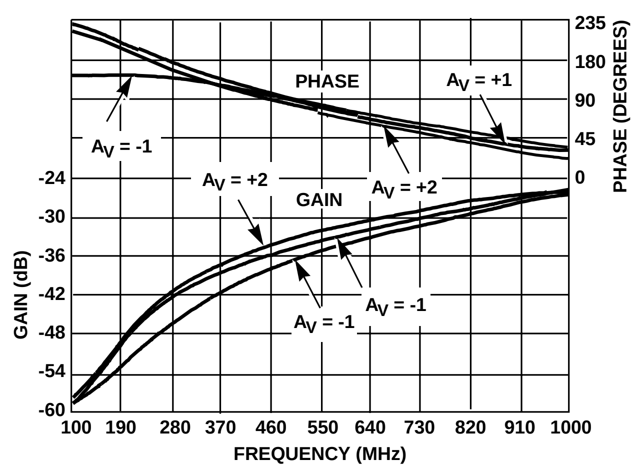


FIGURE 24. HIGH FREQUENCY REVERSE ISOLATION (S_{12})

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

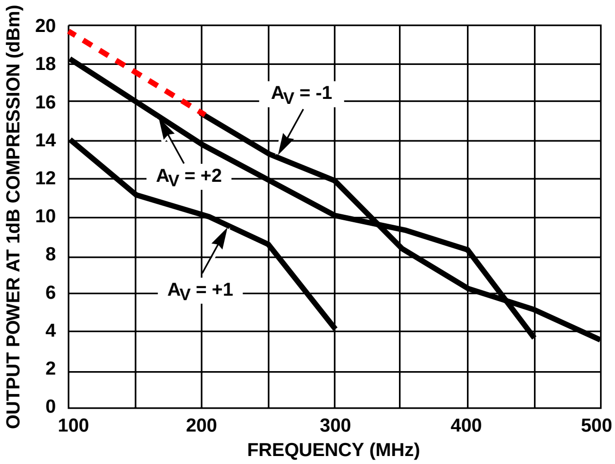


FIGURE 25. 1dB GAIN COMPRESSION vs FREQUENCY

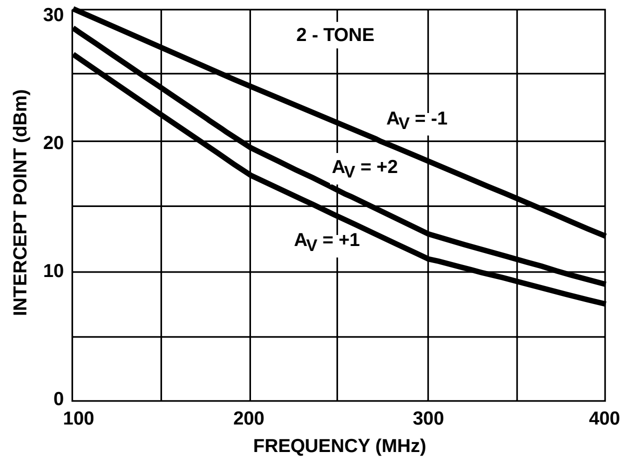


FIGURE 26. THIRD ORDER INTERMODULATION INTERCEPT vs FREQUENCY

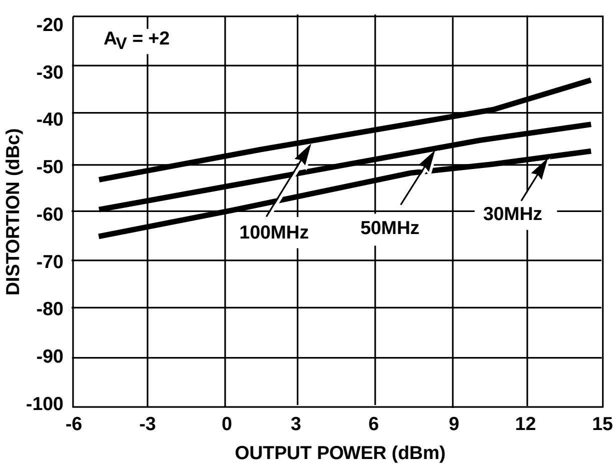


FIGURE 27. SECOND HARMONIC DISTORTION vs P_{OUT}

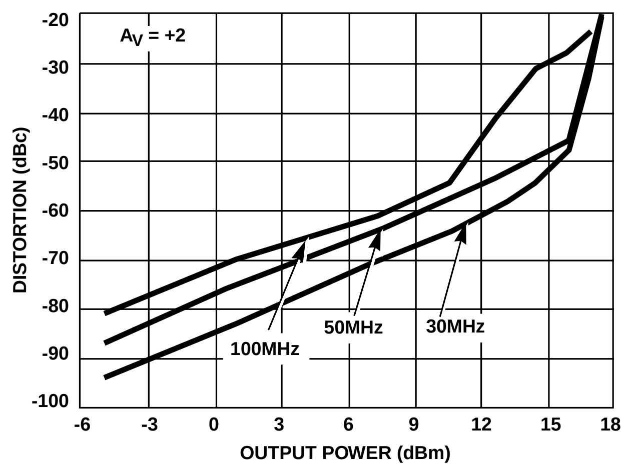


FIGURE 28. THIRD HARMONIC DISTORTION vs P_{OUT}

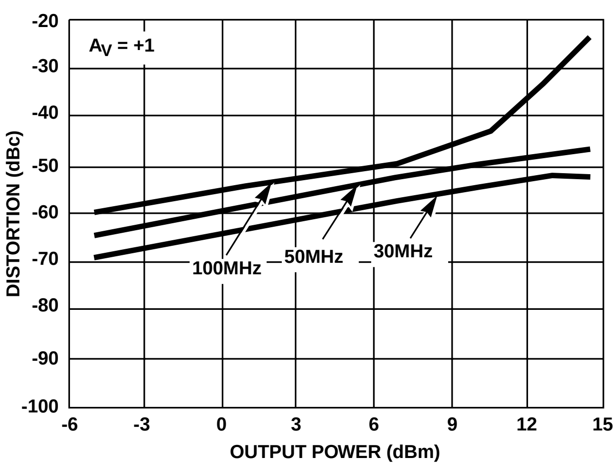


FIGURE 29. SECOND HARMONIC DISTORTION vs P_{OUT}

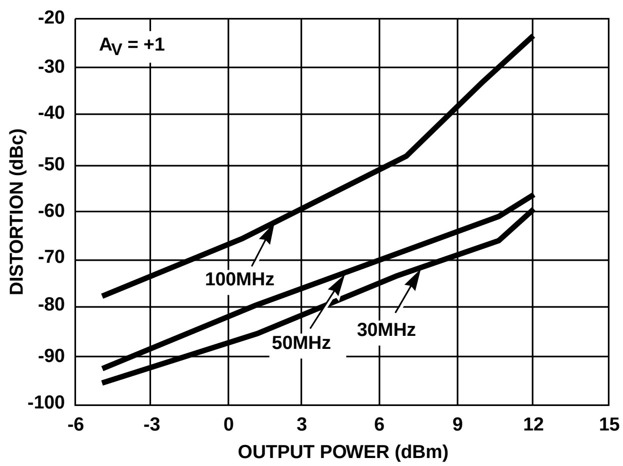


FIGURE 30. THIRD HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

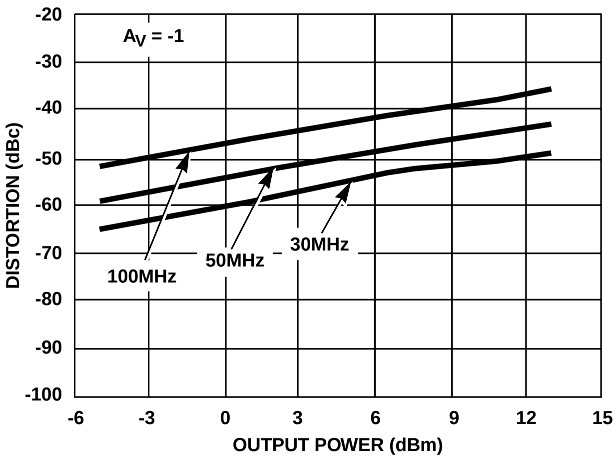


FIGURE 31. SECOND HARMONIC DISTORTION vs P_{OUT}

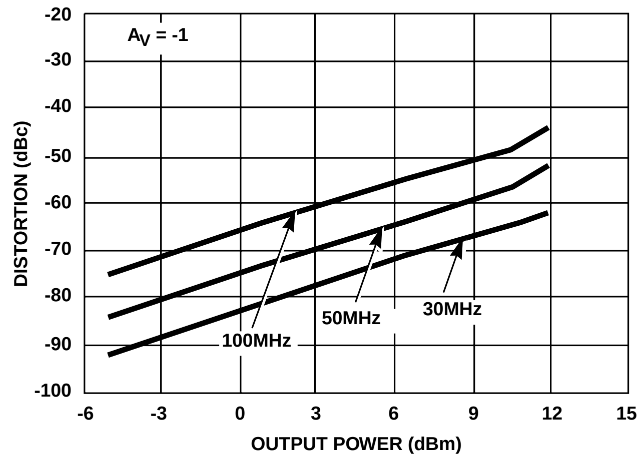


FIGURE 32. THIRD HARMONIC DISTORTION vs P_{OUT}

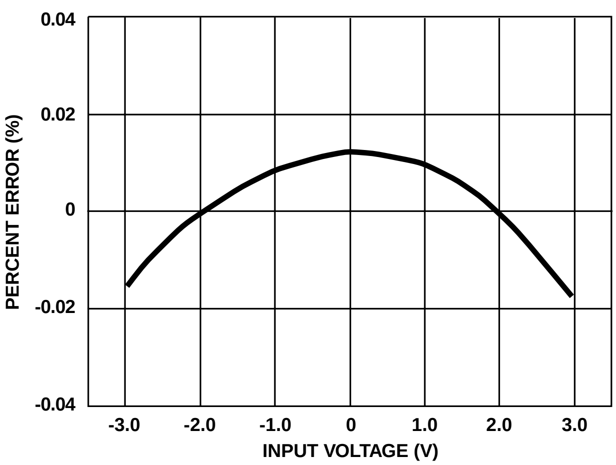


FIGURE 33. INTEGRAL LINEARITY ERROR

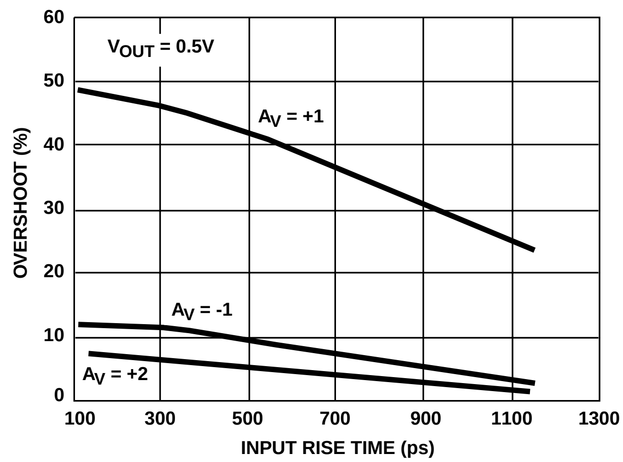


FIGURE 34. OVERSHOOT vs INPUT RISE TIME

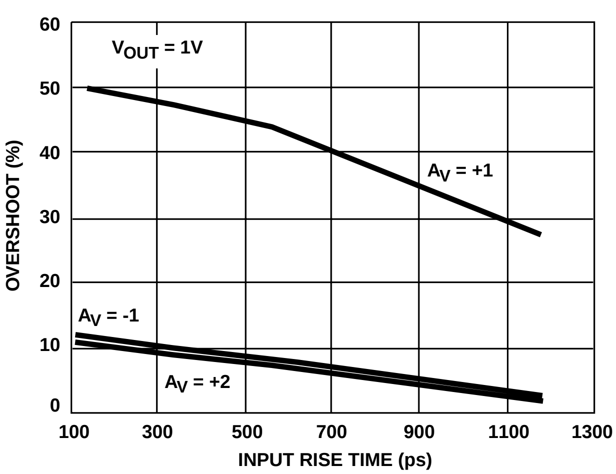


FIGURE 35. OVERSHOOT vs INPUT RISE TIME

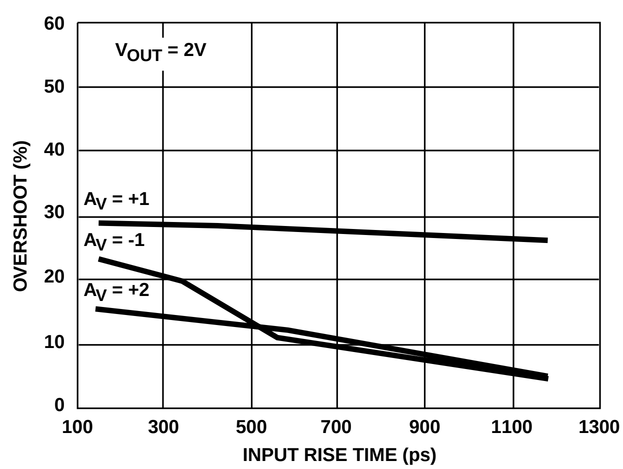


FIGURE 36. OVERSHOOT vs INPUT RISE TIME

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

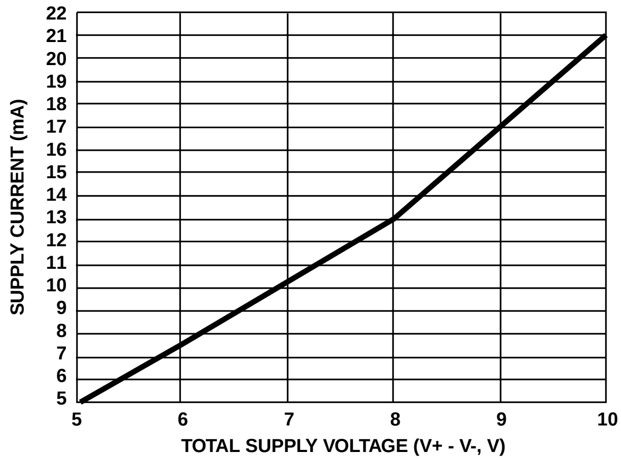


FIGURE 37. SUPPLY CURRENT vs SUPPLY VOLTAGE

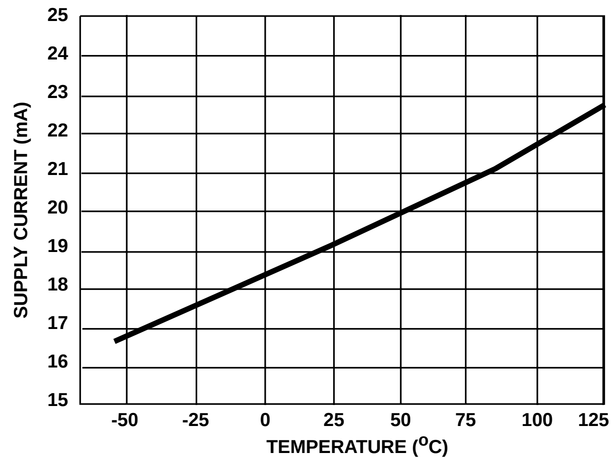


FIGURE 38. SUPPLY CURRENT vs TEMPERATURE

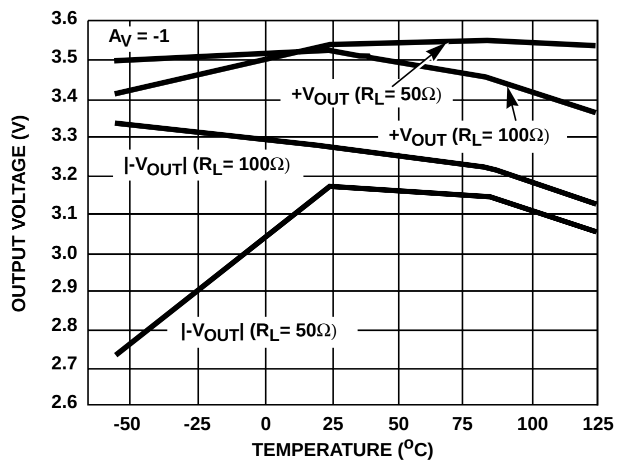


FIGURE 39. OUTPUT VOLTAGE vs TEMPERATURE

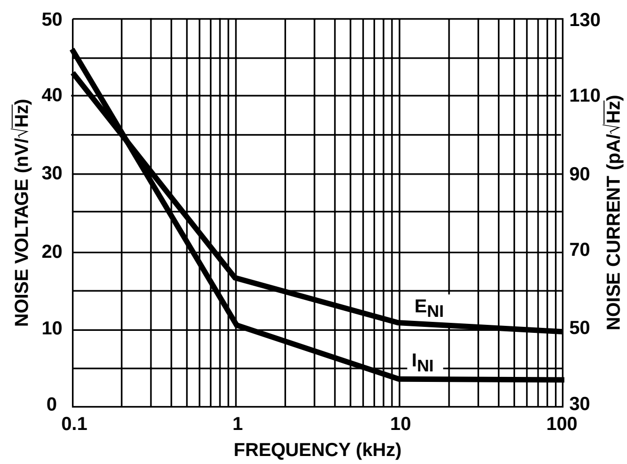


FIGURE 40. INPUT NOISE CHARACTERISTICS

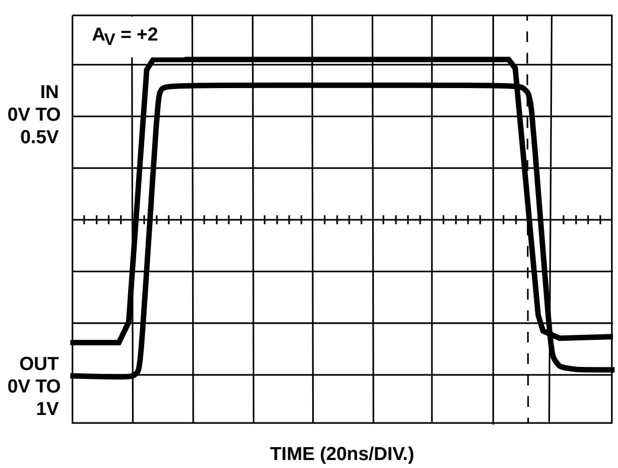


FIGURE 41. UNCLAMPED PERFORMANCE

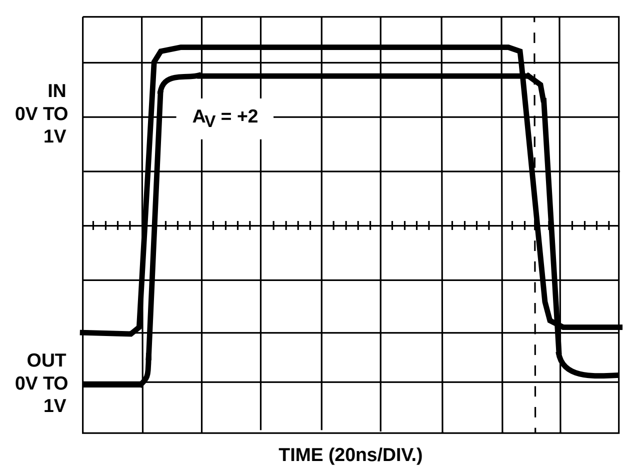


FIGURE 42. CLAMPED PERFORMANCE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

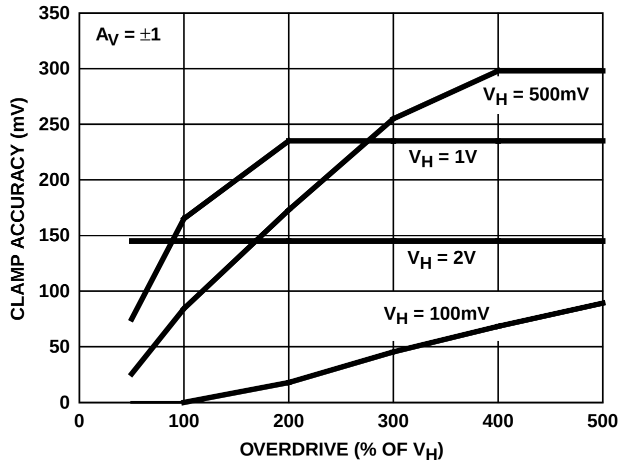


FIGURE 43. V_H CLAMP ACCURACY vs OVERDRIVE

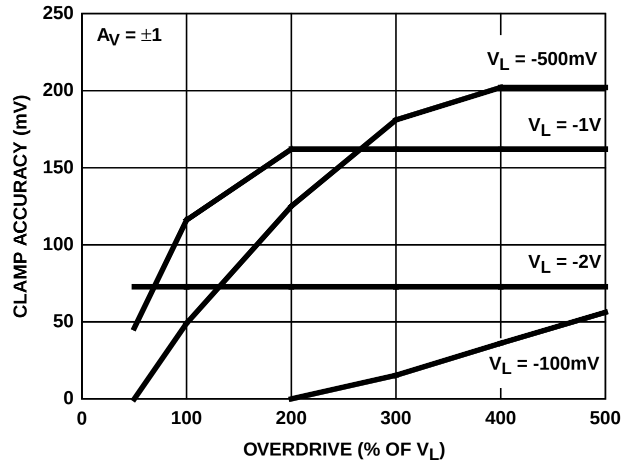


FIGURE 44. V_L CLAMP ACCURACY vs OVERDRIVE

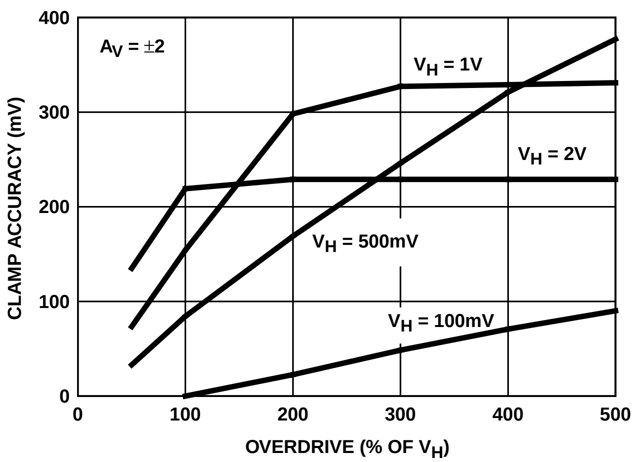


FIGURE 45. V_H CLAMP ACCURACY vs OVERDRIVE

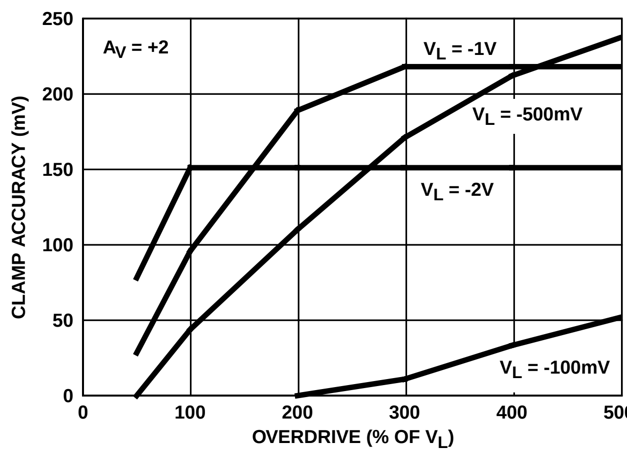


FIGURE 46. V_L CLAMP ACCURACY vs OVERDRIVE

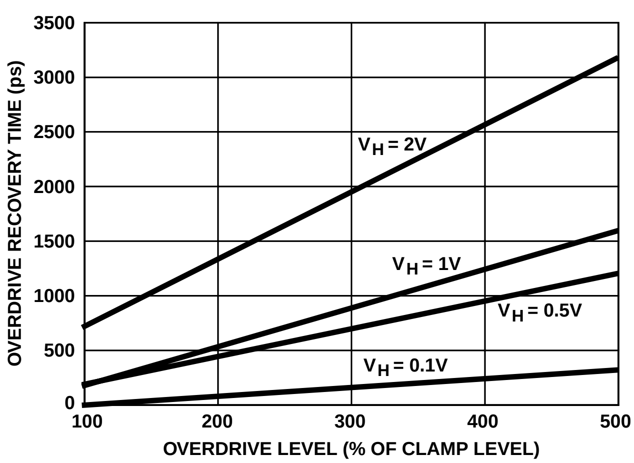


FIGURE 47. OVERDRIVE RECOVERY vs OVERDRIVE

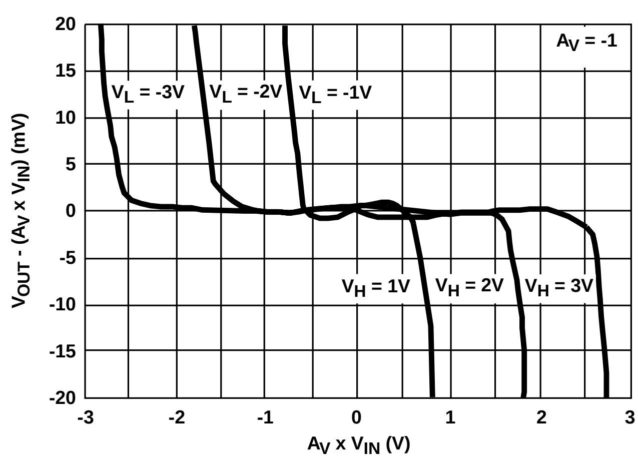


FIGURE 48. NON-LINEARITY NEAR CLAMP VOLTAGE

Typical Performance Curves

$V_{SUPPLY} = \pm 5V$, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

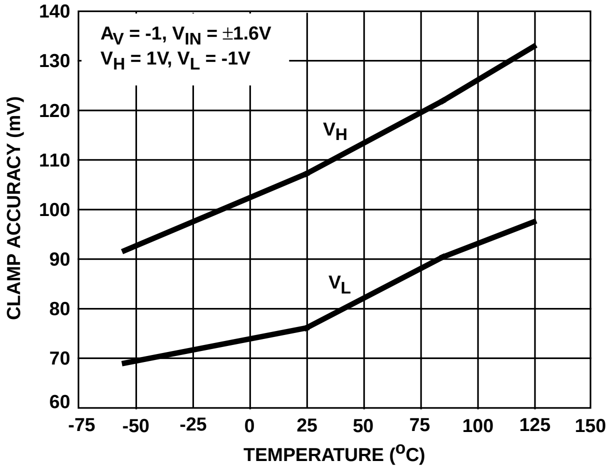


FIGURE 49. CLAMP ACCURACY vs TEMPERATURE

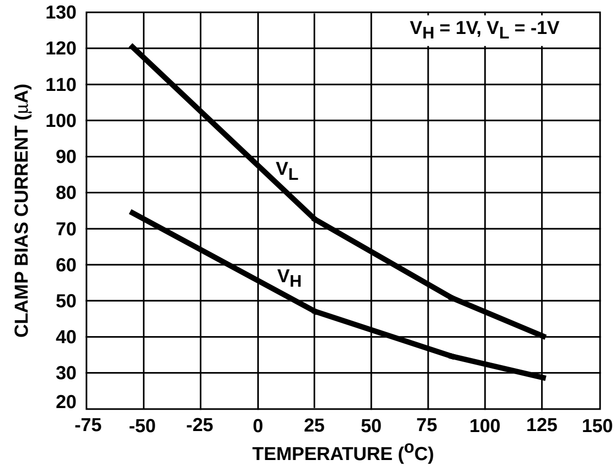


FIGURE 50. CLAMP BIAS CURRENT vs TEMPERATURE

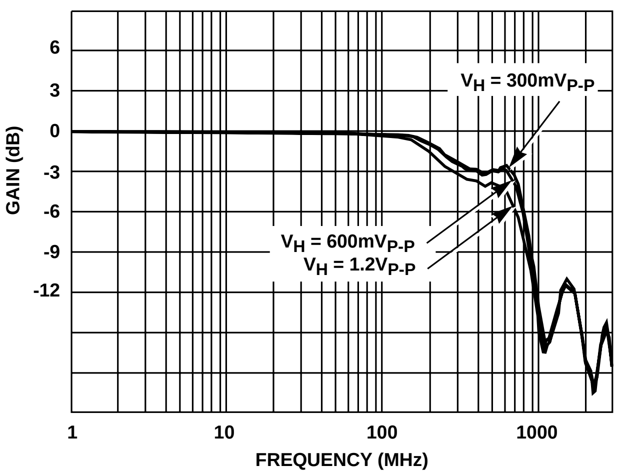


FIGURE 51. V_H CLAMP INPUT BANDWIDTH

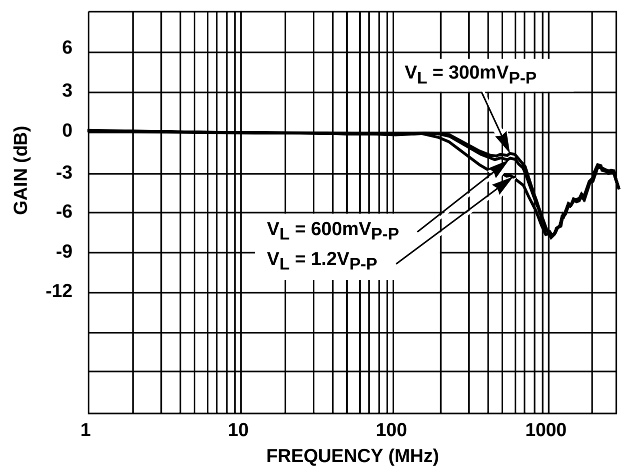


FIGURE 52. V_L CLAMP INPUT BANDWIDTH

Die Characteristics

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils
1600µm x 1130µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT:

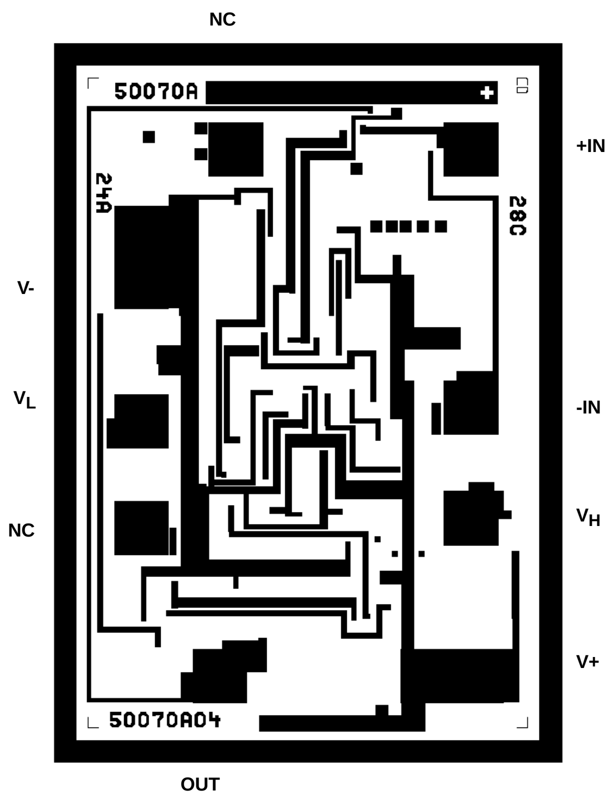
52

SUBSTRATE POTENTIAL (POWERED UP):

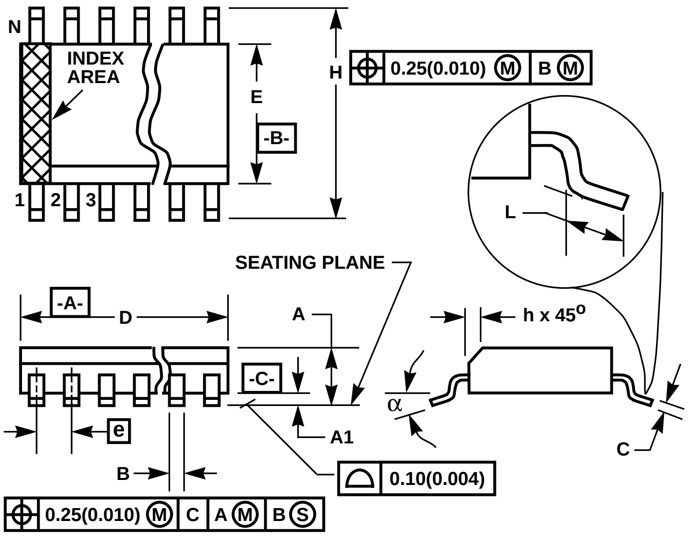
Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1113



Small Outline Plastic Packages (SOIC)



M8.15 **(JEDEC MS-012-AA ISSUE C)**
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029