Data Sheet | October 1998 | File Number 1491.3

4A, 350V and 400V, 2.000 Ohm, N-Channel Power MOSFETs

These are N-channel enhancement-mode silicon-gate power field effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17404.

Ordering Information

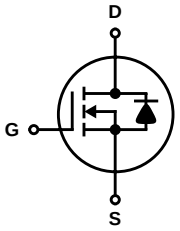
PART NUMBER	PACKAGE	BRAND
RFM4N35	TO-204AA	RFM4N35
RFM4N40	TO-204AA	RFM4N40
RFP4N35	TO-220AB	RFP4N35
RFP4N40	TO-220AB	RFP4N40

NOTE: When ordering, use the entire part number.

Features

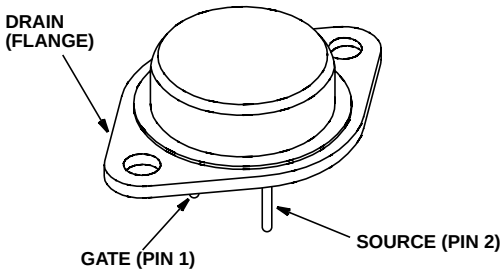
- 4A, 350V and 400V
- $r_{DS(ON)} = 2.000\Omega$
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

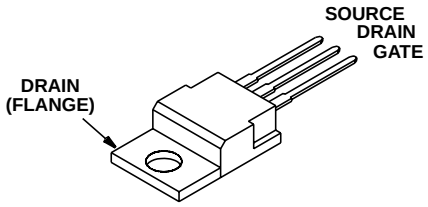


Packaging

JEDEC TO-204AA



JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$ Unless Otherwise Specified

	RFM4N35	RFM4N40	RFP4N35	RFP4N40	UNITS
Drain to Source Voltage (Note 1) . . . . . V_{DS}	350	400	350	400	V
Drain to Gate Voltage (R_{GS} = 1MΩ) (Note 1) . . . . . V_{DGR}	350	400	350	400	V
Continuous Drain Current . . . . . I_D	4	4	4	4	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	8	8	8	8	A
Gate to Source Voltage . . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation . . . . . P_D	75	75	60	60	W
Linear Derating Factor	0.6	0.6	0.48	0.48	$W/^oC$
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 150	-55 to 150	-55 to 150	-55 to 150	^oC
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	300	300	300	^oC
Package Body for 10s, See Techbrief 334 (for TO-220) . . . . . T_{pkg}	260	260	260	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0				
RFM4N40, RFP4N40			400	-	-	V
RFM4N35, RFP4N35			350	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA (Figure 8)	2	-	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}	-	-	1	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, $T_C = 125^oC$	-	-	25	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 4A, V_{GS} = 10V (Figures 6, 7)	-	-	2.000	Ω
Drain to Source On-Voltage (Note 2)	$V_{DS(ON)}$	I_D = 4A, V_{GS} = 10V	-	-	8	V
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 200V, I_D = 2A, R_G = 50Ω, R_L = 100Ω, V_{GS} = 10V (Figures 10, 11, 12)	-	12	45	ns
Rise Time	t_r		-	42	60	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	130	200	ns
Fall Time	t_f		-	62	100	ns
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V f = 1MHz (Figure 9)	-	-	750	pF
Output Capacitance	C_{OSS}		-	-	150	pF
Reverse-Transfer Capacitance	C_{RSS}		-	-	100	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	RFM4N35, RFM4N40	-	-	1.67	$^oC/W$
		RFP4N35, RFP4N40	-	-	2.083	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 2A	-	-	1.4	V
Reverse Recorvery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 100A/µs	-	800	-	ns

NOTES:

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves

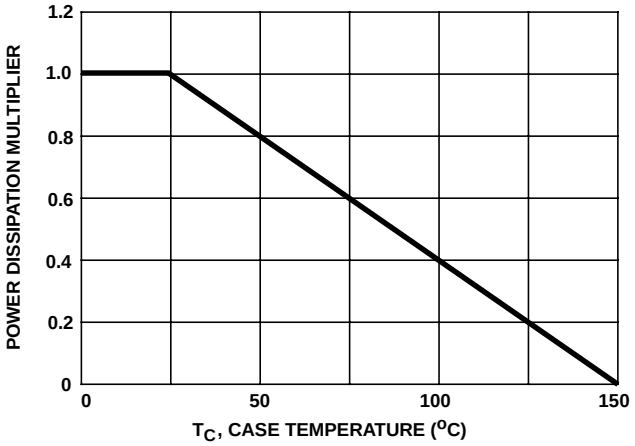


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

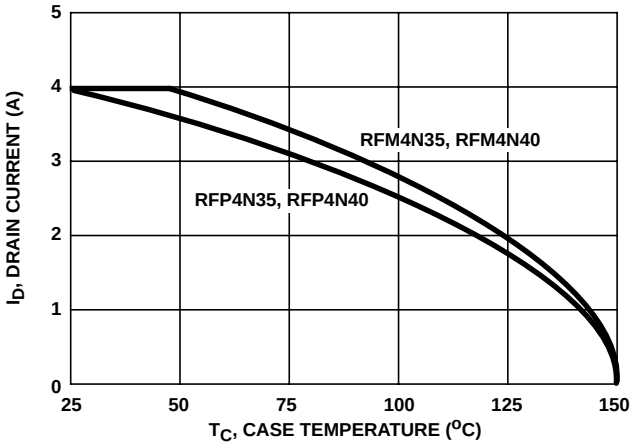


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

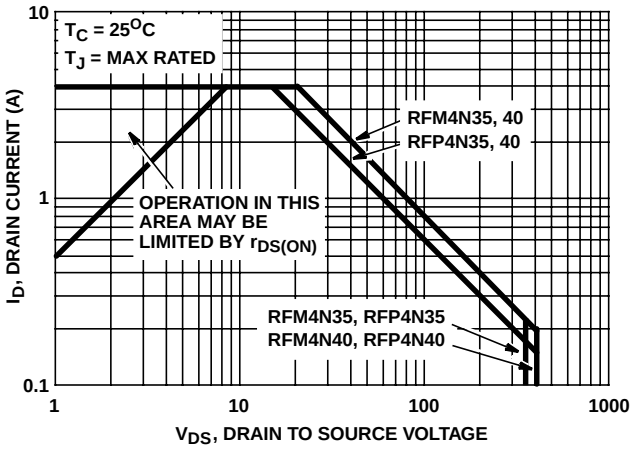


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

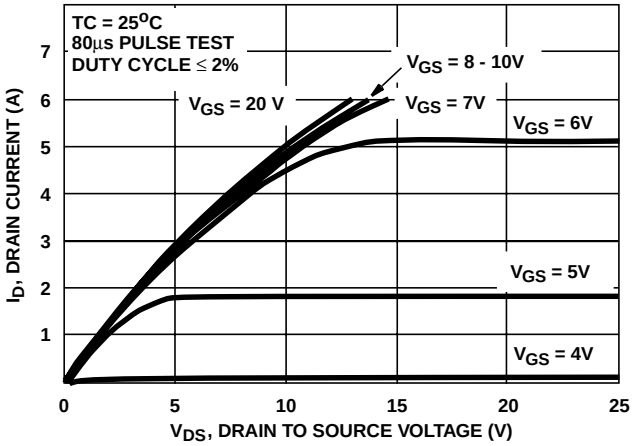


FIGURE 4. SATURATION CHARACTERISTICS

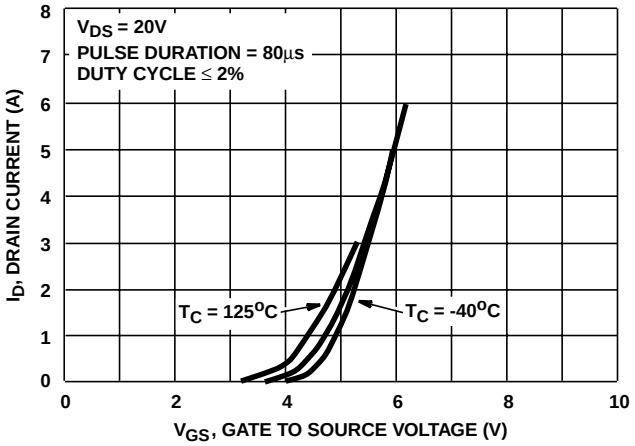


FIGURE 5. TRANSFER CHARACTERISTICS

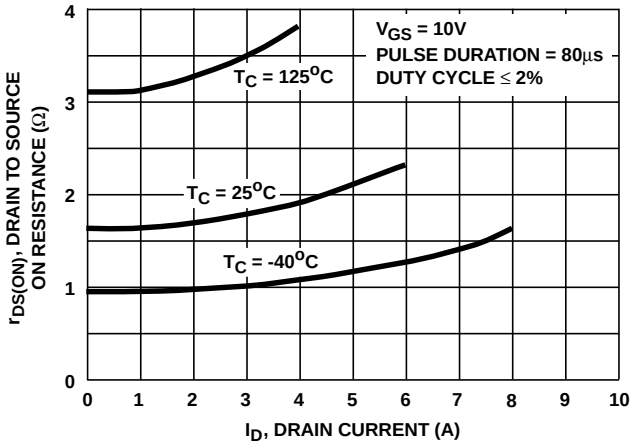


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves (Continued)

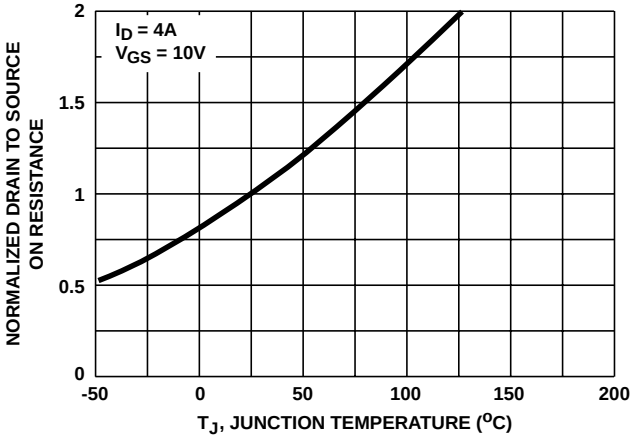


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

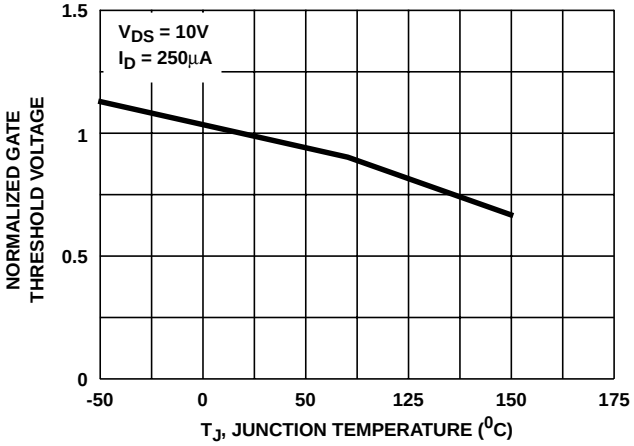


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

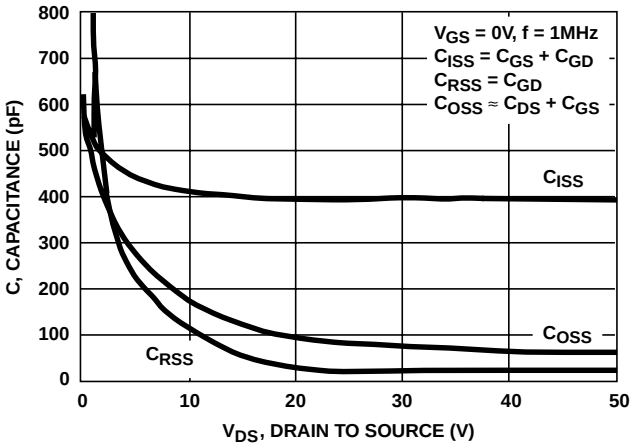
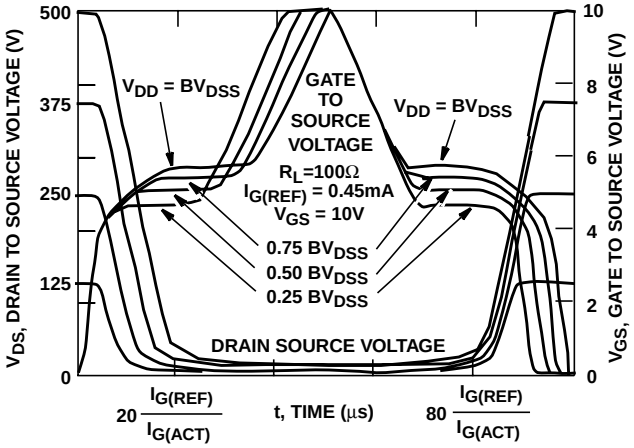


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

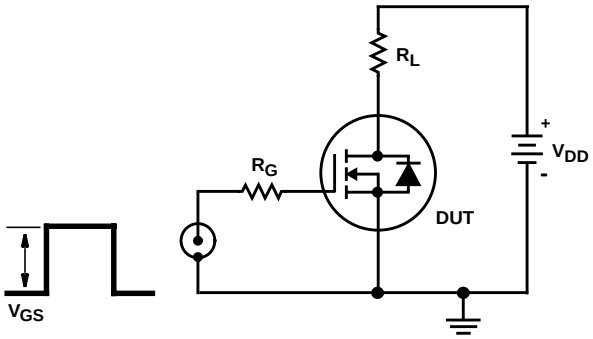


FIGURE 11. SWITCHING TIME TEST CIRCUIT

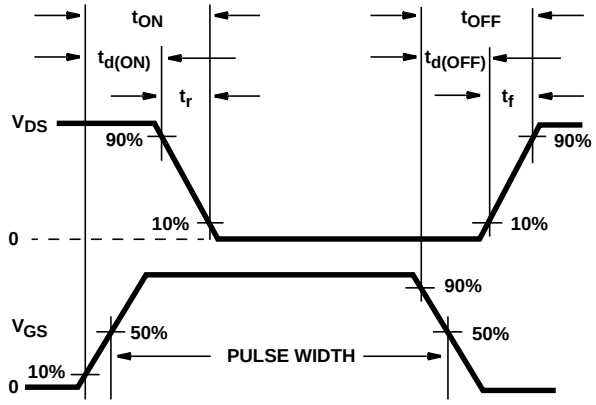


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS