

## 25A, 60V, 0.047 Ohm, N-Channel Power MOSFETs

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA09771.

### Ordering Information

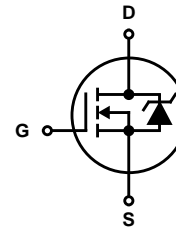
PART NUMBER	PACKAGE	BRAND
RFP25N06	TO-220AB	RFP25N06
RF1S25N06SM	TO-263AB	F1S25N06

NOTE: When ordering use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S25N06SM9A.

### Features

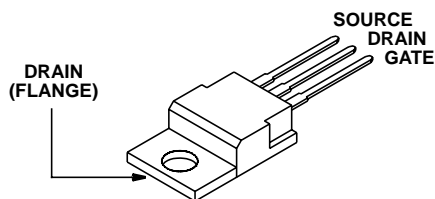
- 25A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

### Symbol

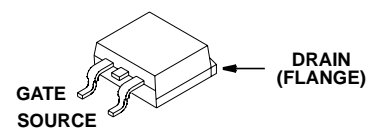


### Packaging

JEDEC TO- 220AB



JEDEC TO-263AB



# RFP25N06, RF1S25N06SMS

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFP25N06, RF1S25N06SM	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	60 V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	60 V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$ V
Continuous Drain Current (Figure 2) . . . . .	$I_D$	25 A
Pulsed Drain Current . . . . .	$I_{DM}$	(Figure 5)
Single Pulse Avalanche Rating . . . . .	$E_{AS}$	(Figure 6)
Power Dissipation . . . . .	$P_D$	72 W
Linear Derating Factor . . . . .		0.48 $\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range . . . . .	$T_J, T_{STG}$	$-55$ to $175$ $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 11)	60	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{V}$ $T_C = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	50	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 25\text{A}, V_{GS} = 10\text{V}$ (Figure 9)	-	-	0.047	$\Omega$
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}, I_D = 12.5\text{A}$ $R_L = 2.4\Omega, V_{GS} = 10\text{V}$ $R_{GS} = 10\Omega$ (Figure 13)	-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$		-	14	-	ns
Rise Time	$t_r$		-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	45	-	ns
Fall Time	$t_f$		-	22	-	ns
Turn-Off Time	$t_{OFF}$		-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0$ to $20\text{V}$	-	-	80	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0$ to $10\text{V}$				
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0$ to $2\text{V}$				
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$ (Figure 12)	-	975	-	pF
Output Capacitance	$C_{OSS}$		-	330	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	95	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)	-	-	2.083	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	62	$^\circ\text{C}/\text{W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 25\text{A}$	-	-	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 25\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

Typical Performance Curves Unless Otherwise Specified

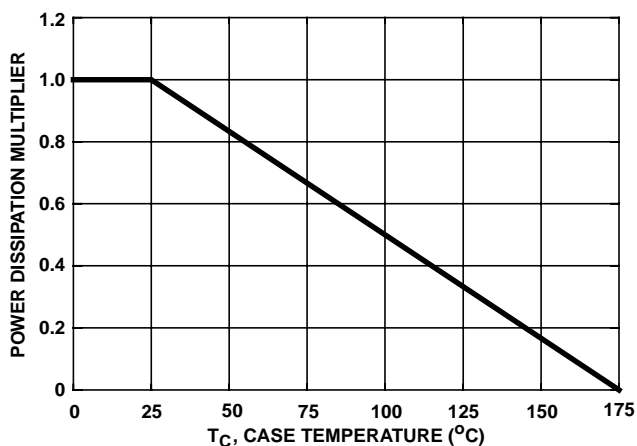


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

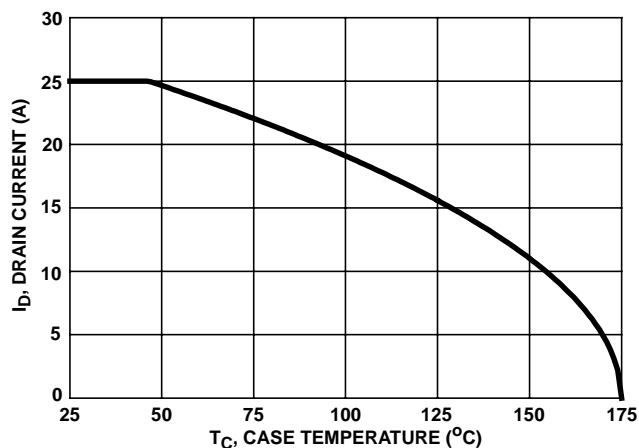


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

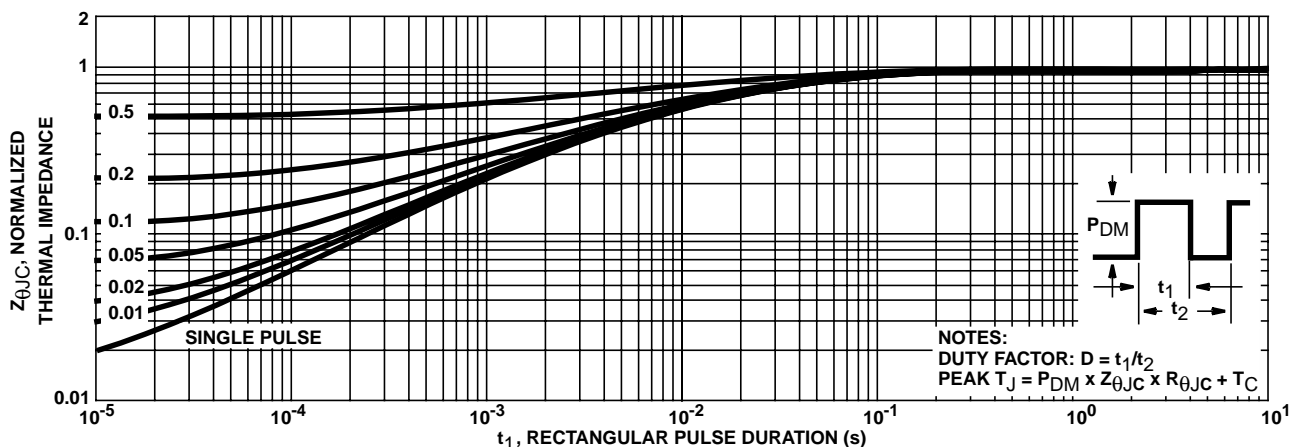


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

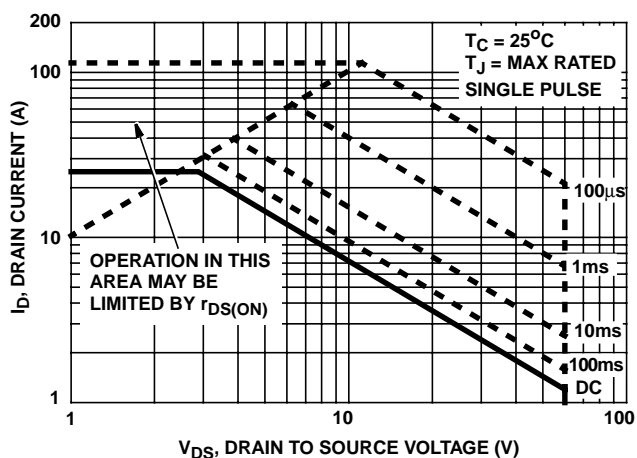


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

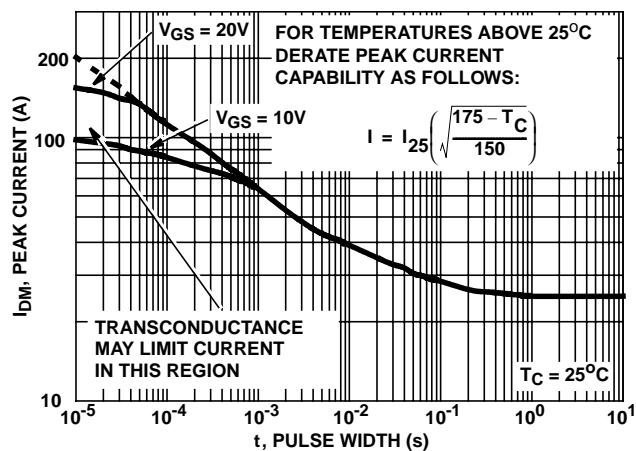
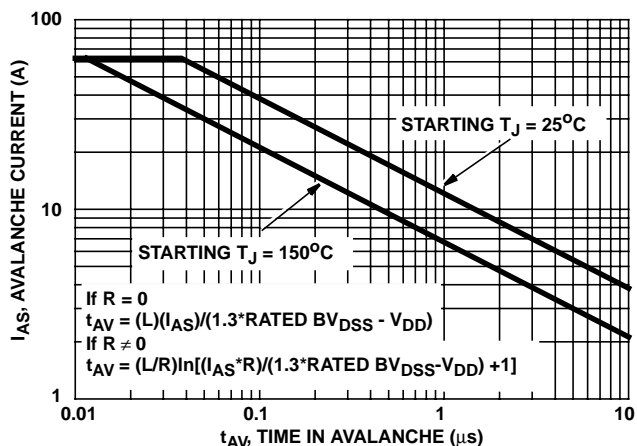


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

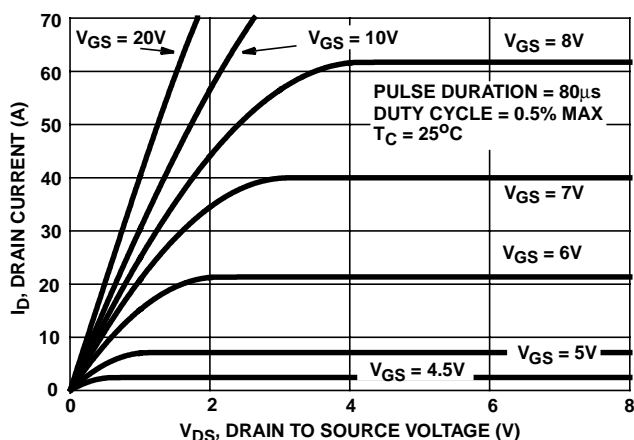


FIGURE 7. SATURATION CHARACTERISTICS

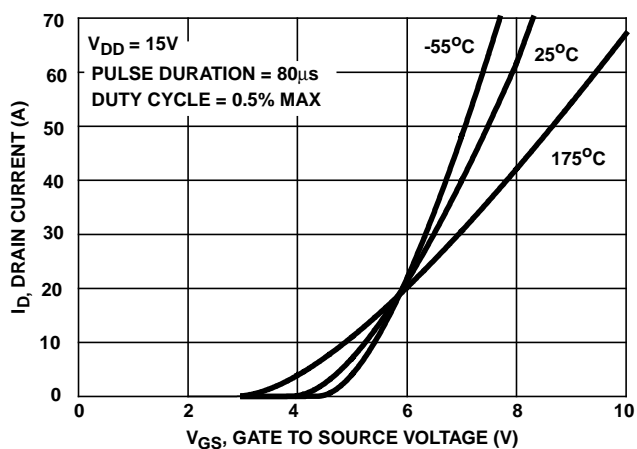


FIGURE 8. TRANSFER CHARACTERISTICS

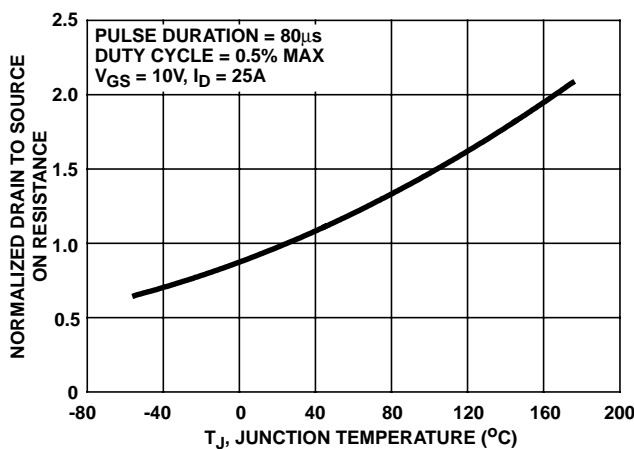


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

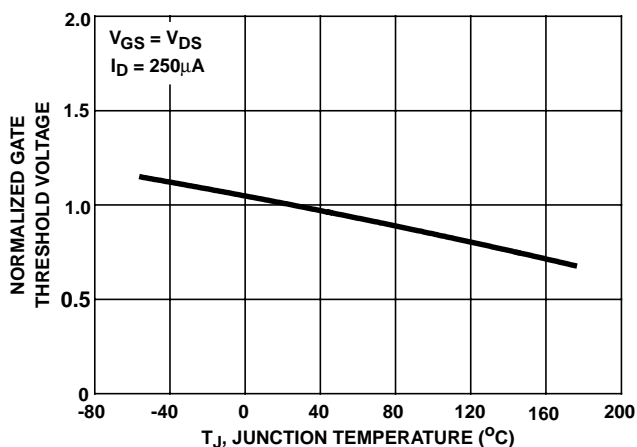


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

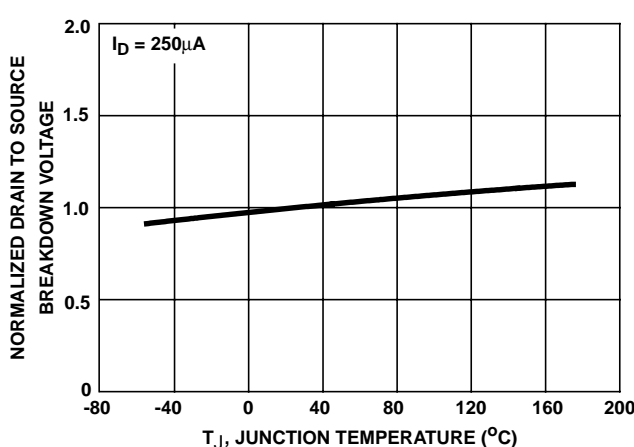


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

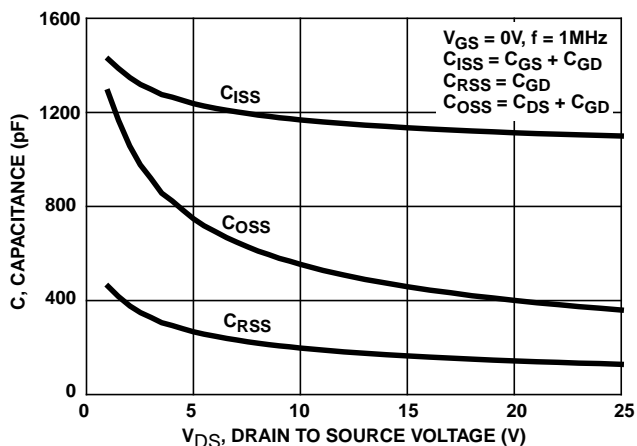
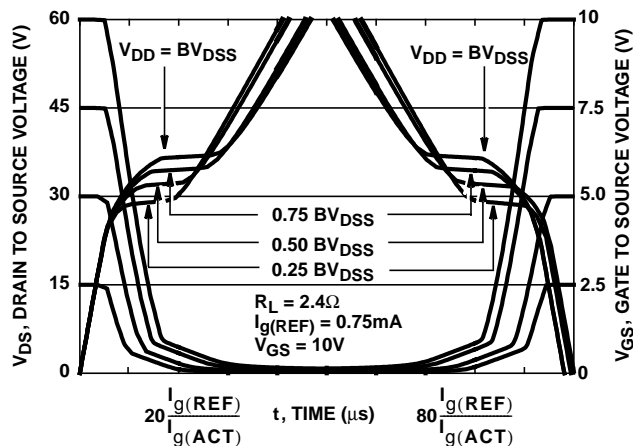


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

**Test Circuits and Waveforms**

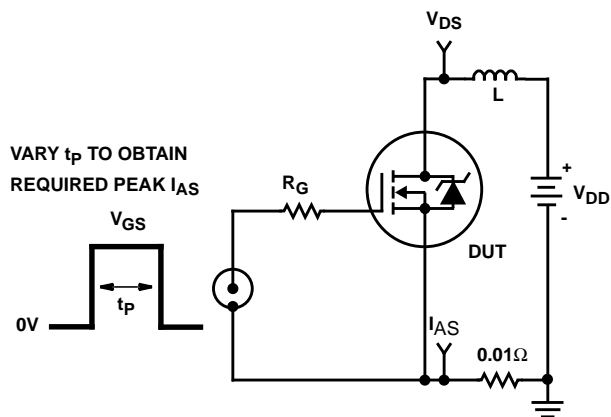


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

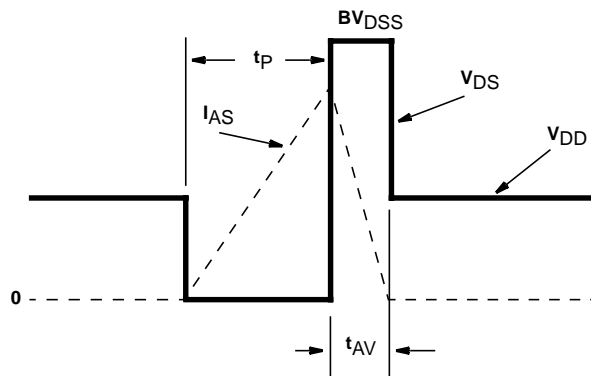


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

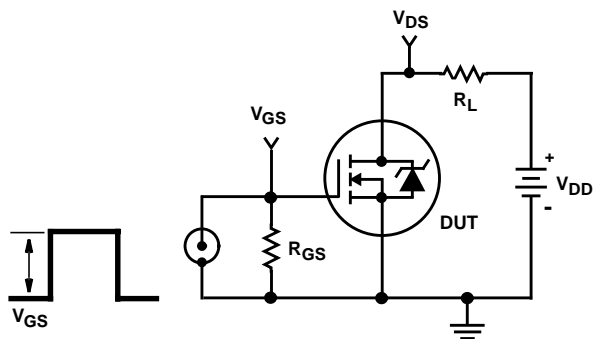


FIGURE 16. SWITCHING TIME TEST CIRCUIT

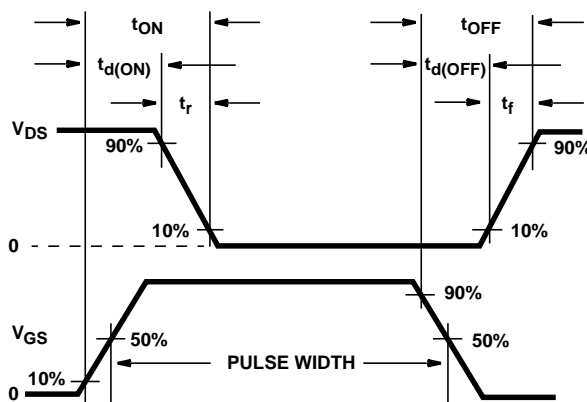


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

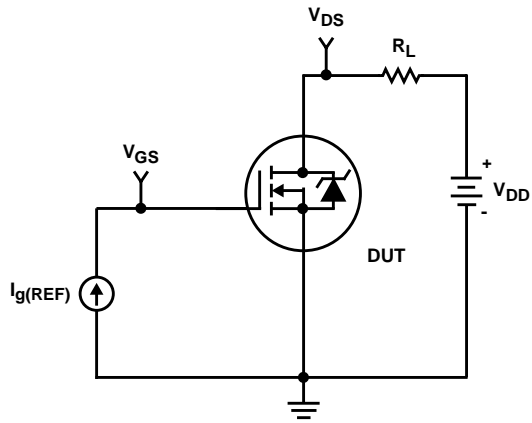


FIGURE 18. GATE CHARGE TEST CIRCUIT

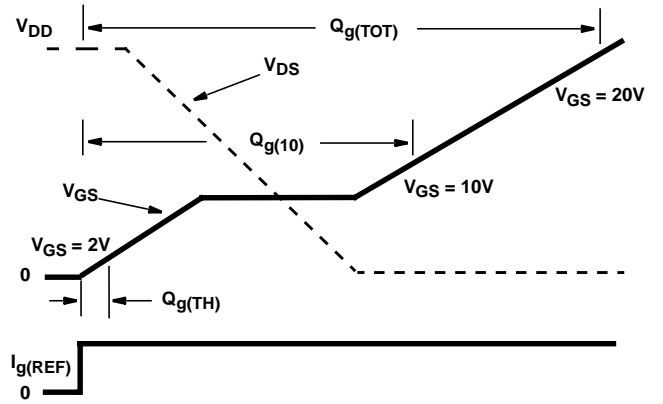


FIGURE 19. GATE CHARGE WAVEFORM

**PSPICE Electrical Model**

.SUBCKT RFP25N06 2 1 3 ; rev 8/19/94

CA 12 8 1.83e-9  
CB 15 14 1.98e-9  
CIN 6 8 9.7e-10DBODY 7 5 DBDMOD  
DBREAK 5 11 DBKMOD  
DPLCAP 10 5 DPLCAPMODEBREAK 11 7 17 18 65.9  
EDS 14 8 5 8 1  
EGS 13 8 6 8 1  
ESG 6 10 6 8 1  
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9  
LGATE 1 9 4.92e-9  
LSOURCE 3 7 4.5e-9MOS1 16 6 8 8 MOSMOD M = 0.99  
MOS2 16 21 8 8 MOSMOD M = 0.01RBREAK 17 18 RBKMOD 1  
RDRAIN 50 16 RDSMOD 1.1e-3  
RGATE 9 20 2.88  
RIN 6 8 1e9  
RSCL1 5 51 RSCLMOD 1e-6  
RSCL2 5 50 1e3  
RSOURCE 8 7 RDSMOD 20.3e-3  
RVTO 18 19 RVTOMOD 1S1A 6 12 13 8 S1AMOD  
S1B 13 12 13 8 S1BMOD  
S2A 6 15 14 13 S2AMOD  
S2B 13 15 14 13 S2BMODVBAT 8 19 DC 1  
VTO 21 6 0.764

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)\*1e6/108,6))}

.MODEL DBDMOD D (IS = 2.32e-13 RS = 5.72e-3 TRS1 = 2.56e-3 TRS2 = -5.13e-6 CJO = 1.18e-9 TT = 5.62e-8)

.MODEL DBKMOD D (RS = 2.00e-1 TRS1 = 3.33e-4 TRS2 = 2.68e-6)

.MODEL DPLCAPMOD D (CJO = 6.55e-10 IS = 1e-30 N = 10)

.MODEL MOSMOD NMOS (VTO = 3.89 KP = 15.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)

.MODEL RBKMOD RES (TC1 = 1.04e-3 TC2 = -1.04e-6)

.MODEL RDSMOD RES (TC1 = 5.85e-3 TC2 = 1.77e-5)

.MODEL RSCLMOD RES (TC1 = 2.0e-3 TC2 = 1.5e-6)

.MODEL RVTOMOD RES (TC1 = -5.35e-3 TC2 = -3.77e-6)

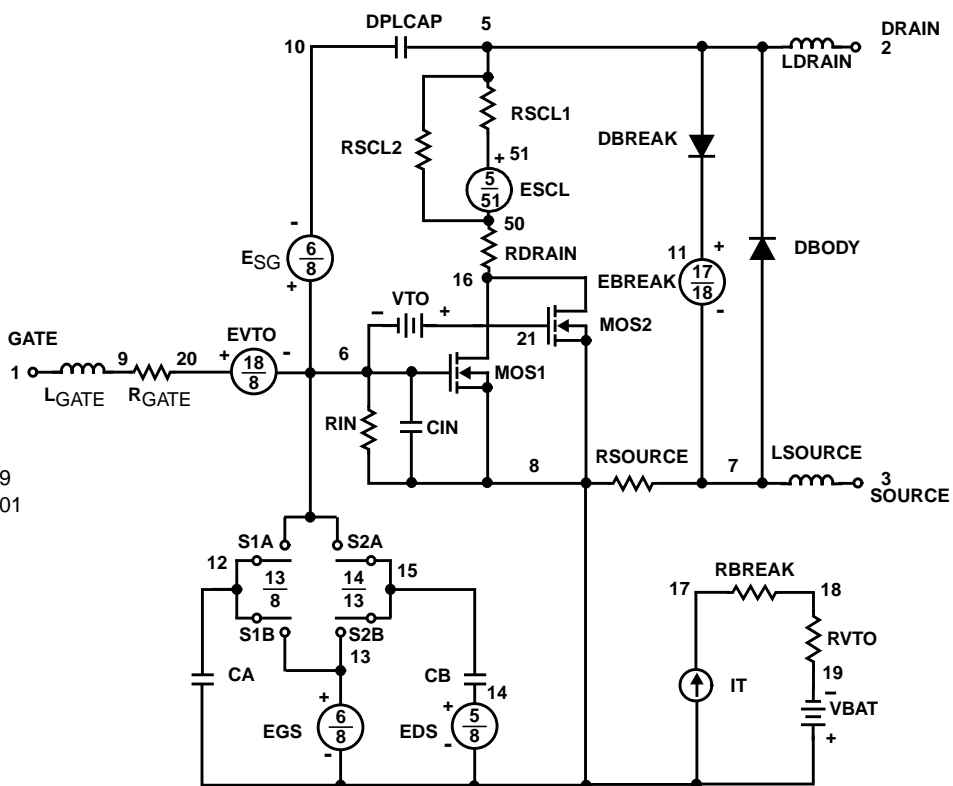
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.04 VOFF = -3.04)

.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.04 VOFF = -5.04)

.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.02 VOFF = 1.98)

.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.98 VOFF = -3.02)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

### **Sales Office Headquarters**

#### **NORTH AMERICA**

Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (407) 724-7000  
FAX: (407) 724-7240

#### **EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

#### **ASIA**

Intersil (Taiwan) Ltd.  
7F-6, No. 101 Fu Hsing North Road  
Taipei, Taiwan  
Republic of China  
TEL: (886) 2 2716 9310  
FAX: (886) 2 2715 3029